GD CONTROL DATA

CDC® KEY TO LEVEL 4 LOGIC DIAGRAMS

SYMBOL DESCRIPTIONS

12AA THROUGH 12AS, 12CA THROUGH 12CV

VOLUME 1

LOGIC DIAGRAM SYMBOLS MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A (12-01-82)	Manual released.
B (04-16-84)	Engineering Change Order 45780. Manual revised to accommodate technical and editorial corrections. Because of extensive changes to this manual, chart tape and dots have not been used, and all pages reflect the latest revision level. This revision obsoletes all previous editions.
C (12-04-84)	Manual revised; includes Engineering Change Order 46650. Front Cover through 4 and 12CI-0 (2 of 5) in Volume 1 are revised.
D (04-15-85)	Manual revised; adds CYBERPLUS Arrays. In Volume 1, changed Front Cover, Title Page, Revision Record, 3 and 4. Added 5 and 6; changed old 5/6 to 7/8; changed 2-1, 12CB-5 (1 of 1), and Comment Sheet. In Volume 2, changed Front Cover, Title Page, Revision Record, 3 and 4. Added 5 and 6; changed old 5/6 to 7/8; changed 12SD-0 (1 of 1), and Comment Sheet. Inserted new index tab 12DA and pages 12DA (1 of 1), 12DB-0 (1 of 1), 12DB (1 of 1), 12DB-0 (1 of 1), 12DB-1 (1 of 1), 12DB-2 (1 of 1), 12DB-3 (1 of 1), 12DB-4 (1 of 1), 12DC (1 of 1), 12DC-0 (1 of 1), 12DD (1 of 1), 12DD-0 (1 of 1), 12SB (1 of 1), 12SB-0 (1 of 2), 12SB-0 (2 of 2), 12SB-1 (1 of 2), 12SB-1 (2 of 2), 12ST (1 of 1), 12ST-0 (1 of 2), 12ST-0 (2 of 2), 12SU (1 of 1), 12SU-1 (1 of 1), 12SX (1 of 1), 12SX-1 (1 of 2), 12SX-1 (2 of 2), 12122-1 (1 of 1), 12122-2 (1 of 1), 12141-1 (1 of 1), 12165-1 (1 of 1), 12180-1 (1 of 1), 12470-1 (1 of 1), 12474-1 (1 of 1).
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Publication No.	
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REVISION LETTERS I, O, Q, S, X AND Z ARE NOT USED.

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or use Comment Sheet in the back of this manual.

PREFACE

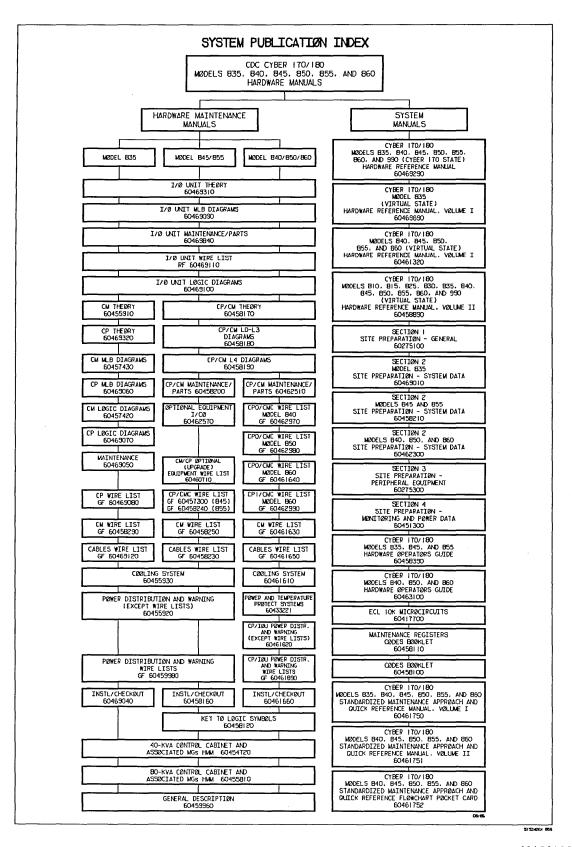
This manual is one of a set of manuals for the $CDC^{\textcircled{0}}$ CYBER 170 Models 845 and 855 Computer Systems, CYBER 180 Models 840, 845, 850, 855, 860, and 990 Computer Systems, CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 990E, and 995E Computer Systems, and the CYBERPLUS Parallel Processor. The System Publication Indexes on the following pages list other manuals that are applicable to the computer equipment.

This manual contains two volumes. Volume 1 contains the key to level 4 (L4) diagrams section and the Symbol Descriptions section for the 12AA through 12CV LSI arrays. Volume 2 contains the Symbol Descriptions section for the 12DA through 12DD LST arrays, the 12SA through 12SX LSI arrays, the 12101 through 12474 Emitter Coupled Logic (ECL) 100,000 series microcircuits, and the 12HA through 121HH half-arrays.

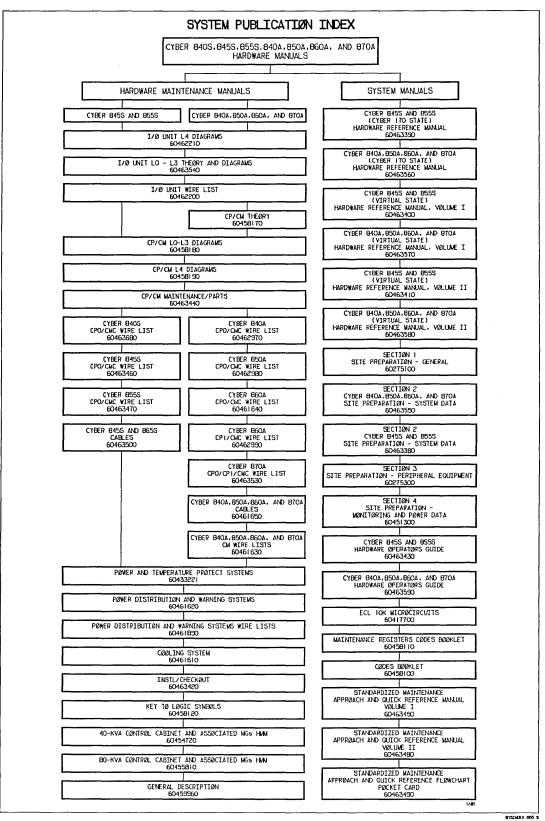
The key to L4 diagrams section describes the L4 diagrams and supplementary charts such as backup charts and connector charts. The Symbol Descriptions section provides an operational description, pin number and bias information for every logic circuit used in the central processor.

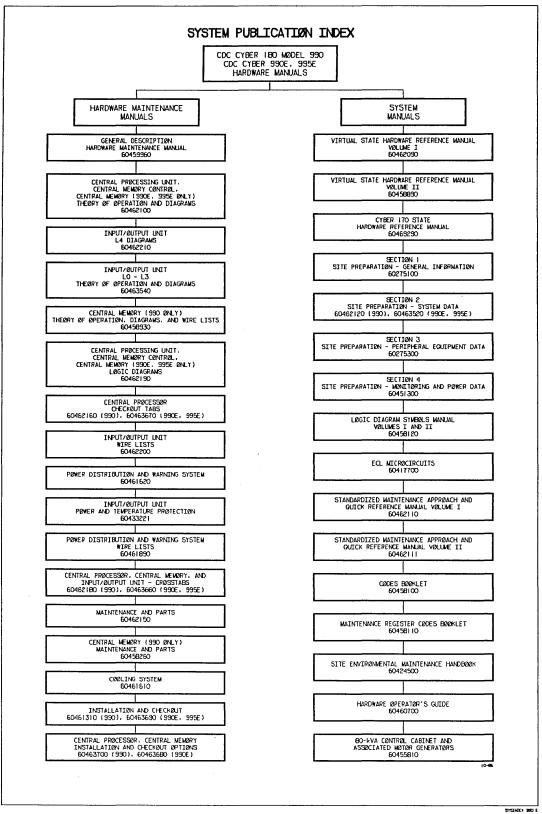
This manual is intended primarily for customer engineers and does not contain design ground rules. Logic designers should refer to applicable Control Data specifications and vendor literature for complete electrical characteristics and application guidelines.

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RELATED PUBLICATIONS (CYBERPLUS)

Following is a list of other manuals applicable to the CYBERPLUS Multiparallel Processor System. The manuals are available from:

Control Data Corporation Literature and Distribution Services 308 North Dale Street St. Paul, Minnesota 55103

<u>Title</u>	Publication Number
Medium and Large Scale Computer Systems, Site Preparation Manual, Section 1, General Information	60275100
CYBERPLUS Parallel Processor Site Preparation Manual, Section 2, Site Data	60461720
Medium and Large Scale Computer Systems, Site Preparation Manual, Section 3, Peripheral Equipment Data	60275300
Medium and Large Scale Computer Systems, Site Preparation Manual, Section 4, Monitoring and Power Data	60451300
Site Environmental Maintenance Handbook	60424500
CYBERPLUS Parallel Processor Hardware Maintenance Manual, Volume l Installation and Checkout	60461740
CYBERPLUS Parallel Processor Hardware Maintenance Manual, Volume 2 Maintenance and Parts Data	60461850
CYBERPLUS Parallel Processor Hardware Maintenance Manual, Volume 3 Diagrams	60461830
CYBERPLUS Parallel Processor Hardware Maintenance Manual, Volume 4 Troubleshooting	60462390
CYBERPLUS Parallel Processor Hardware Reference Manual	77960981
CYBERPLUS Parallel Processor Wire Lists	60461870

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RELATED PUBLICATIONS (CYBERPLUS), Cont'd

<u>Title</u>	Publication Number
CYBERPLUS Parallel Processor CYBER 180 Models 840, 850, 860, 990 CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 990E, 995E Cooling System Hardware Maintenance Manual	60461610
CYBERPLUS Parallel Processor CYBER 180 Models 840, 850, 860, 990 CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 990E, 995E Power Distribution and Warning System Hardware Maintenance Manual	60461620
25-kVA Frequency Converter Hardware Maintenance Manual	60456520
40-kVA Control Cabinet and Associated Motor-Generators Hardware Maintenance Manual	60454720
80-kVA Control Cabinet and Associated Motor-Generators Hardware Maintenance Manual	60455810
CYBERPLUS Parallel Processor Maintenance Software Manual	60461730
Concurrent Maintenance Library (CML) Reference Manual	60455980

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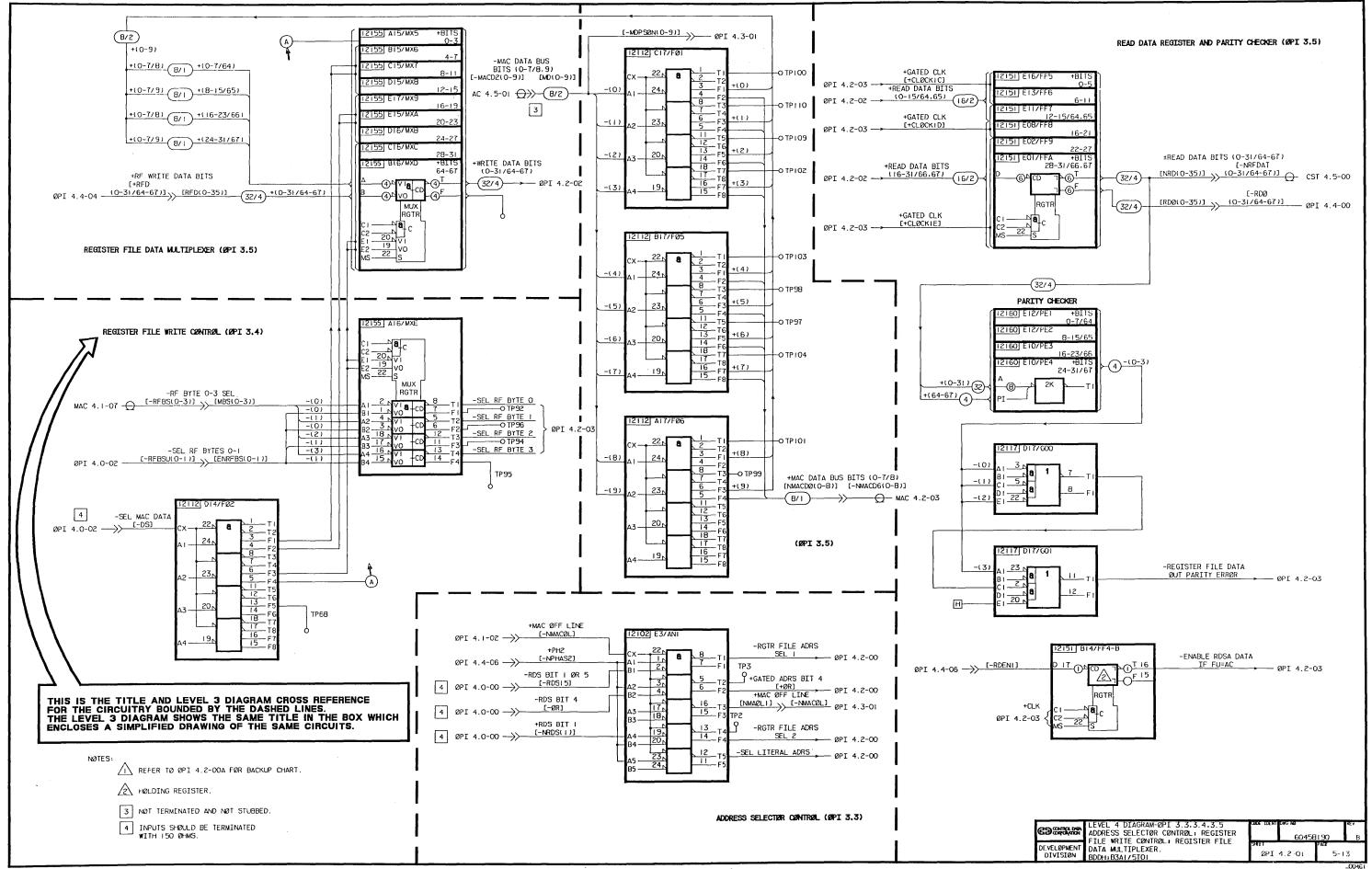
SECTION 1

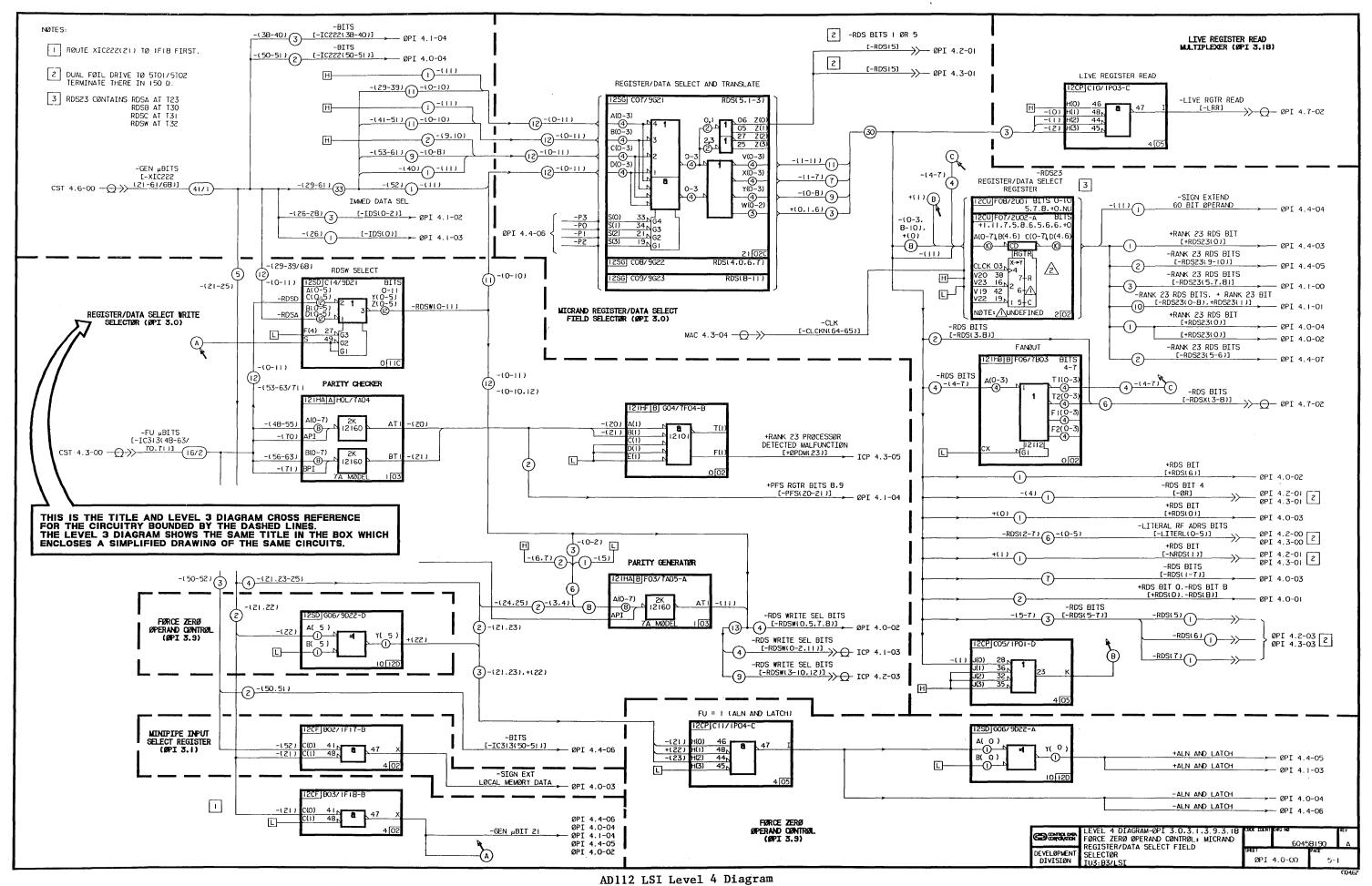
KEY TO LEVEL 4 LOGIC DIAGRAMS

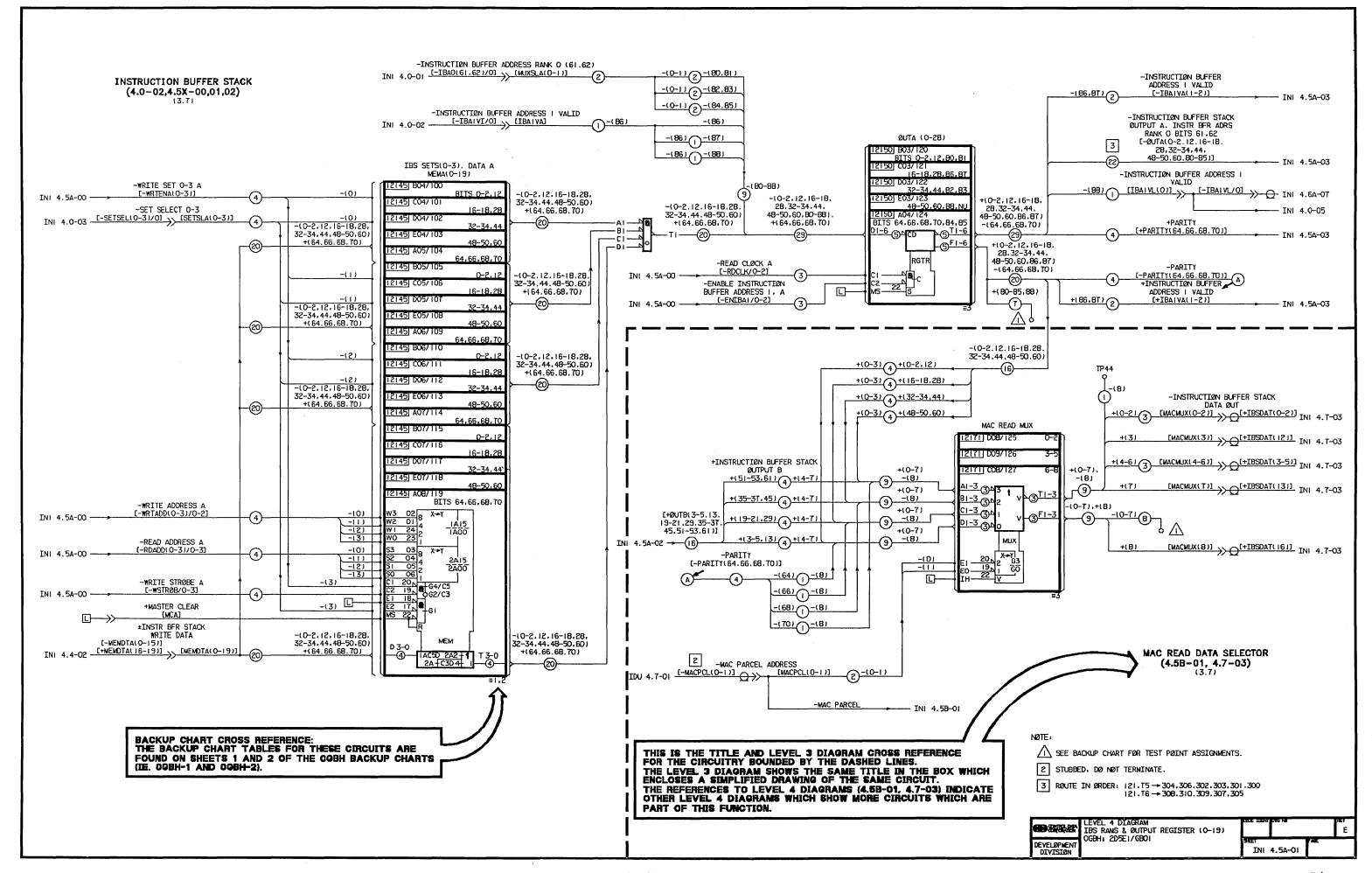
INTRODUCTION

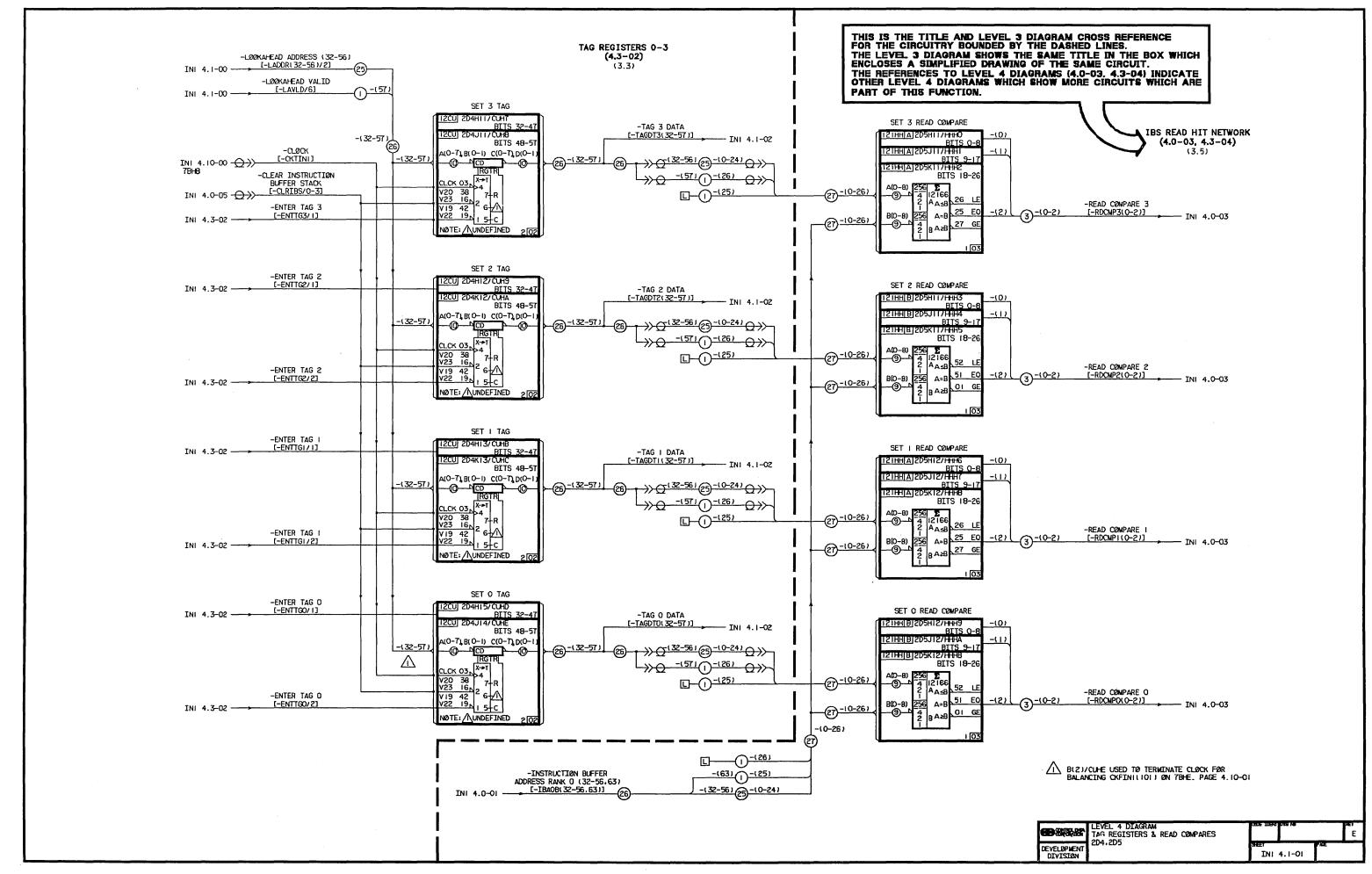
The Level 4 (L4) logic diagram shows the ECL 100K chips and LSI arrays and all data and control paths between them. This diagram also shows the functional relationship between the inputs and outputs to each array/chip with ANSI symbology. The L4 diagram is the lowest level diagram provided for field maintenance. The following examples show ECL 100K L4 diagrams and LSI L4 diagrams.

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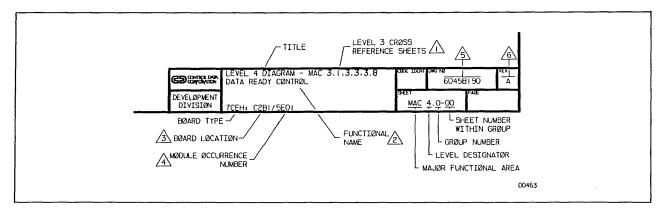




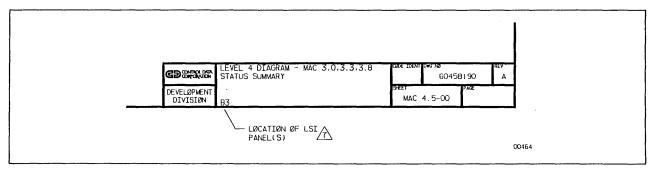


TITLE BLOCKS

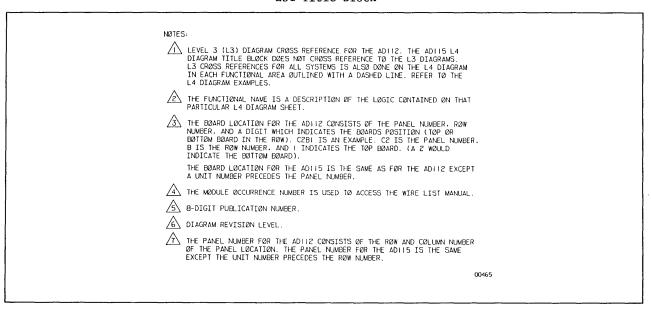
The title blocks for the ECL 100K and LSI L4 diagrams are shown in the following examples. They differ only in the addition of a board type and module occurrence number for ECL 100K L4 diagrams.



ECL 100K Title Block

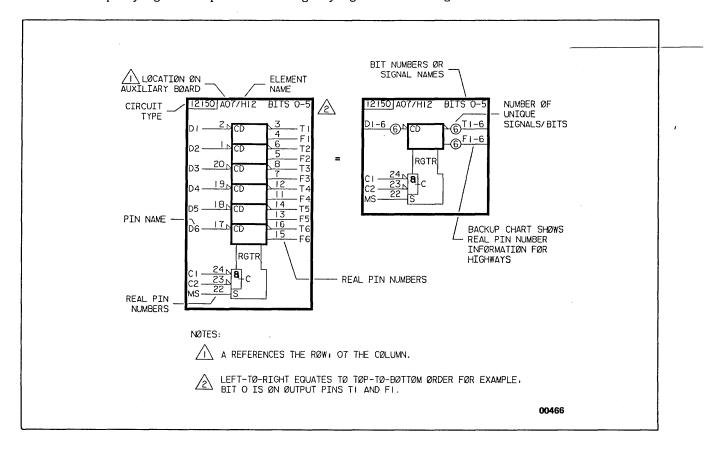


LSI Title Block

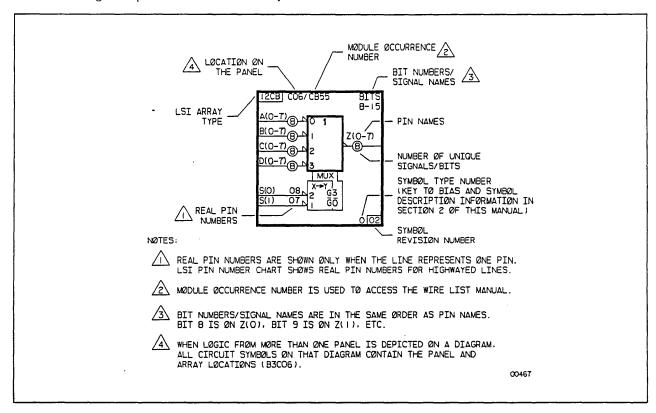


SYMBOLOGY

Physical components (ECL 100K chips, LSI arrays, and half-paks) are depicted by boxes containing ANSI symbology. The following examples use standard ANSI symbols enclosed in boxes. The example on the right shows the same ECL 100K circuit as does the one on the left but uses simplifying techniques called highwaying and combining.

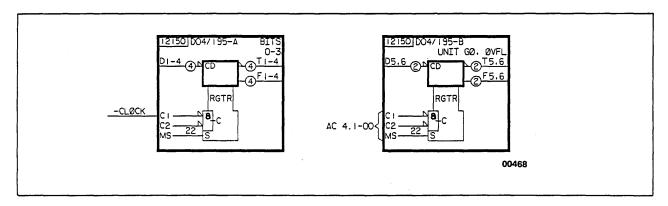


The following example shows an LSI array.



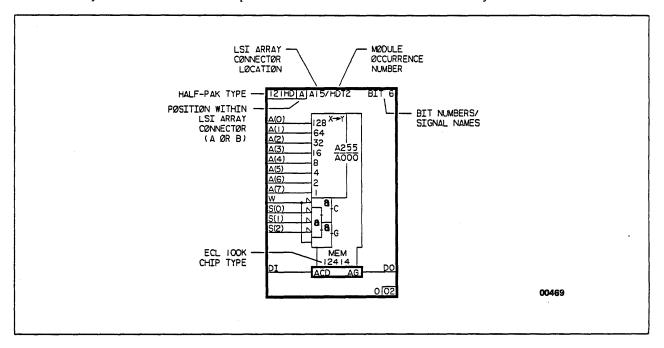
Sometimes a chip is shown more than once in a group of diagrams. The following examples show two symbols for the same 12150 chip. The example on the left shows four circuits used for bits 0 through 3. The example on the right shows the remaining two circuits used for the signals Unit Go and Overflow. Note that the control signal (-CLOCK) is shown only once.

The element name for this chip is 195 and is the same for each use. The element name is followed by a dash and a multiple-use identifier. The first place the element is used, the multiple use identifier is an A. Further uses of the same element receive multiple-use identifiers of B, C, D, etc.



LSI HALF-PAK ARRAY

The following example shows an LSI half-pak array circuit. An LSI half-pak is an ECL 100K chip packaged in a form compatible with an LSI array connector. A half-pak occupies half of an LSI array location. Two half-paks can reside at the same LSI array location.

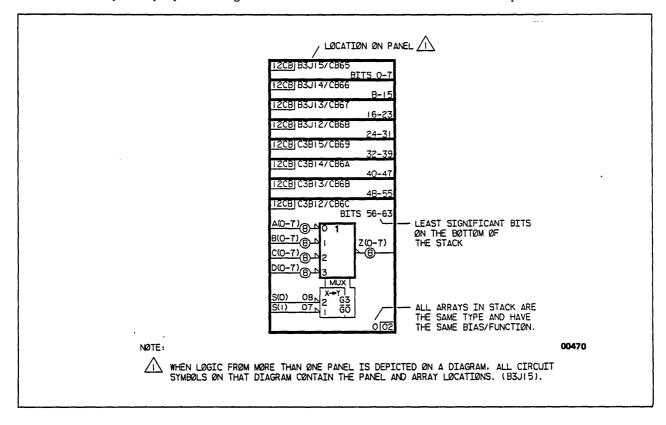


1-14

STACKING

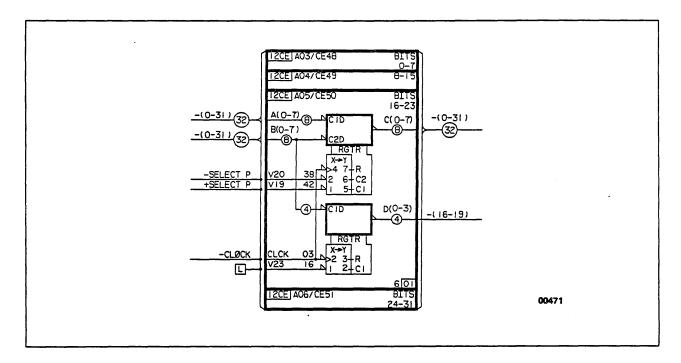
The following example shows eight 12CB arrays performing a MUX operation to a 64-bit trunk. The stack is split across two panels so the panel and array locations are shown in each symbol.

Identical arrays/chips performing the same function are stacked wherever possible.



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The following example shows a case where the least significant bits (bottom of the stack) are not the ones pictured. This occurs when one of the other arrays in the stack performs a unique or additional function. The least significant bits are still on the bottom but the atypical array is diagrammed. In this case, bits 16 through 19 are latched into another register and output on pins D (0 through 3) of the array at location AO5.



FUNCTIONAL INTERCONNECTION

Functional interconnection of the logic is accomplished by lines representing signals interconnecting the ANSI symbols.

These signal lines are a functional interconnection and do not represent the physical order of routing, as in daisy chains, or the number of physical conductors carrying logically identical signals as in a fanout. The explicit physical interconnection information is contained in the CP/CMC Wire List Hardware Maintenance Manual listed in the preface.

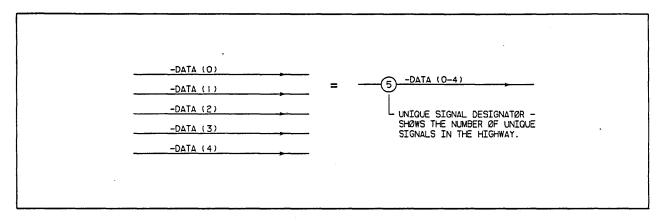
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INTERCONNECTION TECHNIQUES

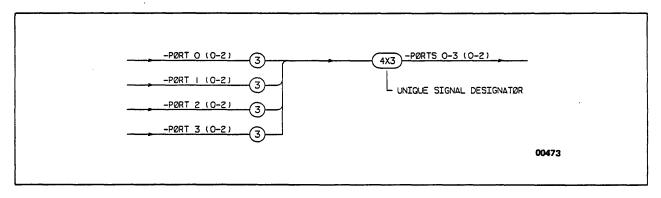
Interconnection techniques are the methods used to combine, expand, and depict the data/control path lines between circuit symbols on the diagrams.

HIGHWAYING

Highwaying is a technique which combines more than one signal into a common line. The following example shows how the same information can be contained in one line instead of many.

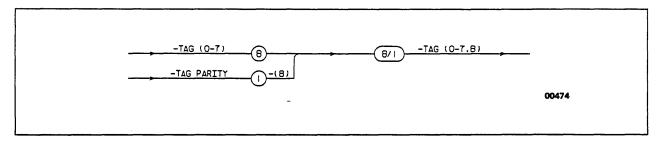


Similar signal groups from various sources are combined in a highway as shown in the following example. The first number in the unique signal designator of the highwayed signal is the number of signal groups combined and the second number is the number of signals/bits per line.



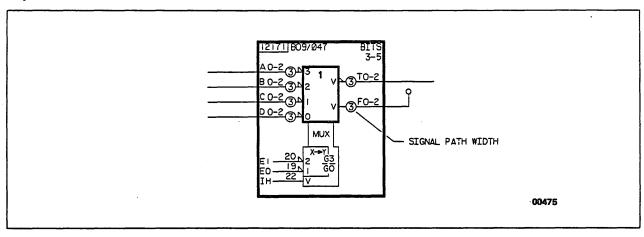
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Parity signal lines are highwayed as shown in the following example.



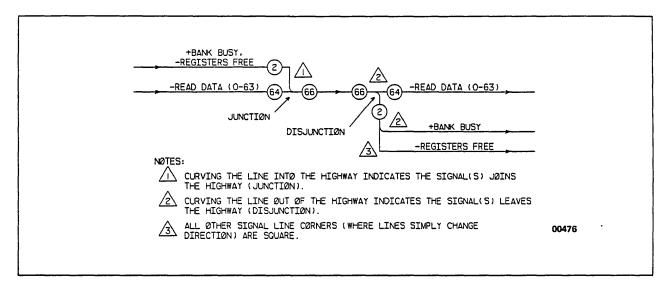
Signal path width relates to the number of unique signals represented by the path. Multiple copies (fanouts) of the same signal do not increase the count.

The circled number embedded in a lead denotes the signal path width. The following example shows six 3-bit widths. A lead without a circled number denotes a single bit width (control inputs).

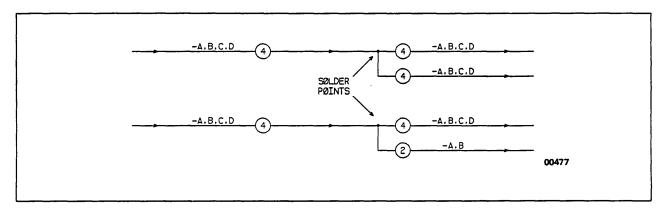


CONNECTIONS

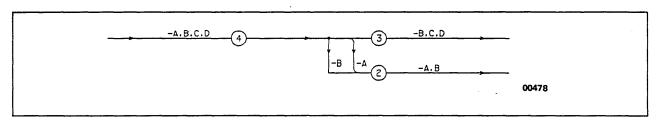
Signals join (junction) or leave (disjunction) a highway as shown in the following example.



Solder points on a highway indicate that signals are tapped out of the highway, and are fanned out to more than one location. Refer to the following examples.



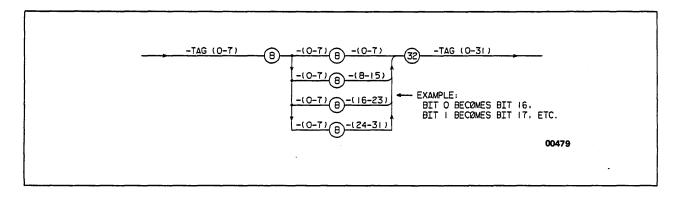
The following example shows a complex disjunction which is formed when some signals leave the highway and some are tapped out. Instead of showing complex disjunctions as they actually are, as in the following example, the diagrams use the solder point as in the preceding example. The complex disjunction is defined by the signal names entering and leaving the disjunction.



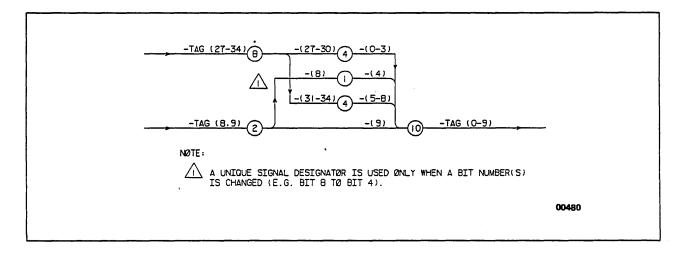
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BIT NUMBER CHANGES

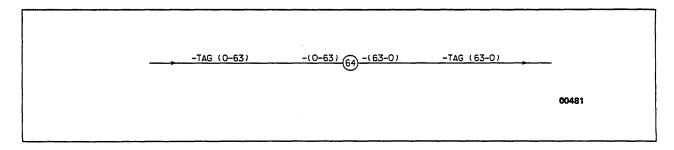
Bit number changes along a highway occur for many reasons (for example assembling data into wider highways or merging two or more highways). The following examples represent the various techniques used for changing bit numbers for an 8-bit highway expanding to a 31-bit highway, two highways merging, and an end-for-end swap, respectively.



8-Bit Highway Expanding to 31-Bit Highway



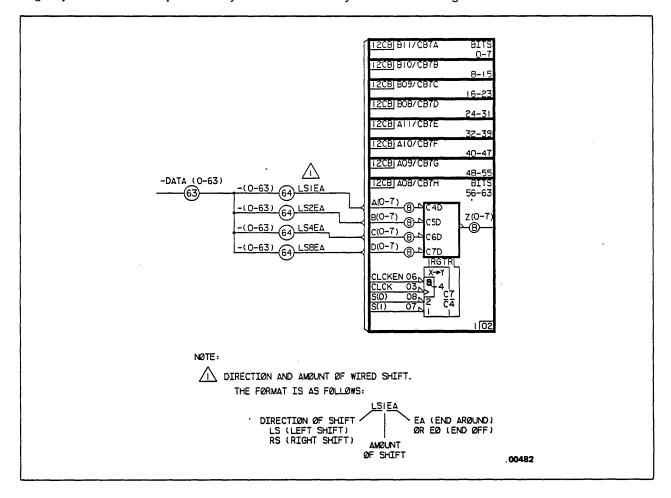
Two Highways Merging



End-For-End Swap

1-20

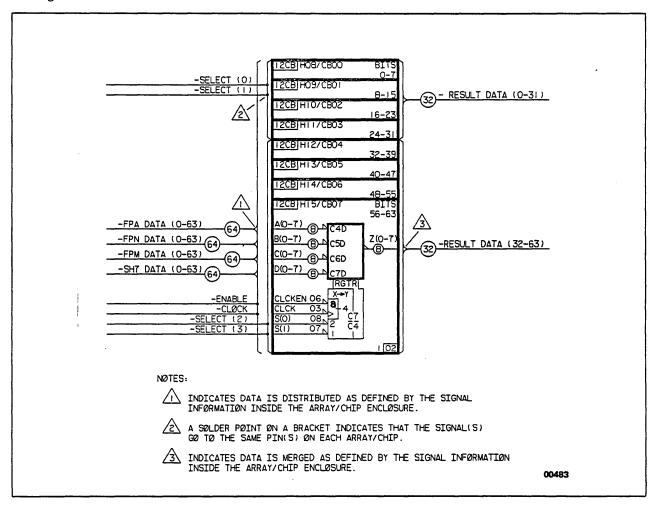
The following example shows a wired shift which is similar to changing bit numbers along a highway. This technique is only used immediately before entering a bracket.



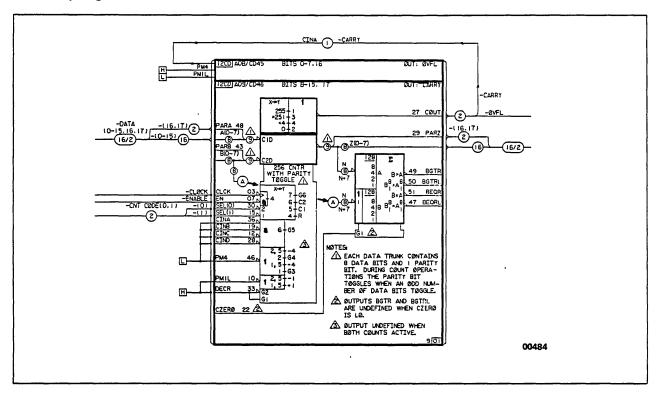
BRACKETING

Bracketing is the technique which shows the connection of the single and highwayed signals to stacks of LSI arrays or ECL 100K chips.

Multiple brackets show more complex data and control distribution. In the following example the brackets distribute the bits in the input data trunks among all the arrays in the stack. The enable and clock signals also connect to each array in the stack and can use the same bracket as the input data. The select signals do not connect to the entire stack. Select (2) and (3) connect to a bracket adjacent to arrays at locations H12 through H15. Select (2) connects to pin S(0) of these arrays and Select (3) connects to pin S(1). The order (from top-to-bottom) that the Select (0) and (1) signals connect to the top bracket must be the same as the Select (2) and (3) signals connect to the bottom bracket. Therefore Select (0) connects to pin S(0) and Select (1) connects to pin S(1) on arrays at locations H08 through H11.



The following example shows a 16-bit counter composed of two 12CD arrays. In this example, the array at location AO9 has the CINA and PM4 signals biased low and PM1L biased high. These connections are made by passing the signals through the bracket directly to the array. In like manner, the array at location AO8 has PM4 biased high, PM1L biased low, and the carry signal connects to CINA.



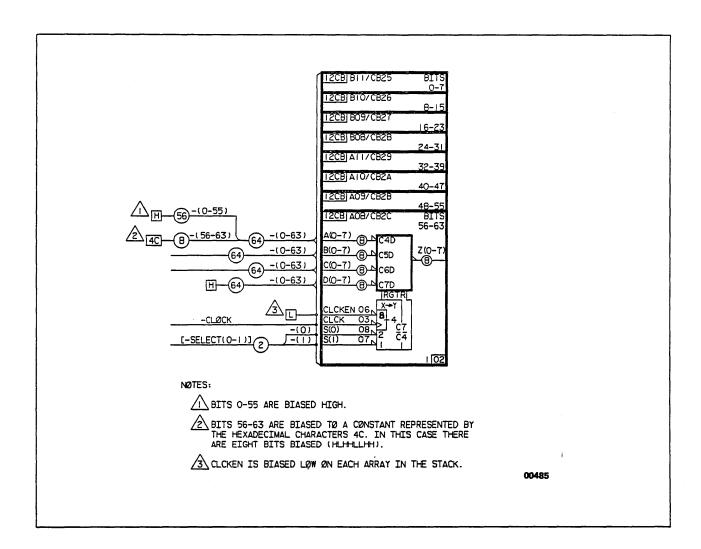
BIAS/CONSTANTS

The following example depicts bias/constant signals. Bias signals are those which are connected to a static high or low logic level. A box around an L or H indicates a static low or high logic level.

A constant signal is a value which is invariable in a given operation or calculation. In the following example, 8 bits are biased to the hexadecimal constant 4C(HLHHLLHH).

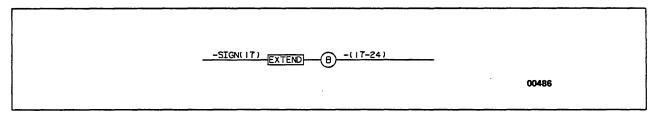
When the number base does not fit evenly into the number of bits biased, the bits are considered right justified (for example, groups of bits marked off starting from the least significant end of the bit string).

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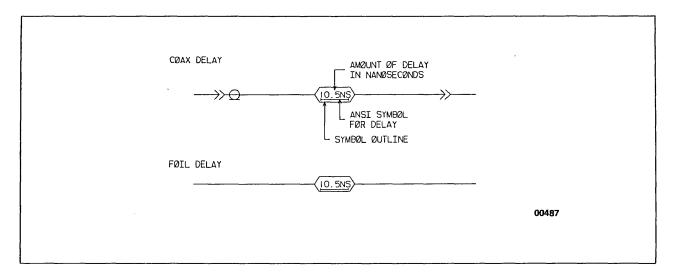


EXTENDING/DELAYING

A signal may be extended (fanned out) into several bit positions as shown in the following example of sign extension.

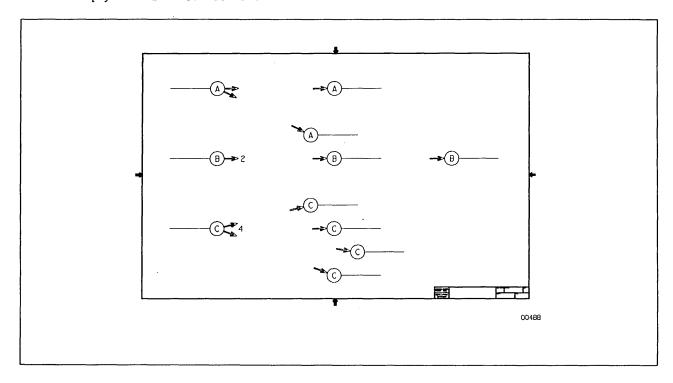


A signal may be delayed by the number of nanoseconds specified as shown in the following examples.



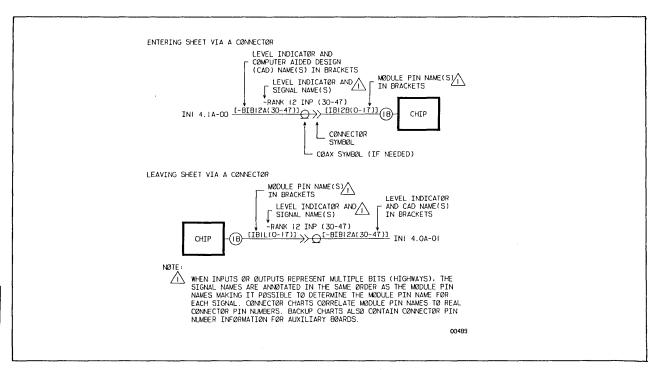
REFERENCES

The technique used to indicate an on-sheet reference is shown in the following example. On-sheet references represent a means of connecting one or more symbols on the same page without a physical line connection.

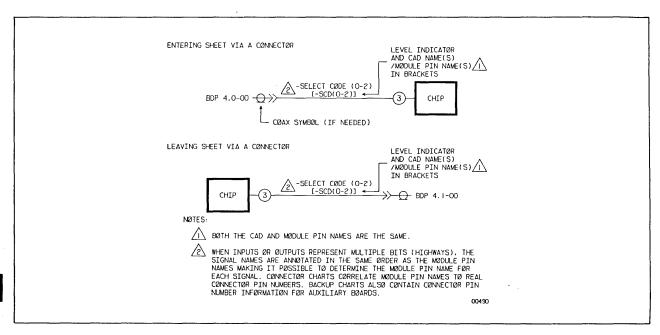


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In the following examples, off-sheet references through a connector are separated into three categories: multiple-use auxiliary boards, single-use auxiliary boards, and LSI.



Multiple-Use Auxiliary Board



Single-Use Auxiliary Board

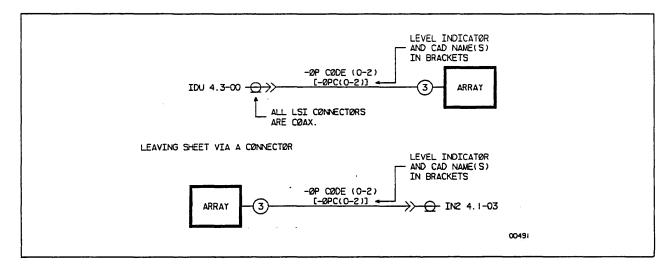
When the signal enters or leaves a connector through coax, the coax symbol is used with the connector symbol.

When an LSI circuit connects to an auxiliary board through foil, the connector symbol is shown on the auxiliary board L4 diagram.

When an LSI circuit connects to an auxiliary board through coax there are two connector symbols; one on the LSI L4 diagram for the LSI coax connector and one on the auxiliary board L4 diagram for the auxiliary board connector. Coax symbols also show that the connection was through coax.

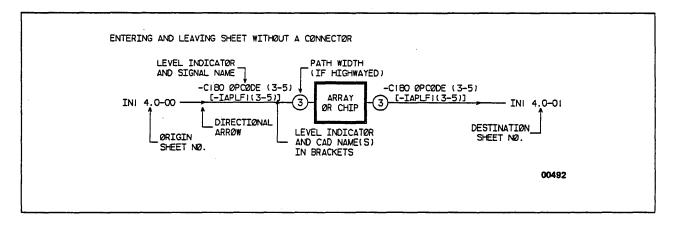
When LSI connects to LSI through coax there are two connector symbols on the LSI L4 diagram(s) as shown in the following example; one where the signal leaves an array through an LSI coax connector and one where the signal enters another array through an LSI coax connector. There is one exception to this rule. When an LSI L4 diagram depicts more than one panel, the connectors between the panels depicted on the diagram are not shown.

When LSI connects to LSI through foil, no connector symbol is necessary.



LSI

Off-sheet references without a connector are shown in the following example. All off-sheet references have a meaningful signal name and may also have a computer aided design (CAD) name to describe it. The names for a signal or highway are the same at each end.

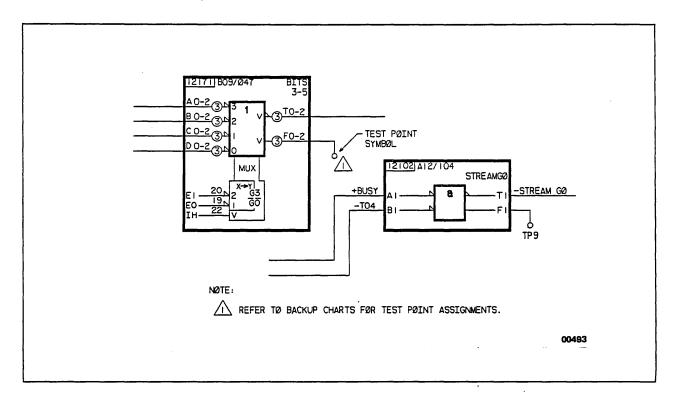


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TEST POINTS

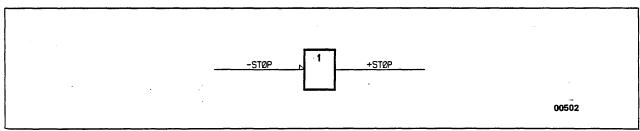
Test points connect to unused pins and are available on auxiliary boards only.

When the test point symbol represents a single test point, the test point number appears adjacent to it on the L4 diagram. When the test point symbol represents a highway (multiple test point), a note refers the user to the appropriate L4 backup chart (refer to the following example). The L4 backup charts contain the test point pin numbers as destinations of the appropriate unused pins.



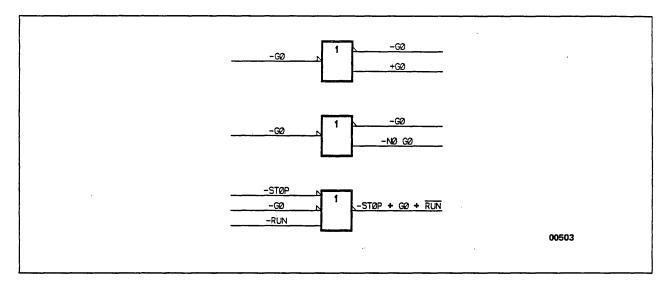
SIGNAL LEVELS

All signal names are preceded by an active LO (-) or an active HI (+) level indicator as shown in the following example.



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The following example shows that NOT bars are not used except within Boolean expressions.



NOTES

Notes are numbered statements or tables located around the periphery of the diagram, usually at the bottom. They explain diagram conventions that are not obvious and are unique to that diagram. Conventions that apply to all L4 diagrams are described in this manual.

Notes may be general or specific. A general note refers to the entire diagram or to a convention used frequently on the diagram. A specific note relates to a specific circuit, item, or area. Specific note numbers are enclosed in triangles which relate them to numbered triangles near the diagram conventions they describe.

AD112 LEVEL 4 BACKUP CHART

The AD112 Level 4 backup chart example shows a L4 backup chart. L4 backup charts contain tabular information supplementary to highwayed or stacked elements on a L4 diagram. The L4 backup charts show real and virtual pin numbers, bit numbers, and element names.

All ECL 100K circuits which are depicted highwayed or stacked on auxiliary boards have individualized L4 backup charts which relate signals to pin names and real pin numbers. When the L4 backup charts represent all the elements in a stack, they are arranged from left to right or top to bottom on the sheet. The left or top element on a backup chart represents the top element in the stack (lowest bit number).

Stacked LSI circuits do not use individualized backup charts. LSI pin number charts show the relationship between pin names and real pin numbers. The LSI pin number charts are located in section 2 of this manual.

12155		LØ	IC:	C3		NAL	E٠	MOO	
SØURCE	DAISY	T	ĬΡ	R TP	HAME	R ØP	ØP.	DEST	L
LØ		7	ΑĪ	04		105	TI	TERM	П
P2A-01		T	BI	03	_ 0	06	FΙ	D2-14	
LØ]_	Ã2	02		08		TERM	Г
P2A-03		ŢΪ	BZ	ΟĪ	i '	07	F2	D2-17	1
CB-14		ΤŦ	A3	16	2	173	T3	TERM	Т
P1A-39		17	B3	15	۲ ا	14	F3	D2-19	Г
B8-05	G4-02	T-	A4	ĪΒ	3	12	T4	TERM	$\overline{}$
P1A-37		IT	B4	17		II	F4	D2-16	
		Γ	Cī	24					
		Г	CZ	23	ı				
D5-08	C3-19	Т	EI.	20					
C3-20	B3-20	Γ	EZ MS	19	ļ				
		T	MS	22	i				

SOUNCE	CHATN	Ľ.	IP	ĮP.	NAME	2P		DEST
C122		T	AI	15		14		F10-16
P2B-27		T	ВІ	16	6	13	FI	TERM
P28-34		T	CI	17				_
D2-13		I	DI	18				
C92		T	A2	23		Ξ.		F10-24
P2B-29		I	B2	24	7	12	F2	TERM
P2B-38		T	ß	0	' '			
D2-15		T	D2	02				
C87		T	A3	03		70	T3	F10-04
P2B-30		Т	В3	04	8	08	F3	TERM
P2B-40		T	C3	05				
D2-11		T	D3	06				
G9-20		T	ĒΙ	20				
G9-19		T	ΕO					
			ĬΗ	22				

12171		L£	IC:	GIC		NAL	Œ:	MO4	
SØURCE	DAISY	T	ΙP	R	BIT	R 2P	₽ V	DEST	L
C122		ĪŦ	AI	15		14	TI	F10-16	T_
P2B-27		T	BI	16	6	13	FI	TERM	T_
P28-34		ÌΤ	CI	17	٥ ا	ſ			
D2-13		T	DI	18	l	l			
C92		T	A2	23				F10-24	L
P2B-29		T	B2	24	7	12	F2	TERM	L
P2B-38		T	CZ	01	l '				
D2-15		IT	D2	02		L			_
C87		T	A3	03				F10-04	T
P2B-30		T	B3	04	8	08	F3	TERM	L
P2B-40		T	CZ	05	٥	1			
D2-11		T	D3	06		_			
G9-20		ŢΤ	ΕĪ	20					
G9-19		T	EO		l				
			ĬΗ	22					

12192	LØC:	CI		NAK	Œ١	TOI	
SØURCE DAISY CHAIN	T V	R IP	BIT NAME	R	γP	DEST	L
C2-05	TAL	02	0	05	TI	P1A-23	
			١	04		P1A-26	
B2-08	ZA T	ΟĪ	-	07		PIA-2T	
				06	F2	PIA-24	
B2-13	T A3	18	2	12			
				13	F3	P1A-22	
B2-12	T A4	17	3	14	T4		
				15	F4	P1A-20	
				08	T5		
				Ш	T6		
	CX	22					
	CY	20					

12155		L	C:	В3		NAL	Œŧ	MOI	
SØURCE	CHATN	T	IP	R	BIT NAME	R ØP	ØΡ	DEST	L
C9-15	G4-06	Γ	ΑI	02	4	08	TI	TERM	
P2A-02		II	Bi	ΟĪ	_+	07	FI	D2-18	T
G4-05	CB-02	L	SA	16	5	Τŝ	TZ	TERM	П
P2A-04		I	B2	15		14	F2	D2-20	
C9-07	G4-04	\prod	Ã3	04	6	05	T3	TERM	
PIA-40		Ī	B3	03		06	F3	D2-13	Ι.
B7-13	G4-03	Ι	Α4	18	7	12	T4	TERM	Ī
P1A-38		ĮΤ	B4	17		Ш	F4	D2-15	\Box
		1	Cï	24					
		Т	CZ	23					
C3-19	B3-19	П	ĒΙ	20					
B3-20	A7-17	Т	ĒŽ	19					
		Γ	MS	22					

12171		L	IC:	FB		NAM	E:	MO5	
SØURCE	DAISY	Т	IP.		BIT	R ØP	ØΡ	DEST	L
F4-20		T	ΑI	23		TT.	TI	C2-04	
GB-14		Т	ΒI	24	0	12	FΙ	TPIO	
CBO		T	c	ΟI					
P2B-18		T	D	02					
F2-03		T	A2	03				B2-02	
GB-11		Т	B2	04		08	F2	TP13	
C71	Γ'	T	CZ	05	'	\Box			
P2B-14		T	D2	06	l				
F4-04		T	Α3	15				B2-16	
GB-07		T	R	16	2	Σ	F3	TP08	
C75		T	ន	17	ے ا				
P2B-12		T	D3	18					
F9-20		T	ĒΤ	20					
F9-19		T	ΕO	19					
			H	22					
			_						_

MUNCE.	CHAIN	Т	ΙP	IP	NAME NAME	R ØP	ØP	DEST	L
0-II		T	Αľ	04	0	05	TI	C1-02	
Ι			BI	03			FI	A3-24	
			AZ	02		08	T2		
			B2	<u>ie</u>		07	F2		
			A3			13	T3		
			B3	15		4	F3		
			A4	18		2	T4		
			B4	17		\equiv	F4		
7-15	B2-24		CI	24		_			
04-16	B02-23		C2	23	l				
2-19		I	EL	8					
2-20	C2-20		E2	-9	Ī				
			MS	22					

12192		Le	C:	BI		NAM	F١	TO2	
SØURCE	DAISY CHAIN	T	V IP	R	BIT	R pp	ØP.	DEST	L
B2-05		T	ΑĪ	02	4	05	ŤΙ	P1A-15	
					-7	04	FL	BI-AIG	
A2-08_		T	A 2	OI	5	07	T2	PIA-13	
					l	06	F2	PIA-14	
A2-05		T	A3	18	6	12		PIA-II	
				•	١٥	13	F3	PIA-12	
A2-13		T	Α4	17	7	14	T4	P1A-09	
					11	15	F4	PIA-IO	
				_		08	T5		
						III	T6		
		I	CX	22					
		T	CY	20	i i				

12171		LØ	JC:	G8		NAM	E٠٨	102	
SØURCE	DAISY CHAIN	T	JP.	R IP	BIT NAME	R ØP	ØP.	DEST	L
C/6		Ī	AI.	15		13		FB-24	
P2B-19		T	BI	16	ا ا	14	FI	TERM	
P2B-31		T	Cï	17	0				
D2-14		Ŧ	DI	18			_		
C79		Ī	A2	23		Π		FB-04	
P2B-20		Т	D2 C2	24		12	F2	TERM	
P2B-33		T		01	' '				
D2-17		I	D2 A3	02		l			
C60		T				07		F8-16	
P2B-21		Τ	B3	04	2	08	F3	TERM	
P2B-35		Τ	C3	05	-				
D2-19		I	D3						
A7-07	G9-20		ΕÏ	20					
A7-11	G9-19		EΟ	19					
		L	ΙH	22					

12171		LØ	C:	F9		NAM	Œι	MO6	
SØURCE	DAISY CHAIN	Т	IP	R IP	BIT NAME	R ØP	ØP.	DEST	L
F04-03		T	ΑI	03		07	TI	B2-18	Т
G9-11		T	BI	04	3	08	FΙ	TP21	Т
CIIO		ŢΤ	CI	05	٦	Г			
P2B-10		T	DI	06	1				
E2-03	C7-02	T	A2	15		14	T2	B2-04	T
G9-07		T	B2	16	4	13	F2	TP25	Т
C114		T	CZ	17	-				
P2B-08		TŦ	DZ	18		1			
F5-16		ΤŦ	Ã3	23		111	T3	A2-02	Т
G9-14		T	B 3	24	5	12	F3	TPIB	Т
C113		T	C3	ΟI	5				
P2B-06		T	D3	02		1			
F10-20	F8-20	Т	EŢ	20					
F10-19	F8-19	T	EO	19	l				
		Ι	ĪΗ	22					

SOURCE	CHAIN	Т	IP.	IP.	NAME.	P P	ØP	DEST	L
8-07		Ŧ	ΑĪ	Ó2	,	08	Ti	CI-0I	
Ī			ВІ	OI.	_ '	07	FI	A3-05	
8-14		Ī	A2	TG	2	13	T2	C1-18	
II 9-07			B2	15		14	F2	A3-03	
9-07		I	A3	18	3	12	13	CI-17	
1 <u>T</u> 9-14			B3	17		Ξ	F3	A3-04	
9-14		Ŧ	Α4	04		05	T4	B1-02	
Ī			B4	03		06	F4	A3-23	
HI 22-24 202-23	A2-24		CT	24					
202-23	A02-23		C2	23					
32-19	C2-19		EI	20					1
12-20	B2-20		EZ	19	l				
			MS	22					

LØC: B2 NAME: MO9

12192		ĹŹ	C:	ΑI		NAM	E٠	T03	
SØURCE	DAISY CHAIN	T	ΥP	R IP	BIT NAME_	R ØP	ØΡ	DEST	L
A2-11	A3-06	Г	ΑĪ		8	07		PIA-07	
					-0	06		PIA-08	
A5-14		T	A2	02				P1A-28	
						04	F2	P1A-27	
		Г	A3	18		12	T3		
						13	F3		
		П	A4	17		14	T4		
					Ì	15	F4		
						08	T5		
						III.	T6		
		П	CX	22					
			CY	20					

12171		L	C:	G9		NAM	Æε	MO3	
SØURCE	DAISY	Т	IP.	R IP	BIT NAME	R ØP	ØP	DEST	L
CB3		T	ΑĪ	23		III	TI	F9-04	
P2B-22		[Ţ	BL	24	3	12	드	TERM	
P2B-37		ļΤ	CI	01	,				
D2-16		II	DI	02		L			
C84		ΙŦ	A2	03		07	T2	F9-16	
P2B-24		ĮΤ	B2	04		08	F2	TERM	
P2B-39		T	C2	05	7			·	
D2-18		II	DZ	06					
C109		ĪĪ	Α3	15				F9-24	
P2B-26		T	B3	16	5	13	F3	TERM	
P2B-32		Ţ	C3	17	,				
D2-20		I	D3	18					
G8-20	G10-20			20					_
GB-19	GIO-19		EO	19					
			IΗ	22					

12171		LØ	IC:	FIC		NAL	Æε	MO7	
SØURCE	DAISY CHAIN	T	ΙP	R IP	BIT NAME	R pp	ØP.	DEST	L.
F3-16		T	ΑI	15		14	TI	A2-04	
GIO-14		T	BI	16	6	13	FI	TP24	П
C88		Ŧ	CI	17	0	Γ.			
P2B-04		T	DΙ	18					
F3-15		ŢΤ	A2	23				A2-16	Г
G10-11		T	B2	24	7	12	F2	TP23	
CISI		T	CZ	OI.	'				
P2B-02		ĪΤ	D2	02					
E2-08		T	A3	03		07	T3	A2-18	Г
G10-07		TŦ	B3	04	8	08	F3	TP22	
C117		JΤ	C3	05		\Box			
P1B-40		T	D3	06		1			
G14-13	F9-20	Ľ	EL	20					
G13-13	F9-19	T	EO	19					
		Γ	ĬΗ	22					

12155		IC:	AZ		NAL	E٤	MOA	
SØURCE CHA	SY T	ΙP	R IP	BIT NAME	R ØP	ØP	DEST	Ī
F9-11	(T	AT	ŌΖ	5	00	TI	BI-OI	T
HI		BI	OI	l. ³	07	FI	A3-01	Т
F10-14	Ť	AZ	04	6	05	ΤŹ	BI-18	
HI		B2	03		06	F2	A3-02	T
FIO-II		A3	16	7	13	T3	BI-I7	Т
HI		B3	15		14	F3	A3-22	L
F10-07	[T	A4	ΤĒ	8	12	T4	TERM	L
HI		B4	17	_ 0	Ш	F4	AI-OI	Ι
B2-24		CI	24					
B02-23		œ	23					
A2-19 B2	-19	Εï	20					
B5-14 A2	-20	E2	19					
		MS	22					

12160		L	iC:	A3		NAN	E٠	P02	
SØURCE	DAISY	Т	ΙP	R IP	IN BIT	R ØP	ØP	DEST	L
C2-06		T	ΑI	24	0	07	TI	C13-24	
B2-07		T	A2	05		Г			
B2-14		T	A3	03	2]			
B2-11		T	A4	04	3	1			
B2-06		T	A5	23	4				
A2-07		T	AG	ō	5	1			
A2-06		T	Α7	02	6	1			
A2-14		ĪŤ	BA	22	7				
A2-01		IT	ΡĨ	8	8				

00494

LEVEL 4 BACKUP CHART SUPPLEMENTARY WIRING INFØRMATIØN MAC 4.0-02 DEVELØPMENT DIVISIØN MAC 4.0-02A The backup chart table for each ECL 100K chip is either X-section or whole-chip format. In whole-chip format, there is one element name given to the whole chip and each circuit has a uniquely named set of pins. In X-section format, each circuit on the chip receives a unique element name and the set of pin names is the same for each circuit.

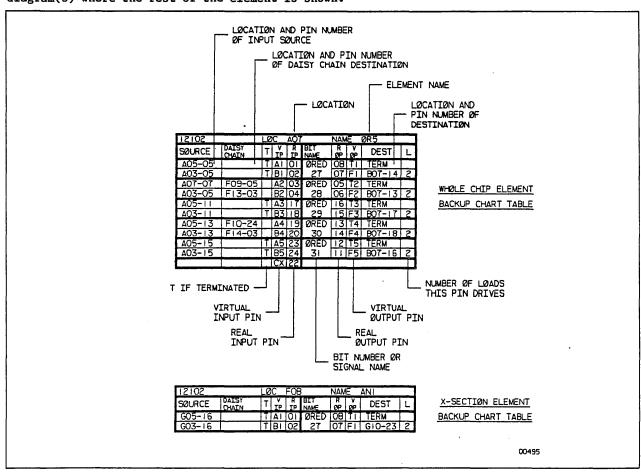
The AD112 whole chip and X-section backup chart tables example shows tables for a 12102 chip.

The whole chip backup chart table shows all pins for the entire chip. The heavy horizontal lines divide the chip into its individual sections (i.e., circuits). In this case there are five circuits with the common control at the bottom (virtual pin CX, real pin 22).

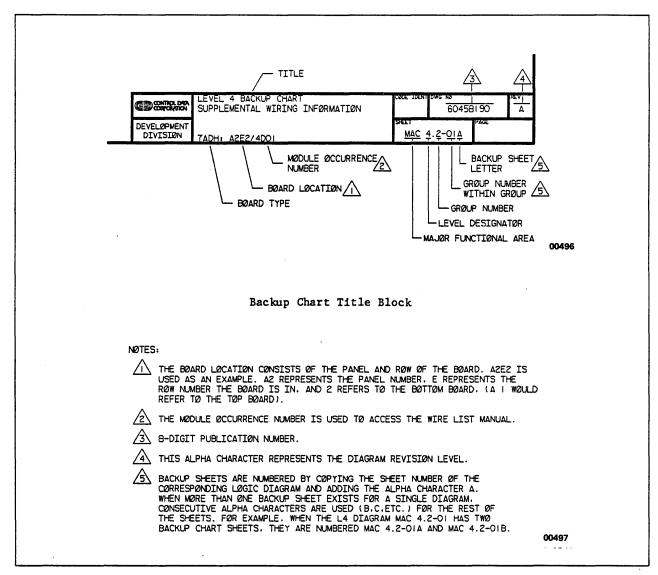
The X-section backup chart table shows the pins for any one section.

When the circuit is depicted as an X-section element and is stacked on the L4 diagram, the stack represents a stack of X-sections. Therefore, X-section element backup chart table are used. When the circuit is depicted as a whole-chip element and is stacked, the stack represents a stack of whole chips. Therefore, whole-chip element backup chart tables are used. All circuits symbols which show highwayed circuits represent whole-chip models and use whole-chip element backup charts.

When there is more than one symbol per whole chip on the L4 diagram, the element backup chart table for the entire chip is placed on the backup chart for the L4 diagram which shows the A piece. A note on that backup chart gives the L4 diagram sheet number(s) for the diagram(s) where the rest of the element is shown.



AD112 Whole Chip and X Section Backup Chart Tables



AD112 Backup Chart Title Block

AD115 LEVEL 4 BACKUP CHARTS

The model 990 level 4 backup chart example shows a L4 backup chart. L4 backup charts contain tabular information supplementary to highwayed or stacked elements on a L4 diagram. The L4 backup charts show real and virtual pin numbers, bit numbers, and element names.

All ECL 100K circuits which are depicted highwayed or stacked on auxiliary boards have individualized L4 backup charts which relate signals to pin names and real pin numbers. When the L4 backup charts represent all the elements in a stack, they are arranged from left to right or top to bottom on the sheet. The left or top element on a backup chart represents the top element in the stack (lowest bit number).

Stacked LSI circuits do not use individualized backup charts. LSI pin number charts show the relationship between pin names and real pin numbers. LSI pin number charts are located in section 2 of this manual.

The backup chart table for each ECL 100K chip is either X-section or whole-chip format. In whole-chip format, there is one element name given to the whole chip and each circuit has a uniquely named set of pins. In X-section format, each circuit on the chip receives a unique element name and the set of pin names is the same for each circuit.

The AD115 whole chip and X section backup chart tables example shows tables for a 12102 chip.

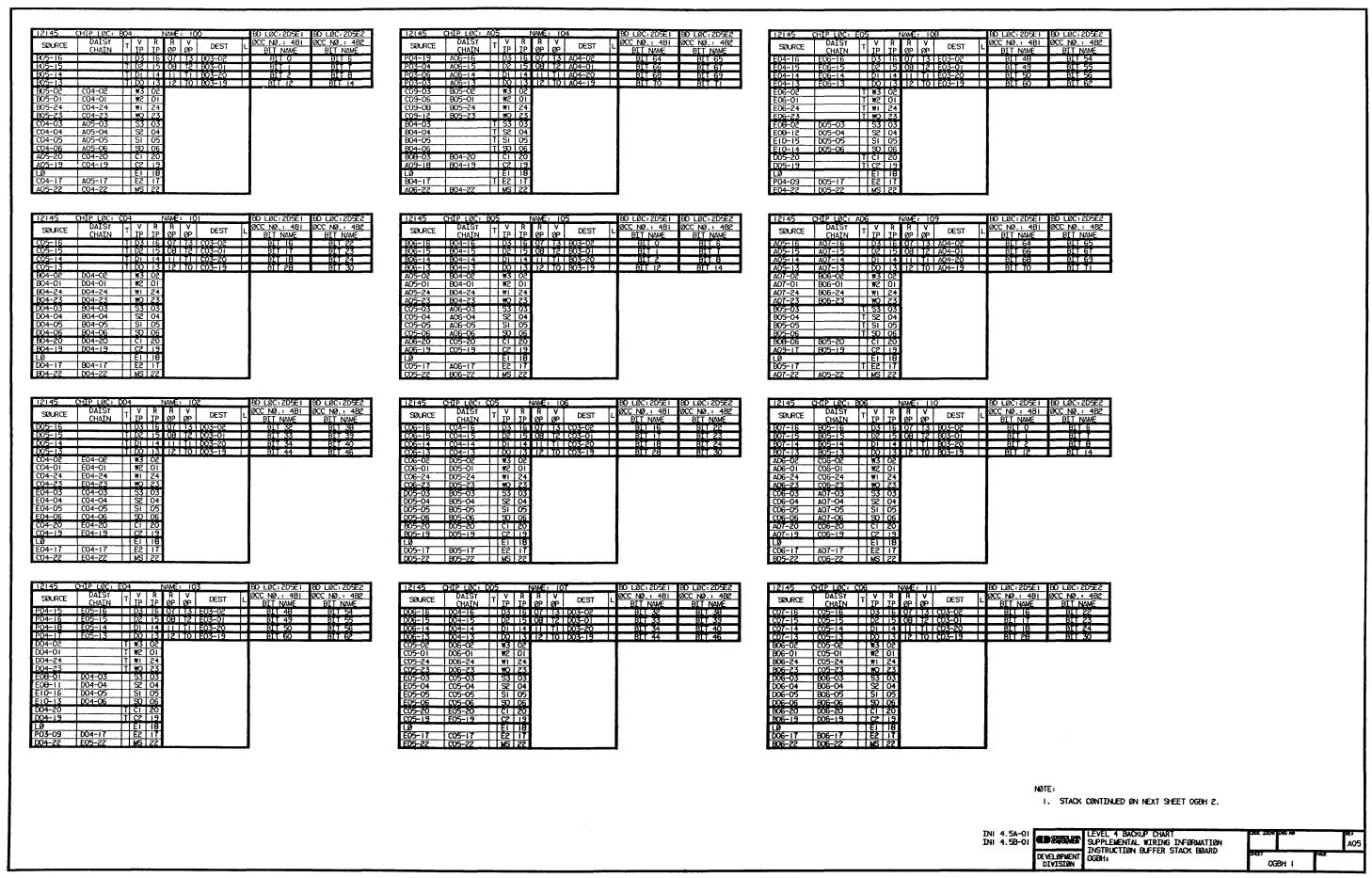
The whole-chip backup chart table shows all pins for the entire chip. The heavy horizontal lines divide the chip into its individual sections (i.e., circuits). In this case there are five circuits with the common control at the bottom (virtual pin CX, real pin 22).

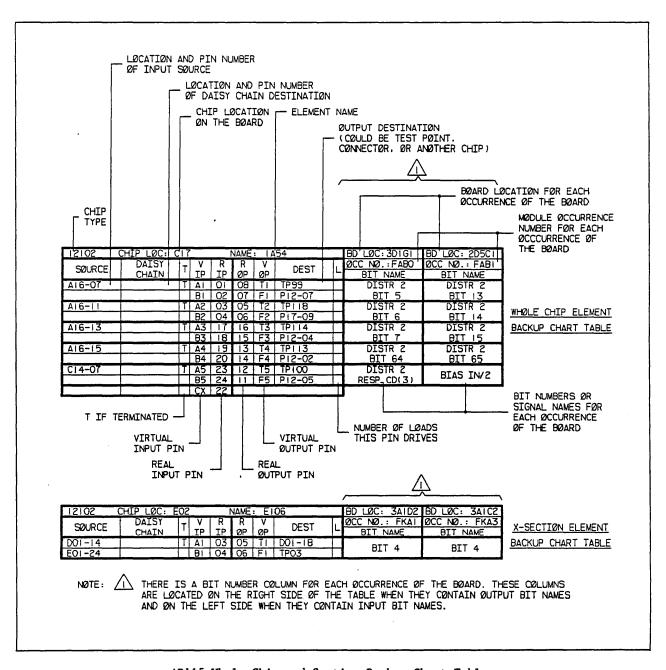
The X-section backup chart table shows the pins for any one section.

When the circuit is depicted as an X-section element and is stacked on the L4 diagram, the stack represents a stack of X-sections. Therefore, X-section element backup chart tables are used. When the circuit is depicted as a whole-chip element and is stacked, the stack represents a stack of whole chips. Therefore, whole-chip element backup chart tables are used. All circuits symbols which show highwayed circuits represent whole-chip models and use whole-chip element backup charts.

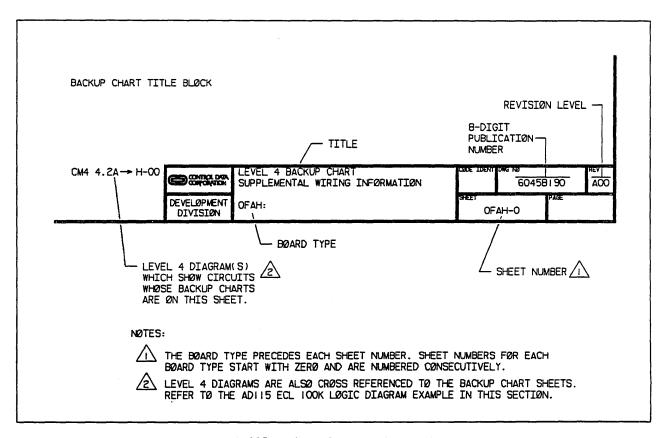
The AD115 backup chart title block example shows the information located in the title block and L4 diagram cross reference information.

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AD115 Whole Chip and Section Backup Chart Tables



AD115 Backup Chart Title Block

AD112 LEVEL 4 CONNECTOR CHARTS

The following examples depict a AD112 L4 connector chart for an ECL 100K auxiliary board and a zero insertion force (ZIF) board, respectively. The formats used for both types are similar.

Connector charts correlate real connector pin numbers with the module pin names on the L4 diagrams. There is an entry on the connector chart for each signal entering or leaving an ECL 100K board.

The AD112 Connector Chart Title Block example shows the information located in the title $block_{\bullet}$

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E	BIT NAME	I/Ø	PAGE	VIRTUAL PIN	REAL PIN
VIRTUAL	REAL				
HIGHO	NU	I	00	VOI	POI-19
HIGHI PFSØ BIT O	NU SUE		├┼╴	V02 V03	P02-15
PFSØ BIT I	SCE	+		V03	PO2-26
PFSØ BIT 2	PFSAC BIT 56	++-	-	V05	PO2-18
PFSØ BIT 3	PFSAC BIT 57			V06	POI-26
PFSØ BIT 4	PFSAC BIT 58			707	P03-24
PFSØ BIT 5	PFSAC BIT 59		$\sqcup \bot$	V08	P03-19
PFSØ BIT 6 PFSØ BIT 7	PESAC BIT 60		-	V09	P02-17
PFSØ BIT 7 PFSØ BIT B	PFSAC BIT 61 PFSAC BIT 8		⊬	VIO	P03-7 P04-24
PFSØ BIT 9	PFSAC BIT 9	++-	╁┼╴	V12	PO3-15
PFSØ BIT 10	PFSAC BIT 10	++-	-	VI3	PO4-15
PFSØ BIT II	PFSAC BIT II			VI4	P04-5
PFSØ BIT 12	PFSAC BIT 12			V15	PO4-19
PFSØ BIT 13	PFSAC BIT 13			V16	P05-22
PFSØ BIT 14	PFSAC BIT 14			VI7	P05-5
PFSØ BIT 15 PFSØ BIT 16	PFSAC BIT 15		 	V18	P05-20
PFSØ BIT 16 PFSØ BIT 17	PFSAC BIT 16 PFSAC BIT 17	+	╂╼┼┈	V20	P06-19 P06-6
PFSØ BIT 18	PFSAC BIT 1B	1-1-	┝┼	V20 V21	P06-26
PFSØ BIT 19	PFSAC BIT 19	+		V22	P06-5
PFSØ BIT 20	PFSAC BIT 20			V23	P06-2
PFSØ BIT 21	PFSAC BIT 21			V24	P06-7
PFSØ BIT 22	PFSAC BIT 22	\perp		V25	P07-26
PFSØ BIT 23	PFSAC BIT 23	+	$\vdash \vdash$	V26	P07-21
PFSØ BIT 24 PFSØ BIT 25	PFSAC BIT 24 PFSAC BIT 25		├┼	V27	P07-24 P07-18
PFSØ BIT 26	PFSAC BIT 25 PFSAC BIT 26	╂╌┼╌		V28 V29	POB-20
PFSØ BIT 27	PFSAC BIT 27	++	╁┼	V30	P07-19
PFSØ BIT 28	PFSAC BIT 28	1		V31	P08-22
PFSØ BIT 29	PFSAC BIT 29			V32	P08-21
PFSØ BIT 30	PFSAC BIT 30	$\bot \bot$		V33	PO8-26
PFSØ BIT 31	PFSAC BIT 31		$\vdash \vdash$	V34	P01-2
PFSØ BIT 32 PFSØ BIT 33	PFSAC BIT 32 PFSAC BIT 33			V35 V36	PO8-24 PO2-22
PFSØ BIT 34	PFSAC BIT 34	- - -		V36 V37	PO1-21
PFSØ BIT 35	PFSAC BIT 35	++	\vdash	V38	P02-25
PFSØ BIT 35 PFSØ BIT 36	PFSAC BIT 2	++-	\vdash	V39	POI-25
PESØ BIT 37	PFSAC BIT 3	T =		V40	PO3-22
PFSØ BIT 38	PFSAC BIT O	\perp		V41	P03-25
PFSØ BIT 39	PFSAC BIT I		<u> </u>	V42	P03-26
PFSØ BIT 40 PFSØ BIT 41	PFSAC BIT 40 PFSAC BIT 41		 	V43 V44	PO3-18
PFSØ BIT 41 PFSØ BIT 42	PFSAC BIT 41 PFSAC BIT 42	╂═╂╌		V44 V45	PO4-26 PO3-5
PFSØ BIT 43	PFSAC BIT 43	++	 	V46	P02-5
PFSØ BIT 44	PFSALN BIT 40	++		V47	P04-20
PFSØ BIT 45	PFSAC BIT 45			V48	P04-17
PFSØ BIT 46	PFSAC BIT 46			V49	P05-25
PFSØ BIT 47	PFSAC BIT 36	11	$\sqcup \sqcup$	V50	P05-21
PFSØ BIT 48	PESAC BIT 6	++	$\vdash \vdash$	V51	PO5-19
PFSØ BIT 49 PFSØ BIT 50	PFSAC BIT 7 PFSAC BIT 37	1-1-		V52 V53	P06-24 P06-8
PFSØ BIT 50	PFSAC BIT 37 PFSAC BIT 38	+-+	\vdash	V53 V54	P06-15
PFSØ BIT 52	PFSAC BIT 39	1	$\vdash\vdash$	V55	P06-3
PFSØ BIT 53	PFSALN BIT 41	\top		V56	P06-1
PFSØ BIT 54	PFSBDP BIT 26			V57	P06-4
PFSØ BIT 55	PFSBDP BIT 23	\perp		V58	P07-25
PFSØ BIT 56	PFSBDP BIT 6	4-4-	$\vdash \vdash$	V59	PO7-20
PFSØ BIT 57 PFSØ BIT 58	PESBOR BIT 7			V60	PO7-22
PFSØ BIT 58 PFSØ BIT 59	PFSBDP BIT B PFSBDP BIT 18	+-		V61 V62	P07-17 P07-16
PFSØ BIT 60	PFSBDP BIT 10	1-1-	\vdash	V63	P07-15
PFSØ BIT 61	PFSBDP BIT 17	1		V64	P08-25
PFSØ BIT 62	PFSBDP BIT 16	1	-	V65	PO8-18
PFSOØ BIT O	SUET	Ø	8	XOI	POI~17
PFSOØ BIT I	SCE I	Ø	8	X02	PO1-7
PMØ(X)	PMØ BIT O	II.	01	V66	P13-4

I	BIT NAME	I/Ø	PAGE	VIRTUAL PIN	REAL PIN
VIRTUAL	REAL			75-	
ZERØ	ZERØI	- Ø	01	X03	P13-5 P12-6
PFSI BIT O PFSI BIT I	PFSBDP BIT 5 PFSBDP BIT II	I	01	V69	P10-3
PFSI BIT I PFSI BIT Z	PESBDP BIT 21		\vdash	V70	PII-15
PFSI BIT 3	PFSBDP BIT 22 PFSBDP BIT 14		\Box	V71	P10-1
PFSI BIT 4	PFSBDP BIT 14			V72	P11-7
PFSI BIT 5	PESBDP BIT 15			V73	P12-8
PFSI_BIT_6	PFSBDP BIT 12		ш	V74	P11-9
PFSI BIT 7	PFSBDP BIT 13		<u> </u>	V75	P12-3
PFSI BIT 8	PFSBDP BIT 20		\vdash	V76	P13-16
PFSI BIT 9	PFSBDP BIT 24			V77	P12-4 P13-7
PFSI BIT 10 PFSI BIT 11	PFSBDP BIT 19 PFSBDP BIT 25		┡	V78 V79	P13-6
PFSI_BIT_II PFSI_BIT_I2	PFSBDP BIT O	++	 -	V80	P13-10
PFSI BIT 13	PFSBDP BIT I	- - -	\vdash	VBI	P13-2
PFSI BIT 14	PFSBDP BIT_2_		 - - 	V82	P13-2 P13-8
PFSI BIT 15	PFSBDP BIT 3		-	V83	P13-9
ONES	BIASI	I	01	V84	P12-7
REGSEL O	REGSEL BIT O	I	02	V85	PO1-20
REGSEL I	REGSEL BIT I	I	02	V86_	PO1-22
WT	WT	_ _ <u>I</u> _	02	V87	POI-24
CLRERR	CLRERR	- - <u>Ī</u> -	02	V88	POI-16
MBC BIT O	MBC BIT 0 MBC BIT 1 MBC BIT 2	- - <u>‡</u> -	02	V89	P05-6
MBC BIT I	MBC BIT 1	 I	02	V90 V91	P05-3 P05-2
WBC BIT 2 RGSELØ BIT O	RGSELØ BIT O	T p	02	X04	P02-24
RGSELØ BIT I	RGSELØ BIT I	ø	02	X05	POI-18
WTØ	WTØ	T Ø	02	X06	PO2-20
CLRERØ	CLRERØ	Ø	02	X07	P02-7
MBCØ BIT O	MBCØ BIT O	Ø	SO	XO8	P05-8
MBCØ BIT I	MBCØ BIT I	Ø	02	X09	P04-18
MBCØ BIT 2	MBCØ BIT 2	Ø	02	XIO	P04-22
MDØ BIT O	NMACD6 BIT O	Ī	03	V92	P09-26
MDØ BIT I	NMACD6 BIT I	Î	03	V93	P09-25
MDØ BIT 2	NMACD6 BIT 2	<u>-</u>	03	V94 V95	P09-19
MDØ BIT 3 MDØ BIT 4	NMACD6 BIT 3	$\frac{1}{1}$	03	V96	P09-17 P09-21
MDØ BIT 5	NMACD6 BIT 5	─ †	03	V97	P09-22
MDØ BIT 6	NMACDG BIT 6	ΤÎ	03	V98	P10-26
MDØ BIT 7	NMACD6 BIT 7	Ī	03	V99	P10-25
MDØ BIT 8	NMACD6 BIT B	Ī	03	WOI	PI0-19
WDI BITO	MDI BITO	Ø	03	XII	P12-17
WDI BIT I	MDI BIT I	Ø	03	XIZ	P12-15
MDI_BIT2	MDI BIT 2	Ø	03	XI3	PII-4
MDI BIT 3	MDI BIT 3	Ø	03	XI4	PII-6
MDI BIT 4	MDI BIT 4	Ø	03	X15	P11-8
MDI BIT 5	MDI BIT 5	Ø	03	XI6	P11-17 P12-16
MDI BIT 6 MDI BIT 7	MDI BIT 6	l ø	03	XI7	P12-16
MDI BIT 8	MDI BIT B	ø	03	XI9	P11-2
GATE	GATE BIT O	Ϊ́	03	WOZ	P10-21
BDSEL.	BDSEL BIT O	ΗÌ	03	WO3	P10-20
ØR	PFSØR BIT O	Ø	03	X20	P09-9
CLØCKB	CLØCKB (450)	I	03	WO4	P10-4
CLØCKA	CLØCKA (451)	I	03	W05	P09-15
DEC BIT O	DEC BIT 32	Ø	03	X21	P09-24
DEC BIT I	DEC BIT 33	+	\sqcup	X22	P08-1
DEC BIT 2	DEC BIT 34	+	$\vdash\vdash\vdash$	X23	PO8-17
DEC BIT 3	DEC BIT 35		H	X24	PO8-19
DEC BIT 4 DEC BIT 5	DEC BIT 36 DEC BIT 37	++	-	X25 X26	PO8-15 PO8-9
DEC BIT 6	DEC BIT 38		\vdash	X27	P09-7
DEC BIT 7	DEC BIT 39		\vdash	X28	P09-3
DEC BIT B	DEC BIT 40	+	\vdash \vdash \vdash	X29	P10-7
DEC BIT 9	DEC BIT 41	1	\Box	X30	P10-10
DEC BIT TO	DEC BIT 42			X31	P10-15
DEC BIT II	DEC BIT 43			X32	PI0-16
DEC BIT 12	DEC BIT 44	17	-	X33	P11-22
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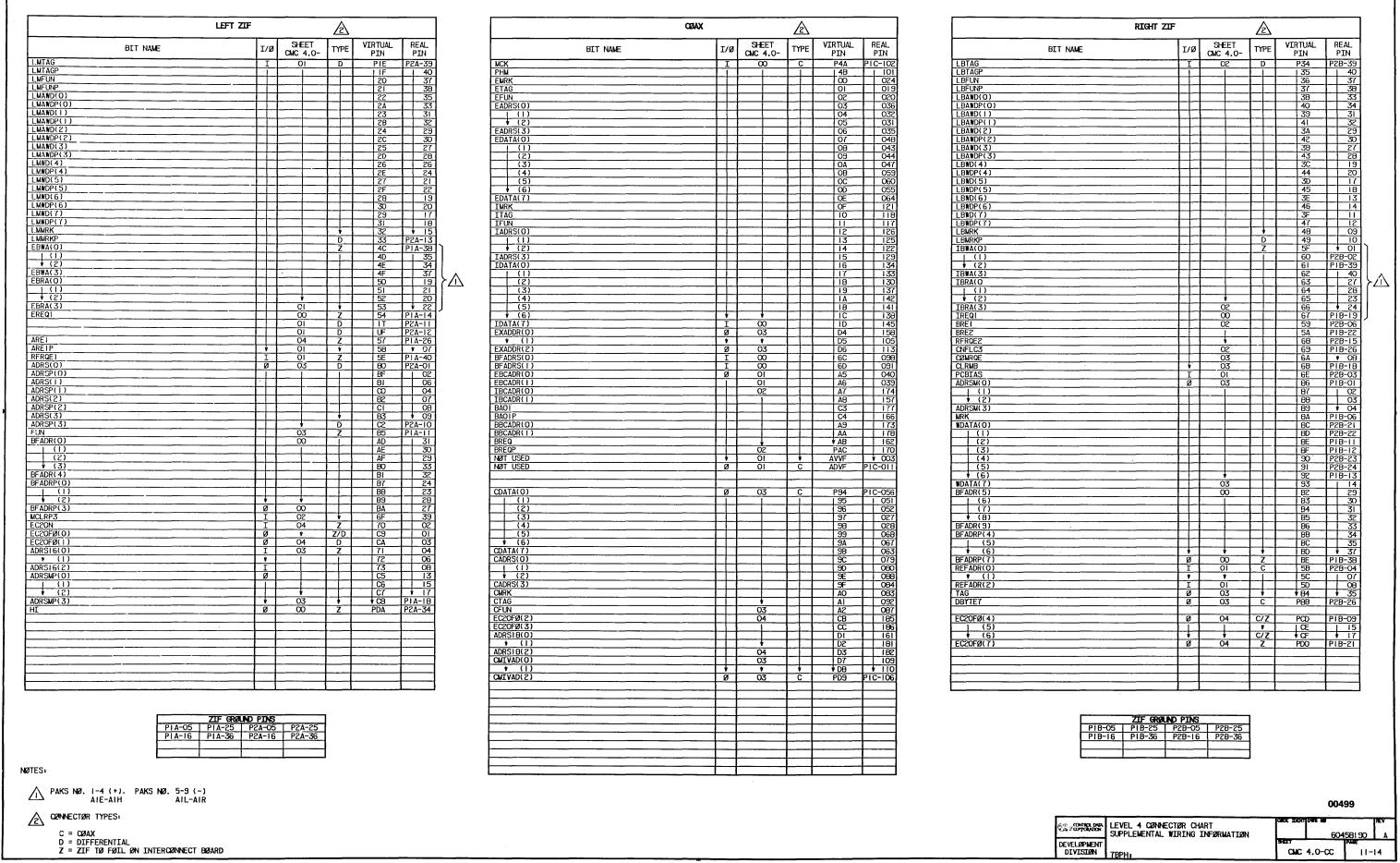
	BIT NAME	I/Ø	PAGE	VIRTUAL PIN	REAL PIN
VIRTUAL	REAL			1674	210 5
DEC BIT 13 DEC BIT 14	DEC BIT 45 DEC BIT 46	Ø	03	X34 X35	P12-5
DEC BIT 15	DEC BIT 47		 	X36	PI I-18
CLKINA	ØUTIG BIT O	Ti	04	W06	P04-9
CLKINB	ØUTI6 BIT I			WO7	P11-25
PHEO	NU			W08	P07-10
PHEI	NU			₩09	P07-9
PHE2	NU			MIO	P07-8
PHE3	NU	- 1 *	*	WII	P07-4
CLK BIT O	CLKN (29)	_ Ø	04	X37	PO1-4
CLK BIT 1	CLKN (30)	- - -	 	X38	POI-10
CLK BIT 3	CLKN (32) CLKN (33)		 -	X39 X40	PO2-10
CLK BIT 4	CLKN (16)		╌┼╌	X41	P03-6
CLK BIT 5	CLKN (18)			X42	P02-2
CLK BIT 6	CLKN (19)		 	X43	P02-3
CLK BIT 7	CLKN (22)	\neg		X44	P03-9
CLK BIT 8	CLKN (2)			X45	P05-18
CLK BIT 9	_ CLKN (3)			X46	P04-01
CLK BIT IO	CLKN (4)			X47	P04-3
CLK BIT II	CLKN (5)			X48	P05-7
CLK BIT 12	CLKN (257)	$\Box\Box$	$\Box\Box$	X49	P06-18
CLK BIT 13	CLKN (258)		$\sqcup \!\! \perp \!\! \perp$	X50	P05-4
CLK BIT 14	CLKN (259)	-	$\sqcup \sqcup$	X51	PO6-25
CLK BIT 15	CLKN (260)			X52	P06-10
CLK BIT 16	CLKN (265)	$\dashv \vdash$	 -	X53	P07-2
CLK BIT 17	CLKN (266)			X54	P07-5 P08-10
CLK BIT 18	CLKN (267) CLKN (268)		 	X55	P08-10
CLK BIT 19 CLK BIT 20	CLKN (272)		┞╼┼╼	X56 X57	PO8-4
CLK BIT 21	CLKN (274)		 	258	P09-10
CLK BIT 22	CLKN (275)		 	X59	P09-18
CLK BIT 23	CLKN (276)		 	X60	P09-4
CLK BIT 24	CLKN (2BI)		 	X61	P13-20
CLK BIT 25	CLKN (282)			X62	P12-10
CLK BIT 26	CLKN (2B3)			X63	P13-22
CLK BIT 27	CLKN (285)			X64	P13-18
CLK BIT 28	CLKN (290)			X65	P12-20
CLK BIT 29	CLKN (291)			X66	P11-16
CLK BIT 30	CLKN (292)			X67	P11-24
CLK BIT 31	CLKN (293)		\perp	X68	P12-25
CLK BIT 32	CLKN (34)		├	X69	PO1-6
CLK BIT 33	CLKN (35)	$-\!\!+\!\!\!+$		X70	POI-15
CLK BIT 34	CLKN (27)		 -	X71	PO1~5
CLK BIT 35 CLK BIT 36	CLKN (28) CLKN (23)			X12 X13	P02-9 P03-4
CLK BIT 37	CLKN (24)			X74	P02-6
CLK BIT 3B	CLKN (25)		 -	X75	P02-8
CLK BIT 39	CLKN (31)			X76	P03-10
CLK BIT 40	CLKN (10)	-		X77	P05-24
CLK BIT 41	CLKN (11)	-++		X78	P04-4
CLK BIT 42	CLKN (O)		\Box	X79	P04-6
CLK BIT 43	CLKN (284)			X80	P05-10
CLK BIT 44	CLKN (261)			X81	P06-20
CLK BIT 45	CLKN (262)	$-\Box$		X82	P05-1
CLK BIT 46	CLKN (263)		\coprod	X83	P06-21
CLK BIT 47	CLKN (264)	-++	$\sqcup \sqcup$	X84	P06-9
CLK BIT 48	CLKN (269)			X85	P07-3
CLK BIT 49	CLKN (270)		 	X86	P07-7
CLK BIT 50 CLK BIT 51	CLKN (271) CLKN (273)	++		X87	P08-16
CLK BIT 52	CLKN (277)		\vdash	X88 X89	P08-5 P08-2
CLK BIT 53	CLKN (27B)	~ 	 	X90	P09-16
CLK BIT 54	CLKN (279)	- -	H-:	X9I	P09-20
CLK BIT 55	CLKN (280)			X92	P09-6
CLK BIT 56	CLKN (286)		\vdash	X93	P13-26
			_		
CLK BIT 57	CLKN (287)	11		X94	P12-21
CLK BIT 56 CLK BIT 57 CLK BIT 58	CLKN (287) CLKN (288)	_++		X94 X95	P12-21 P13-25

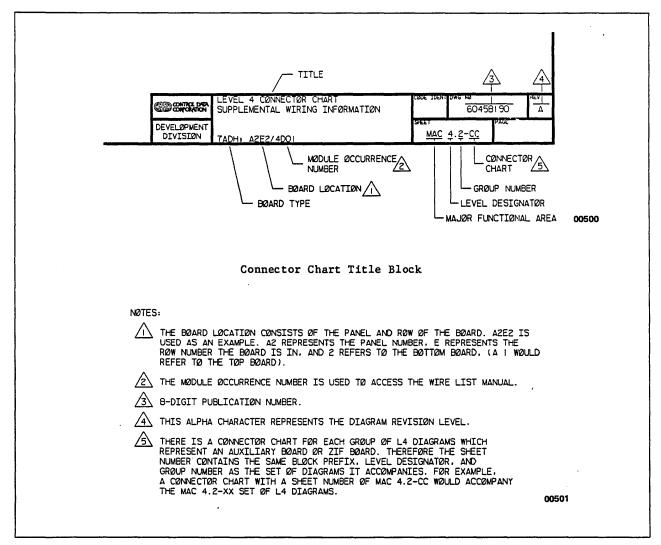
	BIT NAME	I/Ø	PAGE	VIRTUAL PIN	REAL PIN
VIRTUAL	REAL				
CLK 59	CLKN (289)	Ø	04	X96	P13-17
CLK 60	CLKN (294)			X97	P12-22
CLK 61	CLKN (295)			X98	P11-20
CLK 62	CLKN (296)			X99	P11-21
CLK 63	CLKN (297)			YOL	P12-19
CLK 64	CLKN (298)		├ -├-	Y02	P10-6
CLK 65	CLKN (299)		├ ─├─	Y03	P10-22
CLK 66	CLKN (301) CLKN (302)		 	YO4	P10-24
CLK 67	CLKN (302)		┞┈┼╼╴	Y05	
CLK 68	CLKN (303)		- 	Y06	P04-10 P04-7
CLK 69	CLKN (304)		 	Y07 Y08	P03-1
CLK 70 NCLK BIT 0	CLKN (305)		₩-	Y09	
	NCLKN (6)			YIO	POI-3
	NCLKN (15)			YII	POI-8 POI-9
	NCLKN (16)		├ 	YIZ	P02-16
NCLK BIT 3 NCLK BIT 4	NCLKN (14) NCLKN (12)		 -	YIZ	P03-8
NCLK BIT 5	NCLKN (13)		╌┼╌	Y14	P02-4
	NCLKN (0)		╀╌	Y15	P02-1
NCLK BIT 6	NCLKN (1)	-+-	 	YI6	P03-16
NCLK BIT 8	NCLKN (2)		 	Y17	P05-26
NCLK BIT 9	NCLKN (3)		 	YIB	P04-2
CLKINC	ØUT 16 BIT 10	- ' -	╂━┼╌	YI9	P04-8
NCLK II	NCLKN (5)	- p		Y20	P05-9
NCLK 12	NCLKN (256)		╌	Y21	P06-22
NCLK 13	NCLKN (257)		 - -	Y22	P05-15
NCLK 14	NCLKN (258)		 	Y23	P06-17
NCLK 15	NCLKN (259)	- - -	 	Y24	P06-16
NCLK 16	NCLKN (386)	- - -	\vdash	Y25	P07-1
CLKIND	ØUT 16 BIT 11	Ti-		Y26	P07-6
NCLK 18	NCLKN (392)	ø		Y27	P08-B
NCLK 19	NCLKN (393)	1-7-	 	Y28	P08-7
NCLK 20	NCLKN (395)	_	 	Y29	P08-3
NCLK 21	NCLKN (396)		 -	Y30	P09-1
NCLK 22	NCLKN (397)			Y31	P09-B
NCLK 23	NCLKN (398)			Y32	P09-2
NCLK 24	NCLKN (400)			Y33	P13-24
NCLK 25	NCLKN (401)	\neg		Y34	P12-18
NCLK 26	NCLKN (403)	\neg		Y35	P13-21
NCLK 27	NCLKN (405)			Y36	PI3-19
NCLK 28	NCLKN (406)		\vdash	Y31	P12-24
NCLK 29	NCLKN (407)	77		Y38	PI1-10
CLKINE	ØUT 16 BIT 12	T		Y39	P11-26
NCLK 31	NCLKN (409)	Ø		Y40	P12-26
NCLK 32	NCLKN (412)			Y41	P10-8
NCLK 33	NCLKN (413)			Y42	P10-18
NCLK 34	NCLKN (440)	\perp		Y43	P04-16
NCLK 35	NCLKN (441)	$\Box \top$		Y44	P03-3
PM BIT O	CLKPMO			Y45	P02-19
PM BIT I	CLKPMI			Y46	P05-16
PM BIT 2	CLKPM2			Y47	P03-21
PM BIT 3	CLKPM3 _	$\Box\Box$		Y48	PO4-25
PM BIT 4	CLKPM4	$\perp T$		Y49	P13-3
PM BIT 5	CLKPM5			Y50	P12-1
PM BIT 6	CLKPM6	$\perp \Gamma$		Y51	PII-I
PM BIT 7	CLKPM7_	$\Box\Box$	Ш	Y52	P10-17
PM BIT 8	CLKPMB			Y53	P02-21
PM BIT 9	CLKPM9_	$\perp \Gamma$	Ш	Y54	P05-17
PM BIT 10	CLKPMIO			Y55	P03-17
PM BIT II	CLKPMI I	$\perp \perp \perp$		Y56	PO4-21
PM BIT 12	CLKPMI2	\Box		Y57	P13-1
PM BIT 13	CLKPM13			Y58	P12-2
PM BIT 14	CLKPM14	$\perp \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$		Y59	P11-3
PM BIT 15	CLKPM15	+	•	Y60	P10-9
CLK BIT 71	CLKN (306)	Ø	04	Y61	P03-2
	GND				P09-05
	GND				P10-05
	GND				P11-05

00498

LEVEL 4 CONNECTOR CHART
SUPPLEMENTAL WIRING INFORMATION
DEVELOPMENT
DIVISION
TADHI AZEZ/4DOI

DEVELOPMENT
TADHI AZEZ/4DOI





AD112 Connector Chart Title Block

AD115 LEVEL 4 CONNECTOR CHART

The following example shows an AD115 connector chart for an ECL 100K auxiliary board.

Connector charts correlate real pin numbers with the module pin names on the L4 diagrams. There is an entry on the connector chart for each signal entering or leaving an auxiliary board. Each entry on the connector chart contains the module pin name, input or output L4 diagram sheet number, virtual pin number, and real pin number.

Entries are separated into two groups: inputs and outputs. Each group is arranged by module pin names in alphanumeric order.

1-48 60458120 B

AADCLK APRIN APRIN AAPLOR APRIN AAS-02 C28 P09-06 BTEAD(0) I 4.5-03 D04 P11-IB BTEAD(1) I 4.5-03 D05 P11-IB BTEAD(1) I 4.5-03 D06 P11-IB BTEAD(2) I 4.5-03 D06 P11-IB BTEAD(3) I 4.5-03 D07 P12-IT CLRRKI I 4.5-03 D07 P12-IT BTEAD(3) I 4.5-03 D07 P12-IT BTEAD(3) I 4.5-03 D07 P12-IT CLRRKI I 4.5-03 D07 P12-IT BTEAD(3) I 4.5-01 B02 P07-10 BAIVA I 4.5-01 B02 P02-04 IBAIVA I 4.5-01 IBAIVA I 4.5-00 A00 P07-21 IBMUXBI25) I 4.5-02 A00 P07-16 IBMUXBI26) I 4.5-00 A00 P07-17 IBMUXBI27) I 4.5-00 A00 P07-16 IBMUXBI27) I 4.5-00 A02 P07-16 IBMUXBI28) I 4.5-00 A02 P07-16 IBMUXBI28) I 4.5-01 B30 P08-21 MACPCL(1) I 4.5-01 B31 P08-24 MCA MCA I 4.5-01 B31 P08-24 MCA MCA I 4.5-01 B31 P08-28 MCA MCA I 4.5-01 B31 P08-29 MCA MCA I 4.5-01 B31 P08-20 MCA MCA I 4.5-01 B31 P08-20 MCA MCA I 4.5-01 B31 P08-01 MCA MCA I 4.5-01	MØDULE PIN NAME	I/Ø	SHEET	VIRTUAL	REAL
APRIN	AADCI K	- T	4.5-00	PIN	PIN 207-09
BYTEAD(0) I					
BYTEAD(2)	BYTEAD(O)	_ I	4.5-03		
CLRRIN		I	4.5-03	D05	PII-IT
CLRRIN			4.5-03		P11-19
ENTIBAO I 4.5-01 B02 P02-04 IBA1VA I 4.5-01 B02 P02-04 IBA1VB I 4.5-02 C02 P03-04 IBALVB I 4.5-02 C02 P03-04 IBALVB(25) I 4.5-00 A00 P07-21 IBMUXB(26) I 4.5-00 A01 P07-16 IBMUXB(27) I 4.5-00 A02 P07-16 IBMUXB(27) I 4.5-00 A03 P07-15 IBMUXB(27) I 4.5-00 A08 P07-03 MCPCL(0) I 4.5-01 B30 P08-21 MCPCL(0) I 4.5-01 B31 P08-21 MCA I 4.5-01 B07 P05-06 MCB I 4.5-01 B09 P06-07 MCMDTA(1) I 4.5-01 B10 P06-16 MCMDTA(2) I 4.5-01 B10 P06-16 MCMDTA(2) I 4.5-01 B10 P06-16 MCMDTA(3) I 4.5-01 B10 P06-16 MCMDTA(4) I 4.5-01 B12 P06-10 MCMDTA(5) I 4.5-01 B12 P06-10 MCMDTA(6) I 4.5-01 B15 P06-03 MCMDTA(8) I 4.5-01 B16 P05-10 MCMDTA(8) I 4.5-01 B16 P05-10 MCMDTA(8) I 4.5-01 B16 P05-10 MCMDTA(1) I 4.5-01 B16 P06-03 MCMDTA(1) I 4.5-01 B17 P05-05 MCMDTA(1) I 4.5-01 B18 P04-03 MCMDTA(1) I 4.5-01 B18 P04-04 MCMDTA(1) I 4.5-01 B22 P04-18 MCMDTA(1) I 4.5-02 C11 P09-16 MCMDTB(1) I 4.5-02 C11 P09-17 MCMDTB(1) I 4.5-02 C11 P09-18 MCMDTB(1) I 4.5-02 C11 P09-19 MCMDTB(1) I 4.5-02 C11 P09-19 MCMDTB(1) I 4.5-02 C11 P09-19 MCMDTB(1) I 4.5-02 C22 P08-03 MCMDTB(1) I 4.5			4.5-03		P12-17
IBAIVA			4.5-00		
IBALVB(25)					
IBMUXB(26)			4.5-01		
IBMUXBR 27		+-	4.5-00		P07-21
IBMUXB(2T)			4.5-00		P07-17
IBMURBLOR I		Ī	4.5-00		P07-16
MACPCL(1)		I	4.5-00		
MACPCL(0) MACPCL(1) I 4.5-01 B30 POB-21 MCA I 4.5-01 B07 PO5-06 MCB I 4.5-01 B07 PO5-06 MCB I 4.5-01 B07 PO8-07 MEMDTA(0) I 4.5-01 B09 PO5-08 MEMDTA(1) I 4.5-01 B09 PO5-08 MEMDTA(2) I 4.5-01 B10 PO6-16 MEMDTA(2) I 4.5-01 B11 PO5-06 MEMDTA(3) I 4.5-01 B10 PO6-16 MEMDTA(3) I 4.5-01 B11 PO5-06 MEMDTA(3) I 4.5-01 B11 PO5-06 MEMDTA(3) I 4.5-01 B11 PO6-10 MEMDTA(4) I 4.5-01 B12 PO6-10 MEMDTA(5) I 4.5-01 B13 PO6-10 MEMDTA(6) I 4.5-01 B14 PO6-09 MEMDTA(7) I 4.5-01 B15 PO6-09 MEMDTA(8) I 4.5-01 B16 PO5-10 MEMDTA(8) I 4.5-01 B17 PO5-05 MEMDTA(10) I 4.5-01 B18 PO4-03 MEMDTA(11) I 4.5-01 B19 PO4-04 MEMDTA(12) I 4.5-01 B20 PO4-15 MEMDTA(13) I 4.5-01 B20 PO4-15 MEMDTA(14) I 4.5-01 B22 PO4-18 MEMDTA(15) I 4.5-01 B22 PO4-18 MEMDTA(15) I 4.5-01 B24 PO4-13 MEMDTA(16) I 4.5-01 B27 PO4-16 MEMDTA(17) MEMDTA(16) I 4.5-01 B28 PO4-17 MEMDTA(16) I 4.5-01 B29 PO4-18 MEMDTA(16) I 4.5-01 B20 PO4-16 MEMDTA(17) MEMDTA(18) I 4.5-01 B21 PO4-16 MEMDTA(19) MEMDTA(19) I 4.5-01 B22 PO4-18 MEMDTA(19) MEMDTA(19) I 4.5-01 B27 PO3-04 MEMDTA(19) I 4.5-01 B27 PO3-04 MEMDTA(19) I 4.5-02 C09 PO9-20 MEMDTB(1) MEMDTB(1		I	. 1. 7 00	BOA	P07-09
MCA MCB					P08-21
MCB I 4.5-02 COT POB-IT MEMDTA(0) I 4.5-01 BOB PO6-07 MEMDTA(1) I 4.5-01 BOB PO6-07 MEMDTA(1) I 4.5-01 BIO PO6-16 MEMDTA(2) I 4.5-01 BIO PO6-16 MEMDTA(3) I 4.5-01 BIO PO6-16 MEMDTA(5) I 4.5-01 BIO PO6-16 MEMDTA(5) I 4.5-01 BIO PO6-10 MEMDTA(6) I 4.5-01 BIS PO6-09 MEMDTA(7) I 4.5-01 BIS PO6-09 MEMDTA(7) I 4.5-01 BIS PO6-09 MEMDTA(7) I 4.5-01 BIS PO6-09 MEMDTA(1) I 4.5-01 BIF PO5-05 MEMDTA(1) I 4.5-01 BIF PO5-05 MEMDTA(1) I 4.5-01 BIF PO6-08 MEMDTA(1) I 4.5-01 BIF PO6-08 MEMDTA(1) I 4.5-01 BIF PO6-09 MEMDTA(1) I 4.5-01 BIF PO6-05 MEMDTA(1) I 4.5-01 BIF PO6-05 MEMDTA(1) I 4.5-01 BIF PO6-05 MEMDTA(13) I 4.5-01 BIF PO6-05 MEMDTA(13) I 4.5-01 BIF PO6-16 MEMDTA(13) I 4.5-01 BIF PO6-16 MEMDTA(14) I 4.5-01 BIF PO6-16 MEMDTA(14) I 4.5-01 BIF PO6-16 MEMDTA(16) I 4.5-01 BIF PO6-16 MEMDTA(16) I 4.5-01 BIF PO6-16 MEMDTA(16) I 4.5-01 BIF PO6-16 MEMDTA(19) I 4.5-01 BIF PO6-09 MEMDTA(19) I 4.5-01 BIF PO6-09 MEMDTA(19) I 4.5-02 CO9 PO9-20 MEMDTB(1) I 4.5-02 CO1 PO9-17 MEMDTB(1) I 4.5-02 CO1 PO9-18 MEMDTB(1) I 4.5-02 CO1 PO9-18 MEMDTB(1) I 4.5-02 CO1 PO9-19 MEMDTB(1) I 4.5-02 CO1 PO9-19 MEMDTB(1) I 4.5-02 CO1 PO9-09 MEMDTB(1) I 4.5-02 CO2 PO9					P08-24
MEMDTA(1)					
MEMDTA(1) MEMDTA(2) II 4.5-01 MEMDTA(3) II 4.5-01 MIMDTA(3) II 4.5-01 MIMDTA(4) MEMDTA(5) II 4.5-01 MIMDTA(5) II 4.5-01 MIMDTA(5) II 4.5-01 MIMDTA(5) II 4.5-01 MIMDTA(6) MIMDTA(6) MIMDTA(7) II 4.5-01 MIMDTA(7) II 4.5-01 MIMDTA(8) II 4.5-01 MIMDTA(8) MIMDTA(8) II 4.5-01 MIMDTA(8) MIMDTA(8) II 4.5-01 MIMDTA(9) MIMDTA(10) MIMDTA(11) MIMDTA(11) MIMDTA(12) MIMDTA(12) MIMDTA(13) MIMDTA(14) MIMDTA(13) MIMDTA(14) MIMDTA(15) MIMDTA(15) MIMDTA(15) MIMDTA(16) MIMDTA(17) MIMDTA(18) MIMDTA(18) MIMDTA(18) MIMDTA(18) MIMDTA(18) MIMDTA(18) MIMDTA(19) M					
MEMDTA(2) MEMDTA(3) I 4,5-01 MEMDTA(4) MEMDTA(4) I 4,5-01 MEMDTA(5) MEMDTA(6) I 4,5-01 MEMDTA(6) MEMDTA(6) MEMDTA(7) MEMDTA(7) MEMDTA(7) MEMDTA(8) MEMDTA(8) MEMDTA(8) MEMDTA(1) MEMDTA(13) MEMDTA(13) MEMDTA(13) MEMDTA(14) MEMDTA(15) MEMDTA(16) MEMDTA(16) MEMDTA(16) MEMDTA(16) MEMDTA(17) MEMDTA(18) MEMDTA(19) MEMDTA(10) MEMDTA(10) MEMDTA(10)			4 5-01		
MEMDTA(3)			4.5-01		
MEMDTA(4)			4.5-01		
MEMDTA(5)			4.5-01		
MEMDTA(6) MEMDTA(7) MEMDTA(8) MEMDTA(8) MEMDTA(8) MEMDTA(8) MEMDTA(9) MEMDTA(10) MEMDTA(10) MEMDTA(11) MEMDTA(11) MEMDTA(11) MEMDTA(11) MEMDTA(12) MEMDTA(12) MEMDTA(12) MEMDTA(12) MEMDTA(13) MEMDTA(13) MEMDTA(14) MEMDTA(15) MEMDTA(14) MEMDTA(15) MEMDTA(15) MEMDTA(15) MEMDTA(16) MEMDTA(16) MEMDTA(17) MEMDTA(17) MEMDTA(18) MEMDTA(18) MEMDTA(19) MEMDTA(11) MEMDTA(12) MEMDTA(13) MEMDTA(13) MEMDTA(13) MEMDTA(14) MEMDTA(15) MEMDTA(15) MEMDTA(15) MEMDTA(16) MEMDTA(16) MEMDTA(17) MEMDTA(18) MEMDTA(19) M	MEMDTA(5)	I	4,5-01		
MEMDTA(17) MEMDTA(8) I 4.5-01 B16 PO5-10 MEMDTA(9) I 4.5-01 B17 PO5-05 MEMDTA(10) I 4.5-01 B18 PO4-03 MEMDTA(11) I 4.5-01 B19 PO4-04 MEMDTA(11) MEMDTA(12) MEMDTA(12) MEMDTA(13) I 4.5-01 B20 PO4-15 MEMDTA(13) I 4.5-01 B20 PO4-15 MEMDTA(14) I 4.5-01 B22 PO4-18 MEMDTA(14) MEMDTA(15) I 4.5-01 B22 PO4-18 MEMDTA(16) MEMDTA(16) MEMDTA(17) MEMDTA(16) MEMDTA(17) MEMDTA(16) MEMDTA(17) MEMDTA(18) I 4.5-01 B25 PO3-06 MEMDTA(19) MEMDTA(19) MEMDTA(19) MEMDTB(0) MEMDTB(0) MEMDTB(0) MEMDTB(1) MEMDTB(1)	MEMDTA(6)		4.5-01	BJ4	P06-09
MEMDTA(19)					
MEMDTA(11)					
MEMDTA(11)			4.5-01		
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MEMDTA(13)			4.5-01		
MEMDTA(14)			4.5-01		
MEMDTA(15)		Ĩ	4.5-01		
MEMDTA(16)		I	4,5-01		
MEMDTA(18)	MEMDTA(16)	I	4.5-01		P04-19
MEMDTA(19)					
MEMDTB(Q)					
MEMDTB(1)		<u>+</u>			
MEMDTB(2)		- -			
MEMDTB(3)			4.5-02		
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MEMDTB(5)			4.5-02		P09-22
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MEMDTB(15)					
MEMDTB(16) I 4.5-02 C24 POB-10 MEMDTB(17) I 4.5-02 C25 POB-09 MEMDTB(18) I 4.5-02 C26 POB-16 MEMDTB(19) I 4.5-02 C27 POB-15 MUXS_A(0) I 4.5-01 B00 P0Z-03 MUXS_B(0) I 4.5-02 C00 P11-15 MUXS_B(0) I 4.5-02 C00 P11-15 MUXS_B(1) I 4.5-02 C01 P11-10 MUXS_B(1) I 4.5-02 C01 P11-10 MUXS_B(1) I 4.5-02 A19 P0T-03 RDCLK I 4.5-00 A04 P0T-04 RDCLK I 4.5-01 B03 P03-09 RDCLK I 4.5-01 B03 P03-09					
MEMDTB(18) I 4.5-02 C26 PO8-16 MEMDTB(19) I 4.5-02 C27 PO8-16 MUXSLA(0) I 4.5-01 B00 PO2-03 MUXSLA(1) I 4.5-01 B01 PO2-05 MUXSLB(0) I 4.5-02 C00 P11-15 MUXSLB(1) I 4.5-02 C01 P11-10 NADDCK I 4.5-00 A06 POT-OT NBDCLK I 4.5-00 A19 POT-03 RDCLK I 4.5-00 A04 POT-04 SETSLA(0) I 4.5-01 B03 P03-09	MEMDTB(16)		4.5-02		P08-10
MEMDTB(19) I 4.5-02 C2T POB-15 MUXS_A(0) T 4.5-01 BOO POZ-03 MUXS_A(1) I 4.5-01 BOO POZ-05 MUXS_B(0) I 4.5-02 COO P11-15 MUXS_B(1) I 4.5-02 COO P11-15 MUXS_B(1) I 4.5-00 A06 POT-0T NBOLK I 4.5-00 A19 POT-03 NBOLK I 4.5-00 A04 POT-04 RDCLK I 4.5-00 A04 POT-04 RDCLK I 4.5-00 A04 POT-05 RDCLK I 4.5-00 A04 POT-06 RDCLK I 4.5-00 BO3 PO3-09 PO3			4.5-02		
MUXSLA(1) I 4.5-01 B01 P02-05 MUXSLB(0) I 4.5-02 C00 P11-15 MUXSLB(1) I 4.5-02 C01 P11-16 NADDCK I 4.5-00 A06 P07-07 NBDLK I 4.5-00 A04 P07-04 RDCLK I 4.5-00 A04 P07-04 SETSLA(0) I 4.5-01 B03 P03-09			4.5-02		
MUXSLA(1) I 4.5-01 B01 P02-05 MUXSLB(0) I 4.5-02 C00 P11-15 MUXSLB(1) I 4.5-02 C01 P11-16 NADDCK I 4.5-00 A06 P07-07 NBDLK I 4.5-00 A04 P07-04 RDCLK I 4.5-00 A04 P07-04 SETSLA(0) I 4.5-01 B03 P03-09		- f	4.5-02		
MUXS_B(0)		┝╪┈┤	4.5-01		POZ-03
MUXS_B(1) I					
NADOCK I 4.5-00 A06 POT-OT NRDCLK I 4.5-00 A19 POT-O3 RDCLK I 4.5-00 A04 POT-O4 SETSLA(0) I 4.5-01 B03 PO3-O9	MUXSLB(1)		4.5-02		
NBOLK I 4.5-00 A19 POT-03 RDCLK I 4.5-00 A04 POT-04 SETSLA(0) I 4.5-01 B03 PO3-09					
RDCLK I 4.5-00 A04 P07-04 SETSLA(0) I 4.5-01 B03 P03-09	NRDCLK	ΞĪ	4.5-00		
	RDCLK		4.5-00	A04	P07-04
SFIS(A(1) T 4.5-0 R04 D04-09					
32.33.7.7 L 4 T.3-01 D07 F04-03	SETSLA(I)	I	4.5-01	B04	P04-09

			VGDT-A	55
MODULE PIN NAME	I/Ø	SHEET	VIRTUAL PIN	REAL PIN
SETSLA(2)	I	4.5-01	B05_	P04-10
SETSLA(3)	I_	4.5-01	B06	P05-19
SETSLB(0)	I T	4.5-02 4.5-02	CO3 CO4	P08-19 P09-21
SETSLB(2)	Ť	4.5-02	C05	P10-05
SETSLB(3)	Ī	4.5-02	C06	P11-09
SRCLK	Ī	4.5-00	A09_	P07-05
WRTADO(O)	I	4.5-00 4.5-00	All	P07-19 P07-1B
WRTADD(1)		4.5-00	AI2 AI3	P07-22
WRTADD(3)	Ī	4.5-00	AI4	P07-20
WRTEN(O)	I	4.5-00	AI5	P06-04
WRTEN(I)	I_	4.5-00	A16	P06-03
WRTEN(2)	Ţ	4.5-00 4.5-00	TIA BIA	P06-06
WRTEN(3)	-	4.5-00	AIO	P06-05
AØRØUT	Ø	4.5-02	C50	P11-04
ERRØR(O)	Ø	4.5-02	C52	P10-08
ERRØR(I)	Ø	4.5-02	C53	P10-20
ERROR(2)	8	4.5-02	C54 C55	P10-15
ERRØR(3) IBAIVL(0)	Ø	4.5-02 4.5-01	B50	P10-19 P03-24
IBAIVL(1)	Ø	4.5-02	C51	P11-03
MACMUX(O)	ø	4.5-01	851	P05-07
MACMUX(I)	Ø	4,5-01	B52	P05-03
MACMUX(2)	Ø	4.5-01	B53	P05-09
MACMUX(3)	Ø	4.5-01	B54	P08-22
MACMUX(4) MACMUX(5)	Ø	4.5-01 4.5-01	B55_ B56	P08-20 P08-18
MACMUX(6)	Ø	4.5-01	B57	P08-08
MACMUX(7)	ő	4.5-01 4.5-01	B58	P08-05
MACMUX(8)	Ø	4.5-01	B59	P08-07
NAØR	Ø	4.5-02	C56	P11-06
NERRØR(O)	Ø	4.5-02	C57	P10-04
NERROR(1)	8	4.5-02 4.5-02	C58 C59	P10-03 P10-06
NERRØR(2) NERRØR(3)	Ø	4.5-02	C60	P10-07
NPCLOA(O)	ø	4.5-03	D65	P02-10
NPCLOA(1)	Ø	4.5-03	D66	P02-1B
NPCLOA(2)	0	4.5-03	D67	P02-15
NPCLOB(0)	<u>Ø</u>	4.5-03 4.5-03	E04	P13-09 P13-15
NPCLOB(1) NPCLOB(2)	Ø	4.5-03 4.5-03	E05 E06	P13-15
NPCLIA(O)	ø	4.5-03	DT4	P02-09
NPCLIA(I)	Ø	4.5-03	D75	202-07
NPCL1A(2)	Ø	4.5-03 4.5-03 4.5-03	D76	P02-06
NPCL1B(O)	Ø	4.5-03	E13	P12-22 P12-24
NPCLIB(1)	0	4.5-03 4.5-03	E14 E15	P12-24
NPCL1B(2) PCLOAA(0)	Ø	4.5-03	D59	P12-21 P02-20
PCLOAA(I)	ø	4.5-03	D60	102-16
PCLOAA(2)	Ø	4.5-03	D61	P02-17
PCLOAA(3)	Ø	4.5-03	D6Z	PQ1-05
PCLOAA(4)	Ø	4.5-03	D63	PO1-06
PCLOAR(5)	8	4.5-03	D64	P01-07 P01-24
PCLOAB(O) PCLOAB(I)	8	4.5-03 4.5-03	D56 D57	P01-20
PCLOAB(2)	Ø	4.5-03	D58	P01-15
PCLOAC(O)	Ø	4.5-03	D53	P02-22
PCLQAC(I)	Ø	4.5-03	D54	P02-21
PCLOAC(2)	Ø	4.5-03	D55	P02-19
PCLOAD(O)	0	4.5-03 4.5-03	D50 D51	P01-22 P01-21
PCLOAD(1) PCLOAD(2)	Ø	4.5-03	052	PO1-17
PCLOBALQ)	ø	4.5-03	D98	P13-01
PCLOBA(I)	Ø	4.5-03	D99	P13-10
PCLOBA(2)	Ø	4.5-03	E00	P13-01 P13-10 P13-03
PCLOBA(3)	0	4.5-03	E01	P13-22

PCLOBA(4)	EAL
PCLOBA(4)	IN
PCLOBA(5) PCLOBB(0) PCLOBB(1) PCLOBB(1) PCLOBB(1) PCLOBB(1) PCLOBB(2) PCLOB(2) PCLOB(2) PCLOB(0) PCLOB(0) PCLOB(0) PCLOB(1) PCLOB	3-19
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PCLOBR(2) PCLOBC(0) PCLOBC(1) PCLOBC(1) PCLOBC(1) PCLOBC(1) PCLOBC(1) PCLOBC(2) PCLOBC(1) PCLOBC(2) PCLOBC(1) PCLOBC(2) PCLOBC(3) PCLOBC(4) PCLOBC	
PCLOBACO PCLOBOLO PCL	2-03
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PCLOBOLO 0	3-06
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PCL2B(0)	3-15
PCL2B(2) Ø 4.5-03 E1B P1: PCL2B(3) Ø 4.5-03 E1B P1: PCL2B(4) Ø 4.5-03 E2O P1: PCL2B(5) Ø 4.5-03 E2C P1: PCL3A(1) Ø 4.5-03 D83 P0: PCL3A(1) Ø 4.5-03 D84 P0: PCL3A(2) Ø 4.5-03 D85 P0: PCL3A(3) Ø 4.5-03 D86 P0: PCL3A(4) Ø 4.5-03 D86 P0: PCL3A(5) Ø 4.5-03 D86 P0: PCL3B(5) Ø 4.5-03 D86 P0: PCL3B(6) Ø 4.5-03	3-20
PCL2B(2) Ø 4.5-03 E1B P1: PCL2B(3) Ø 4.5-03 E1B P1: PCL2B(4) Ø 4.5-03 E2O P1: PCL2B(5) Ø 4.5-03 E2C P1: PCL3A(1) Ø 4.5-03 D83 P0: PCL3A(1) Ø 4.5-03 D84 P0: PCL3A(2) Ø 4.5-03 D85 P0: PCL3A(3) Ø 4.5-03 D86 P0: PCL3A(4) Ø 4.5-03 D86 P0: PCL3A(5) Ø 4.5-03 D86 P0: PCL3B(5) Ø 4.5-03 D86 P0: PCL3B(6) Ø 4.5-03	3-24 3-21
PCL2B(3) 9 4.5-03 E19 P1. PCL2B(4) 0 4.5-03 E20 P1. PCL2B(5) 0 4.5-03 E21 P1. PCL3A(0) 0 4.5-03 D83 P0. PCL3A(1) 0 4.5-03 D84 P0. PCL3A(2) 0 4.5-03 D85 P0. PCL3A(3) 0 4.5-03 D86 P0. PCL3A(4) 0 4.5-03 D86 P0. PCL3A(4) 0 4.5-03 D86 P0. PCL3A(5) 0 4.5-03 D86 P0. PCL3B(0) 0 4.5-03 D88 P0. PCL3B(0) 0 4.5-03 D88 P0. PCL3B(0) 0 4.5-03 D88 P0.	2-09
PCL2B(5) 9 4.5-03 E21 P1 PCL3A(0) 0 4.5-03 D83 P0 PCL3A(1) 0 4.5-03 D84 P0 PCL3A(2) 0 4.5-03 D85 P0 PCL3A(3) 0 4.5-03 D86 P0 PCL3A(4) 0 4.5-03 D87 P0 PCL3A(5) 0 4.5-03 D88 P0 PCL3B(0) 0 4.5-03 E22 P1	2-19
PCL 3A(4) Ø 4.5-03 D86 PO PCL 3A(4) Ø 4.5-03 D88 PO PCL 3B(0) Ø 4.5-03 E82 PI PCL 3B(0) Ø 4.5-03 E82 PI	2-18
PCL 3A(4) Ø 4.5-03 D86 PO PCL 3A(4) Ø 4.5-03 D88 PO PCL 3B(0) Ø 4.5-03 E82 PI PCL 3B(0) Ø 4.5-03 E82 PI	2-20 3-07
PCL 3A(4) Ø 4.5-03 D86 PO PCL 3A(4) Ø 4.5-03 D88 PO PCL 3B(0) Ø 4.5-03 E82 PI PCL 3B(0) Ø 4.5-03 E82 PI	3-10
PCL 3A(4) Ø 4.5-03 D86 PO PCL 3A(4) Ø 4.5-03 D88 PO PCL 3B(0) Ø 4.5-03 E82 PI PCL 3B(0) Ø 4.5-03 E82 PI	3-08
PCL3B(0) Ø 4.5-03 E22 P1	3-05
PCL3B(0) Ø 4.5-03 E22 P1	3-16
0.0 30(1)	1-20
PCL3B(2) Ø 4.5-03 E24 P1 PCL3B(3) Ø 4.5-03 E25 P1	1-08
70130137 9 7.3°03 CLJ F1	1-16
PCL3B(4) Ø 4.5-03 E26 P1	1-22
PCL3B(5) Ø 4.5-03 E27 PI	1-07

MØDULE PIN NAME	I/0	SHEET	VIRTUAL PIN	REAL PIN
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	LEVEL 4 CØNNECTØR CHART SUPPLEMENTAL WIRING INFØRMATIØN BØARD TYPE – CIGBH	CHOSE TOTAL DATO NO		ACO
DEVELØPMENT DIVISIØN	BOARD TIPE - UGBH	GBA-CC	PALE.	

SECTION 2

SYMBOL DESCRIPTION SHEETS

INTRODUCTION

This section contains the descriptive sheets for LSI arrays and ECL 100K microcircuits. The sheets are arranged in ascending order of LSI array/ECL 100K circuit type which is located in the upper-left corner. These circuit types correspond to 12XX for the LSI arrays, 12HX for the LSI half-pak arrays, and 12XXX for the ECL 100K series circuits.

INFORMATION CATEGORIES

Each sheet(s) contains the following information.

- Logic symbol
- Bias information
- Operational description

Depending upon the circuit type, the following information categories may also be included.

- Boolean algebra equation(s)
- Timing diagram

NOTE

In the REAL-to-VIRT pin tables, the horizontal line separates inputs (above line) and outputs (below line).

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12AA

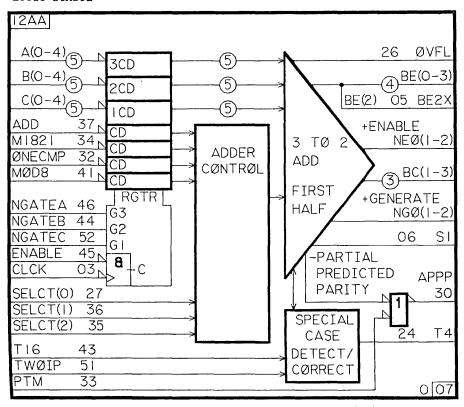
PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	09	V01
A(1)	11	V02
A(2)	16	V03
A(3)	17	V04
A(4)	19	V05
ADD	37	V26
B(0)	22	V06
B(1)	20	V07
B(2)	15	V08
B(3)	38	V09
B(4)	10	V10
C(0)	08	V11
C(1)	42	V12
C(2)	12	V13
C(3)	18	V14
C(4)	21	V15
CLCK	03	V16
ENABLE	45	V18
M1821	34	V28
MOD8	41	V25
NFORCE	02	V17
NGATEA	46	V19
NGATEB	44	V20
NGATEC	52	V21
ONECMP PTM SELCT(0) SELCT(1)		V27 V47 V22 V23
SELCT(2) T16 TWOIP	35 43 51 30	V24 V29 V30 V44
BC(1)	23	V35
BC(2)	28	V36
BC(3)	29	V37
BE(0)	50	V31
BE(1)	07	V32
BE(2)	04	V33
BE(3)	25	V34
BE2X	05	V43
NEO(1)	48	V40
NEO(2)	47	V41
NGO(1)	01	V38
NGO(2)	49	V39
OVFL	26	V46
S1	06	V42
T4	24	V45

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12AA-0 First-Half Adder (Block Diagram).

LOGIC SYMBOL



BIAS LØ = NFØRCE BIAS HI = NØNE

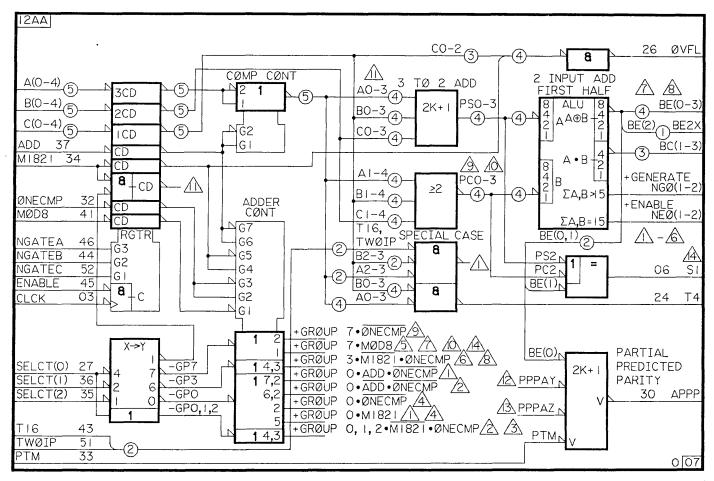
OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagram. Refer to the ANSI symbol.

60458120 B

12AA-0 First-Half Adder (ANSI Symbol).

LOGIC SYMBOL



BIAS LØ = NFØRCE BIAS HI = NØNE 60458120 B

12AA-0 (Cont'd)

The following are notes for the ANSI symbol.

NØTES FØR 12AA TYPE O:

FØRCE PINS NGØ(1-2) HIGH

/2\ FØRCE PINS NGØ(1-2) LØW

3 FØRCE PINS NEØ(1-2) HIGH

4 FØRCE PINS NEØ(1-2) LØW

 \oint PINS NGØ(1-2) = \overline{PSO} PINS NEØ(1-2) = PSO

 $\triangle 6$ PINS NEØ(1-2) = $\triangle 4$, B $\frac{2}{1}$, B $\frac{2}{1}$ = 3 PINS NGØ(1-2) = $\triangle 4$, B $\frac{2}{1}$ > 3

FØRCE PINS BC(1-3) HIGH FØRCE PINS BE(1-3) AND BE2X LØW

FØRCE PINS BC(0-1) HIGH FØRCE PINS BE(0-1) LØW

9 FØRCE PC3 LØW

PIN BC(0) = PSO PIN BE(0) = PSO

⚠ FØRCE AO-2 AND BO-2 LØW AT INPUT TØ 3 TØ 2 ADD

 $\sqrt{2}$ PPPAY = $\overline{BC2}$ $\overline{BE2}$ BE3 + $\overline{BC2}$ BC3 + BE2 $\overline{BE3}$ + BC2 $\overline{BC3}$ $\overline{BE3}$

PPPAZ = BCI + BC2 BEI (BC3 BE2)

14 FØRCE PIN SI LØW

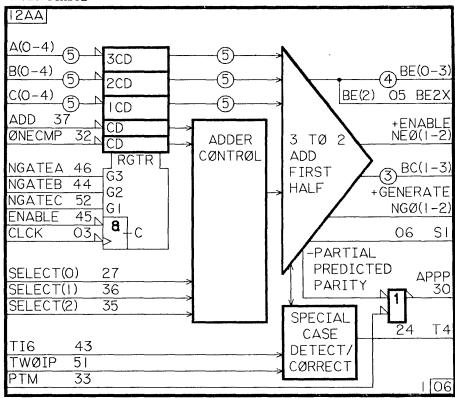
OPERATIONAL DESCRIPTION

To be supplied later.

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12AA-1 First-Half Adder (Block Diagram).

LOGIC SYMBOL



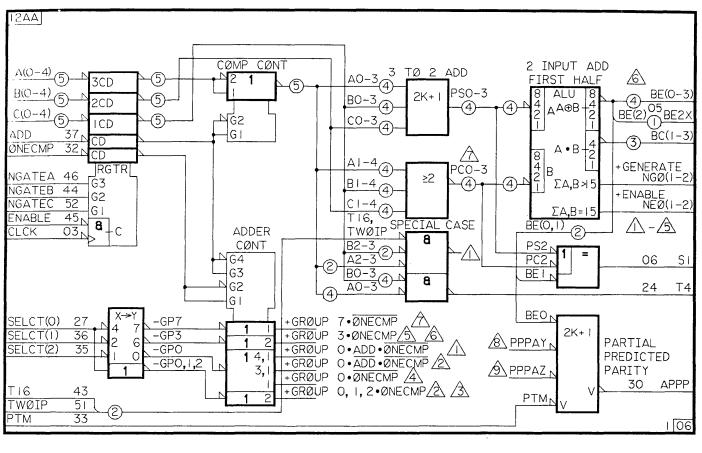
BIAS LØ = NFØRCE

BIAS HI = M1821, MØD8

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagram. Refer to the ANSI symbol.





BIAS BIAS # F $\mathbf{n} = \mathbf{n}$ = NFØRCE = M1821, MØD8

60458120

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12AA-1 (Cont'd)

The following are notes for the ANSI symbol.

NØTES FØR 12AA TYPE 1:

- FØRCE PINS NGØ(1-2) HIGH
- ♠ FØRCE PINS NGØ(1-2) LØW
- ⚠ FØRCE PINS NEØ(1-2) HIGH
- A FØRCE PINS NEØ(1-2) LØW
- \triangle PINS NEØ(1-2) = ΣA_1^2 , B_1^2 = 3 PINS NGØ(1-2) = ΣA_1^2 , B_1^2 > 3
- FØRCE PINS BC(0-1) HIGH FØRCE PINS BE(0-1) LØW
- A FØRCE PC3 LØW
- \bigcirc PPPAY = \bigcirc BC2 BE3 + \bigcirc BC2 BC3 + BC2 \bigcirc BC3 + BC2 \bigcirc BC3 \bigcirc BE3
- PPPAZ = BCI + BCZ BEI (BC3 BEZ)

OPERATIONAL DESCRIPTION

To be supplied later.

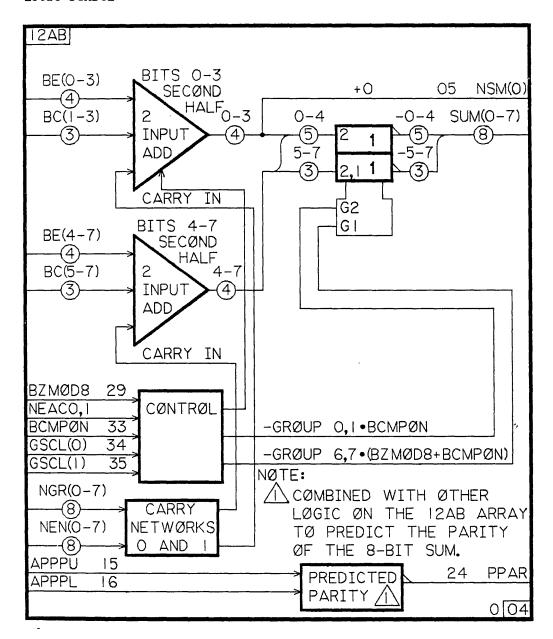
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12AB

PIN	REAL	VIRT
NAME	PIN	PIN
APPPL	16	V38
APPPU	15	V37
BC(1)	06	V05
BC(2)	07	V06
BC(3)	11	V07
BC(5)	18	V12
BC(6)	21	V13
BC(7)	17	V14
BCMPON	33	V20
BE(0)	01	V01
BE(1)	10	V02
BE(2)	08	V03
BE(3)	09	V04
BE(4)	19	V08
BE(5)	22	V09
BE(6)	20	V10
BE(7)	12	V11
BZMOD8	29	V19
GSCL(0)	34	V17
GSCL(1)	35	V18
NEACO	43	V15
NEAC1	37	V16
NEN(0)	42	V29
NEN(1)	52	V30
NEN(2)	51	V31
NEN(3)	47	V32
NEN(4)	32	V33
NEN(5)	23	V34
NEN(6)	28	V35
NEN(7)	49	V36
NGR(0)	45	V21
NGR(1)	50	V22
NGR(2)	44	V23
NGR(3)	46	V24
NGR(4)	48	V25
NGR(5)	36	V26
NGR(6)	38	V27
NGR(7)	41	V28
NSM(0)	05	V48
PPAR	24	V47
SUM(0)	04	V39
SUM(1)	03	V40
SUM(2)	02	V41
SUM(3)	31	V42
SUM(4)	30	V43
SUM(5)	27	V44
SUM(6)	26	V45
SUM(7)	25	V46

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LOGIC SYMBOL

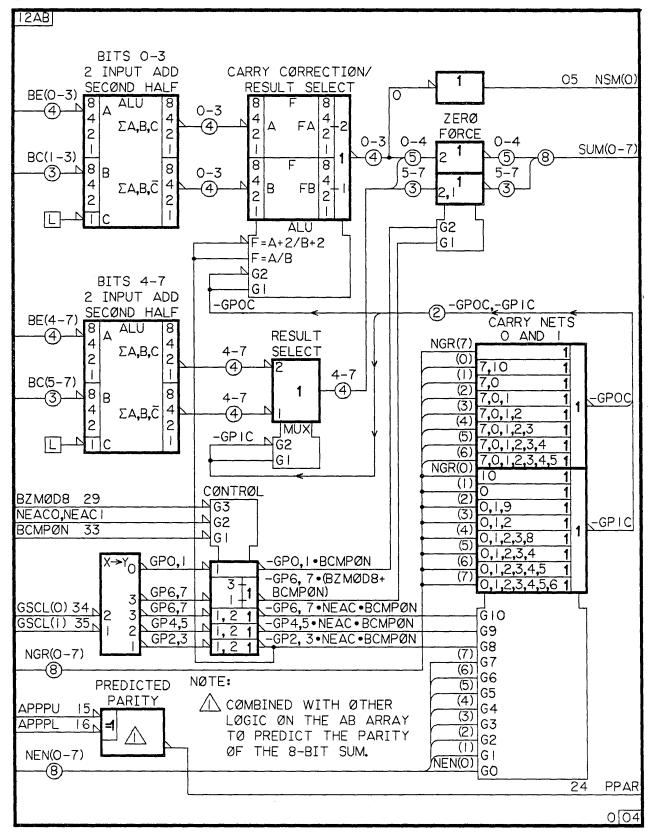


BIAS=NONE

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagram. Refer to the ANSI symbol.

LOGIC SYMBOL

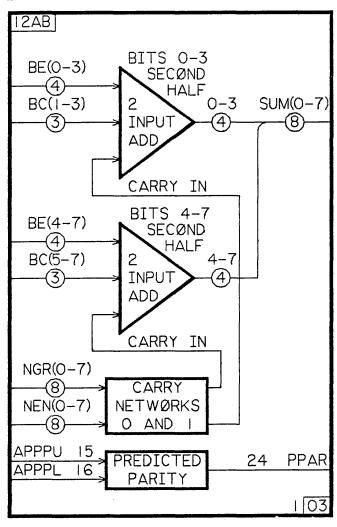


BIAS=NONE

12AB-0 OPERATIONAL DESCRIPTION

To be supplied later.

60458120 B



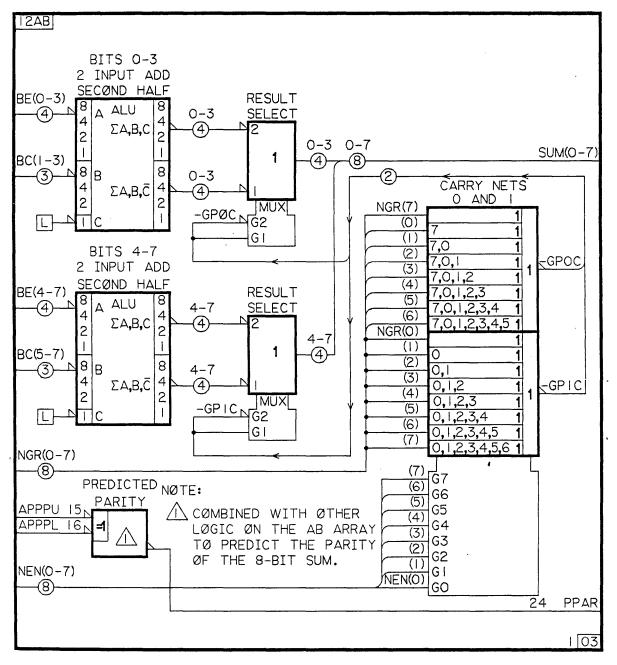
BIAS LØ = NØNE

BIAS HI = BZMØD8, NEACO, NEACI, BCMPØN, GSCL(O-I)

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagram. Refer to the ANSI symbol.

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BIAS LØ = NØNE

BIAS HI = BZMØD8, NEACO, NEACI, BCMPØN, GSCL(O-I)

OPERATIONAL DESCRIPTION

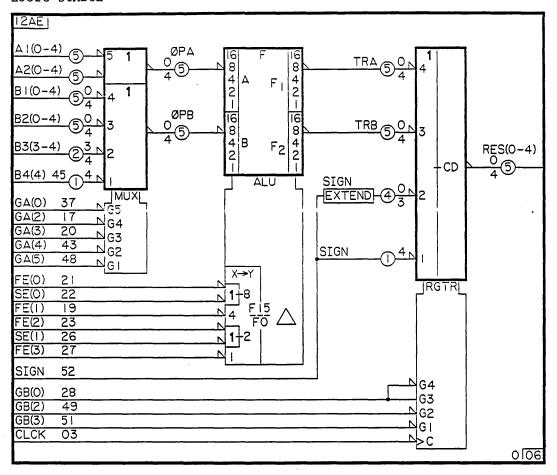
To be supplied later.

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12AE

PIN	REAL	VIRT
NAME	PIN	PIN
A1(0)	33	V01
A1(1) A1(2)	34 36	V05 V09
A1(3)	30	V13
A1(4)	41	V18
A2(0) A2(1)	31 35	V02 V06
A2(1)	38	V10
A2(3)	32	V14
A2(4) B1(0)	44 18	V19 V03
B1(1)	15	V03
B1(2)	12	V11
B1(3) B1(4)	09 47	V15 V20
B2(0)	06	V04
B2(1)	16	V08
B2(2) B2(3)	11 10	V12 V16
B2(4)	50	V21
B3(3)	08	V17
B3(4) B4(4)	46 45	V22 V23
CLCK	03	V30
FE(0)	21	V34
FE(1) FE(2)	19 23	V35 V37
FE(3)	27	V38
GA(0)	37	V24
GA(2) GA(3)	17 20	V26 V27
GA(4)	43	V28
GA(5)	48	V29
GB(0) GB(2)	28 49	V39 V41
GB(2)	51	V43
LSGN	07	V25
NFOR SE(0)	01 22	V31 V33
SE(1)	26	V36
SEL SIGN	42 52	V40 V42
NOSG	05	V32
RES(0)	29	V44
RES(1) RES(2)	25 24	V45 V46
RES(3)	04	V47
RES(4)	02	V48

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BIAS LØ = NFØR, SEL, LSGN BIAS HI = NØNE

NØTE: \triangle THIS TABLE SHØWS THE BØØLEAN EQUATIØN FØR ØUTPUTS F₁ AND F₂ FØR EACH FUNCTIØN.

FUNCTIØN	ØUTPUT F _I	ØUTPUT F ₂	FUNCTIØN	ØUTPUT F _I	ØUTPUT F ₂
FO F 2 F 4 F 5 F 6 F 7	B B B B B B B B B B B B B B	31 BAA31 BAAA	F8 F9 F11 F12 F13 F15	B	31 B A A B B A A = B

12AE-0 (Cont'd)

OPERATIONAL DESCRIPTION

The 12AE-0 contains an input mux, an ALU, and an output mux/register.

Input Mux

The data portion of the input mux (top) divides into two functions. The top function is a mux of the Al and A2 input highways. The A2 highway passes through the mux ungated. Gating modifier G5 controls the Al highway. When G5 is active, the mux function ORs the Al and A2 highways together and passes the result to the OPA highway.

Gating modifiers G1-G4 gate one or more of the B1-B4 highways through the lower mux. When more than one of the gating modifiers are active at the same time, the mux ORs the selected highways together and passes the result to the OPB highway.

Note that the B3 and B4 inputs are not 5 bits wide like the other input highways. The B3(3,4) inputs go to bit positions 3 and 4 respectively and the B4(4) input goes to bit position 4.

The GA control inputs (when LO) activate the G1-G5 gating modifiers.

ALU

The OPA and OPB highways enter the ALU, are each weighted binarily, and are designated as operands A and B respectively. The ALU has two highwayed outputs which are weighted binarily and designated F1 and F2.

The F qualifying symbol indicates that the symbol is incomplete and the function information is expressed by equations for the Fl and F2 outputs. A table which accompanies the symbol contains this function information.

The FE(0-3) and SE(0,1) inputs are translated to control the 16 ALU functions. FE(0) and SE(0) are ORed together and the result has a weight of 8 in the translator. FE(2) and SE(1) are ORed together and the result has a weight of 2 in the translator. FE(3) and FE(1) have weights of 1 and 4 respectively.

Translations of 0-15 activate F0-F15 respectively. The table shows the equations for the F1 and F2 outputs for each of the 16 translations. For example, a translation of 0 causes the F1 outputs to equal an OR of the complements of the A and B operands and the F2 outputs to equal a binary value of 31 (all bits L0).

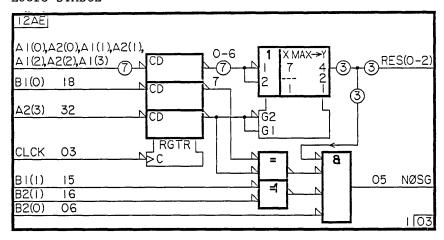
Output Mux/Register

Control inputs GB(0), GB(2), and GB(3) control the output mux and clock on pin CLCK clocks the result of the mux into the register.

GB(0) selects butween the TRA and TRB highways. GB(2) and GB(3) control sign extension. When GB(2) is LO, gating modifier G2 is active and extends sign to bit positions 0-3. When GB(3) is LO, G1 is active and extends sign to bit position 4.

When more than one gating modifier is active at the same time, the mux ORs the selected highways together and passes the result to the register.

60458120 B 2 of 2



BIAS LØ = GB(2,3), SIGN, NFØR

BIAS HI = SEL

OPERATIONAL DESCRIPTION

The 12AE-1 receives 8 data-bits and a sign bit and determines the highest-order bit which is different than the sign bit. It then produces a 3-bit code which contains the complement of the weight of that bit.

Input Register and Priority Coder

Data bits 0-7 enter pins A1(0), A2(0), A1(1), A2(1), A1(2), A2(2), A1(3), and B1(0) respectively. Bit 0 on pin A1(0) is the most-significant bit. Sign enters pin A2(3).

Clock on pin CLCK, clocks the data bits and sign into the input register. The most-significant 7 data bits (0-6) from the register, connect to the priority coder.

When sign is LO, gating modifier G2 is active causing the 7-data bits to enter the priority coder active HI. When sign is HI, Gl is active and the 7-data bits enter the priority coder active LO. The priority coder assigns weights of 7-1 to bits 0-6 respectively. The least significant data bit (bit 7) does not enter the priority coder because it has a weight of 0 and would not affect the code.

The priority coder determines the most significant active bit and produces a 3-bit code containing the weight of that bit. The priority coder outputs the code active HI, i.e., RES(0-2) outputs are all LO for a code of 0. RES(0) is the most-significant code bit.

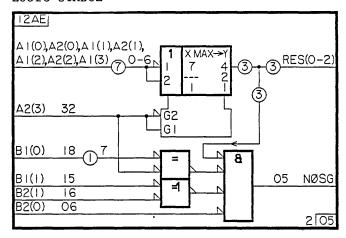
Significant Data Test

Input pins B1(1), B2(1), and B2(0) are control signals which enable a network which determines if any of the 8-data bits are different than the sign bit (significant data).

12AE-1 (Cont'd)

Output pin NOSG is HI when the network is enabled and there are no data bits which are different than sign. The network is enabled (lower two inputs to the AND gate are LO when pin B1(1) is not equal to B2(1) and pin B2(0) is LO. There are no data bits different than sign when bit 7 is equal to sign and all three priority coder outputs are LO (code of 0).

60458120 B 2 of 2



BIAS LØ = GB(2,3), SIGN BIAS HI = SEL, NFØR

OPERATIONAL DESCRIPTION

The 12AE-2 receives 8 data-bits and a sign bit and determines the highest-order bit which is different than the sign bit. It then produces a 3-bit code which contains the complement of the weight of that bit.

Priority Coder

Data bits 0-7 enter pins Al(0), A2(0), A1(1), A2(1), A1(2), A2(2), A1(3), and B1(0) respectively. Bit 0 on pin Al(0) is the most-significant bit. Sign enters pin A2(3).

When sign is LO, gating modifier G2 is active causing the 7-data bits to enter the priority coder active HI. When sign is HI, G1 is active and the 7-data bits enter the priority coder active LO. The priority coder assigns weights of 7-1 to bits 0-6 respectively. The least significant data bit (bit 7) does not enter the priority coder because it has a weight of 0 and would not affect the code.

The priority coder determines the most significant active bit and produces a 3-bit code containing the weight of that bit. The priority coder outputs the code active HI, i.e., RES(0-2) outputs are all LO for a code of 0. RES(0) is the most-significant code bit.

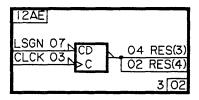
Significant Data Test

Input pins B1(1), B2(1), and B2(0) are control signals which enable a network which determines if any of the 8-data bits are different than the sign bit (significant data).

Output pin NOSG is HI when the network is enabled and there are no data bits which are different than sign. The network is enabled (lower two inputs to the AND gate are LO when pin B1(1) is not equal to B2(1) and pin B2(0) is LO. There are no data bits different than sign when bit 7 is equal to sign and all three priority coder outputs are LO (code of 0).

12AE-3 One-Bit Latch.

LOGIC SYMBOL



THIS BIAS IS COMPATIBLE WITH TYPE |
BIAS LO = GB(2,3), SIGN, NFOR
BIAS HI = NONE

OPERATIONAL DESCRIPTION

Clock on pin CLCK clocks the data on pin LSGN into the latch.

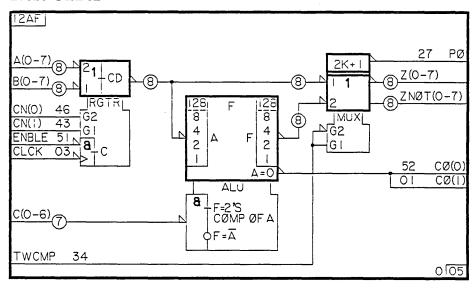
12AF

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	12	V01
A(1)	16	V03
A(2)	10	V05
A(3)	09	V07
A(4)	32	V09
A(5)	37	V11
A(6)	42	V13
A(7)	44	V15
B(0)	20	V02
B(1)	15	V04
B(2)	11	V06
B(3)	08	V08
B(4)	35	V10
B(5)	38	V12
B(6)	41	V14
B(7)	45	V16
C(0)	19	V22
C(1)	26	V23
C(2)	17	V24
C(3)	28	V25
C(4)	25	V26
C(5)	18	V27
C(6)	36	V28
CLCK	03	V19
CN(0)	46	V17
CN(1)	43	V18
ENBLE	51	V21
NFORCE TWCMP	07 34 52	V21 V20 V32 V29
CO(1)	01	V30
PO	27	V31
Z(0)	22	V34
Z(1)	24	V36
Z(2)	06	V38
Z(3)	04	V40
Z(4)	29	V42
Z(5)	33	V44
Z(6)	50	V46
Z(7)	47	V48
ZNOT(0)	21	V33
ZNOT(1)	23	V35
ZNOT(2)	05	V37
ZNOT(3)	02	V39
ZNOT(4)	30	V41
ZNOT(5)	31	V43
ZNOT(6)	49	V45
ZNOT(7)	48	V47

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12AF-0 Mux/Register with Ones or Twos Complement Network.

LOGIC SYMBOL



BIAS LØ = NFØRCE BIAS HI = NØNE

OPERATIONAL DESCRIPTION

The 12AF-0 contains three functional elements, an input mux/register, an ALU, and an outut mux.

Input Mux/Register

Pins CN(0,1) are active HI and control gating modifiers G2 and G1 which gate the A and B highways through the mux. When both gating modifiers are active at the same time, the two highways are ORed together.

Clock on pin CLCK and an enable signal are ANDed together to control clock modifier C. C clocks the mux result into the register.

ALU

The 8-bit register output enters the ALU where it is weighted binarily and designated as operand A. The 8-bit ALU output is weighted binarily and designated as operand F. The ALU also has an output which is LO when the A operand is equal to zero.

The F qualifying symbol indicates that the symbol is incomplete and the function information is expressed by equations in the common control block.

Input pins C(0-6) enter the common control block of the ALU where they are ANDed together to control the function. When the AND gate is active (all inputs LO), the F operand is the two's complement of the A operand. When the AND gate is not active, the F operand is the complement of the A operand.

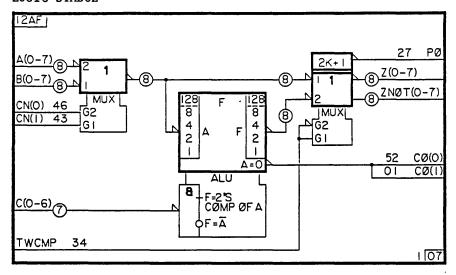
12AF-0 (Cont'd)

Output Mux/Register

Input pin TWCMP selects between two highways, one from the input register (TWCMP HI), or one from the ALU (TWCMP LO). Two highways carry the selected data out of the array. The Z(0-7) outputs are active LO and the ZNOT(0-7) outputs are active HI.

The output mux has a common output block at the top of the symbol (above the double line). The highway selected by the mux is the input to the common output block. The PO output is LO when there are an odd number of active bits in the selected highway.

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BIAS LØ = CLCK, ENBLE BIAS HI = NFØRCE

OPERATIONAL DESCRIPTION

The 12AF-1 contains three functional elements, an input mux/register, an ALU, and an outut mux.

Input Mux

Pins CN(0,1) are active HI and control gating modifiers G2 and G1 which gate the A and B highways through the mux. When both gating modifiers are active at the same time, the two highways are ORed together.

ALU

The 8-bit register output enters the ALU where it is weighted binarily and designated as operand A. The 8-bit ALU output is weighted binarily and designated as operand F. The ALU also has an output which is LO when the A operand is equal to zero.

The F qualifying symbol indicates that the symbol is incomplete and the function information is expressed by equations in the common control block.

Input pins C(0-6) enter the common control block of the ALU where they are ANDed together to control the function. When the AND gate is active (all inputs L0), the F operand is the two's complement of the A operand. When the AND gate is not active, the F operand is the complement of the A operand.

Output Mux

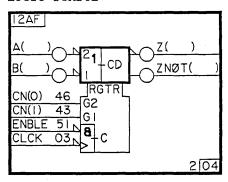
Input pin TWCMP selects between two highways, one from the input mux (TWCMP HI), or one from the ALU (TWCMP LO). Two highways carry the selected data out of the array. The Z(0-7) outputs are active LO and the ZNOT(0-7) outputs are active HI.

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12AF-1 (Cont'd)

The output mux has a common output block at the top of the symbol (above the double line). The highway selected by the mux is the input to the common output block. The PO output is LO when there are an odd number of active bits in the selected highway.

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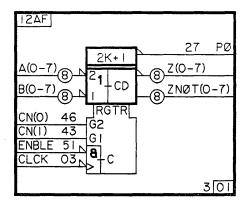
BIAS LØ = NFØRCE BIAS HI = TWCMP

OPERATIONAL DESCRIPTION

Pins CN(0,1) are active HI and control gating modifiers G2 and G1 which gate the A and B highways through the mux. When both gating modifiers are active at the same time, the two highways are ORed together. When both gating modifiers are inactive, zeros are on the input to the register.

Clock on pin CLCK and an enable signal are ANDed together to control clock modifier C. C clocks the mux result into the register.

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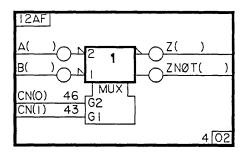
BIAS LØ = NFØRCE BIAS HI = TWCMP

OPERATIONAL DESCRIPTION

Pins CN(0,1) are active HI and control gating modifiers G2 and G1 which gate the A and B highways through the mux. When both gating modifiers are active at the same time, the two highways are ORed together.

Clock on pin CLCK and an enable signal are ANDed together to control clock modifier C. C clocks the mux result into the register.

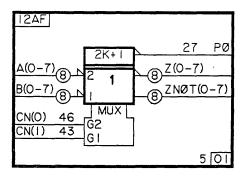
The register has a common output block at the top of the symbol (above the double line). The content of the register is the input to the common output block. The PO output is LO when there are an odd number of active bits in the register.



BIAS LØ = CLCK, ENBLE BIAS HI = NFØRCE, TWCMP

OPERATIONAL DESCRIPTION

Pins CN(0,1) are active HI and control gating modifiers G2 and G1 which gate the A and B highways through the mux. When both gating modifiers are active at the same time, the two highways are ORed together.



BIAS LØ = CLCK, ENBLE BIAS HI = NFØRCE, TWCMP

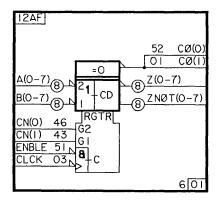
OPERATIONAL DESCRIPTION

Pins CN(0,1) are active HI and control gating modifiers G2 and G1 which gate the A and B highways through the mux. When both gating modifiers are active at the same time, the two highways are ORed together.

The mux has a common output block at the top of the symbol (above the double line). The highway selected by the mux is the input to the common output block. The PO output is LO when there are an odd number of active bits in the selected highway.

12AF-6 Mux/Register with Zero Check.

LOGIC SYMBOL



BIAS LØ = NFØRCE BIAS HI = TWCMP

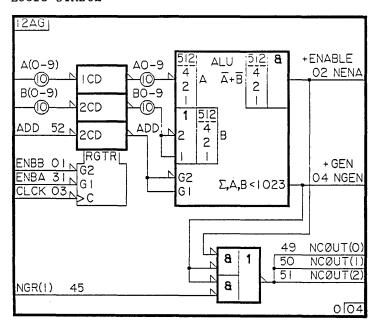
OPERATIONAL DESCRIPTION

Pins CN(0,1) are active HI and control gating modifiers G2 and G1 which gate the A and B highways through the mux. When both gating modifiers are active at the same time, the two highways are ORed together.

Clock on pin CLCK and an enable signal are ANDed together to control clock modifier C. C clocks the mux result into the register.

The register has a common output block at the top of the symbol (above the double line). The content of the register is the input to the common output block. The CO(0,1) outputs are both LO when the contents of the register is equal to zero (no bits active).

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	17	V01
A(1)	16	V02
A(2)	11	V03
A(3)	09	V04
A(4)	10	V05
A(5)	38	V06
A(6)	34	V07
A(7)	33	V08
A(8)	44	V09
A(9)	43	V10
ADD	52	V26
B(0)	18	V11
B(1)	15	V12
B(2)	12	V13
B(3)	06	V14
B(4)	08	V15
B(5)	42	V16
B(6)	37	V17
B(7)	35	V18
B(8)	41	V19
B(9)	47	V20
CLCK	03	V23
ENBA	31	V22
ENBB	01	V25
NE(0)	32	V31
NE(1)	29	V32
NE(2)	21	V33
NE(3)	22	V34
NFRC	07	V24
NG(1)	25	V35
NG(2)	20	V36
NG(3)	19	V37
NGR(1)	45	V30
NSIGN	36	V21
AND	27	V48
C(0)	28	V44
C(1)	26	V45
C(2)	23	V46
C11	30	V47
EQ	24	V41
GEN NCOUT(0) NCOUT(1) NCOUT(2)	50	V40 V42 V43 V29
NENA	02	V38
NGEN	04	V39



BIAS LØ = NFRC BIAS HI = NØNE

-

OPERATIONAL DESCRIPTION

The 12AG-0 has three functional elements: an input register, an ALU, and a carry network.

Input Register

The input register functional element consists of two 10-bit registers and a 1-bit register. Input pins ENBA and ENBB control gating modifiers G1 and G2 which gate the input data to the input of the register. Clock on pin CLCK clocks the selected data into the registers. A register loads zeros when the clock modifier is active while the gating modifier at the input to that register is inactive.

ALU

The A highway enters the ALU where it is weighted binarily and designated as operand A_{\bullet}

The ADD signal controls the complementing of the B highway. When ADD is HI, gating modifier Gl is active and gates the complement of the B highway (active HI) into the ALU. G2 gates the B highway active LO. The selected state of the B highway is weighted binarily and designated as operand B.

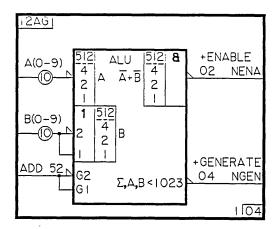
Output NENA is a group enable and is HI when there is a 00, 10, or 01 combination in each bit position of the A and B operands.

Output NGEN is a group generate and is HI when the summation of A and B is less than 1023.

<u>12AG-0</u> (Cont'd)

Carry Network

The NCOUT (0-2) outputs are LO when the following pins are LO: (NENA AND NGEN) OR [NGEN AND NGR(1)].



BIAS LØ = ENBA, ENBB, CLCK BIAS HI = NFRC

OPERATIONAL DESCRIPTION

The A highway enters the ALU where it is weighted binarily and designated as operand $A_{\:\raisebox{1pt}{\text{\circle*{1.5}}}}$

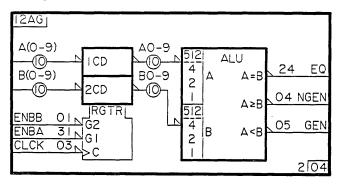
The ADD signal controls the complementing of the B highway. When ADD is HI, gating modifier Gl is active and gates the complement of the B highway (active HI) into the ALU. G2 gates the B highway active LO. The selected state of the B highway is weighted binarily and designated as operand B.

Output NENA is a group enable and is HI when there is a 00, 10, or 01 combination in each bit position of the A and B operands.

Output NGEN is a group generate and is HI when the summation of A and B is less than $1023_{\:\raisebox{1pt}{\text{\circle*{1.5}}}}$

12AG-2 Register to a Compare Network.

LOGIC SYMBOL



BIAS LØ = NFRC BIAS HI = ADD

OPERATIONAL DESCRIPTION

Input Register

The input register functional element consists of two 10-bit registers. Input pins ENBA and ENBB control gating modifiers G1 and G2 which gate the input data to the input of the registers. Clock on pin CLCK clocks the selected data into the registers. A register loads zeros when the clock modifier is active while the gating modifier at the input to that register in inactive.

ALU

The A and B highways enter the ALU where they are each weighted binarily and designated as operands A and B respectively.

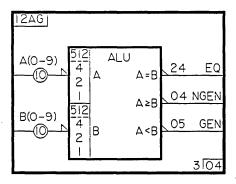
Output EQ is LO when the A operand is equal to the B operand.

Output NGEN is LO when the A operand is greater-than, or equal-to the B operand.

Output GEN is LO when the A operand is less than the B operand.

12AG-3 Compare Network.

LOGIC SYMBOL



BIAS L \emptyset = ENBA, ENBB, CLCK BIAS HI = ADD, NFRC

OPERATIONAL DESCRIPTION

The A and B highways enter the ALU where they are each weighted binarily and designated as operands A and B respectively.

Output EQ is LO when the A operand is equal to the B operand.

Output NGEN is LO when the A operand is greater-than, or equal-to the B operand.

Output GEN is LO when the A operand is less than the B operand.

12AG-4 AND Gate.

LOGIC SYMBOL

12AG				
NG(1) NG(2)	25 _N	8	1 27	AND
NG(3)	19			
NE(3)	25 V		28	C(O)
L			-	4 04

BIAS LØ = NØNE BIAS HI = NE(1,2)

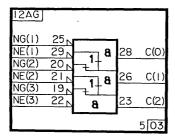
NØTE: CØMPATIBLE WITH 12AG TYPES O, 1, 2, AND 3.

OPERATIONAL DESCRPTION

(None required.)

12AG-5 Carry Network.

LOGIC SYMBOL



BIAS LØ = NSIGN BIAS HI = NØNE

NØTE: CØMPATIBLE WITH 12AG TYPES O, 1, 2, AND 3.

OPERATIONAL DESCRIPTION

Inputs and Outputs

- + Generates enter pins NG(1-3).
- + Enables enter pins NE(1-3).
- + Carries leave pin C(0-2).

Carry Network

The carry network is composed of a series of OR gates and AND gates interconnected to propagate a carry upward through the network.

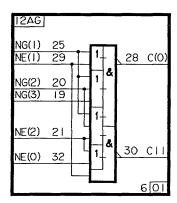
Output pin C(2) is active (HI) when NG(3) AND NE(3) are both active (LO).

Output pin C(1) is active (HI) with the active states of the following: $(C(2) \ OR \ NE(2))$ AND NG(2).

Output pin C(0) is active (HI) with the active states of the following: $(C(1) \ OR \ NE(1)) \ AND \ NG(1)$.

12AG-6 OR/AND Gates.

LOGIC SYMBOL



BIAS LØ = NE(3), NSIGN BIAS HI = NØNE

NØTE: COMPATIBLE WITH 12AG TYPES O, 1, 2, AND 3.

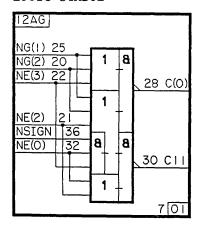
OPERATIONAL DESCRIPTION

Output C(0) is active (LO) with the active HI states of the following: * (NG1 OR NE1) AND (NG1 OR NG2 OR NG3) AND (NG1 OR NG2 OR NE2).

Output Cll is active (LO) with the active HI states of the following: * (NG1 OR NG2 OR NE2) AND (NG2 OR NE0) AND NE1.

60458120 F

^{*} Parentheses were removed from the input pin names in order to make the equation easier to read.



BIAS LØ = NG(3) BIAS HI = NE(1)

NØTE: CØMPATIBLE WITH 12AG TYPES O, 1, 2, AND 3.

OPERATIONAL DESCRIPTION

Output C(0) is active (LO) with the active (HI) states of the following: * (NG1 OR NG2 OR NE3) AND [NG1 OR NG2 OR NE2 OR (NSIGN AND NEO AND NE3)].

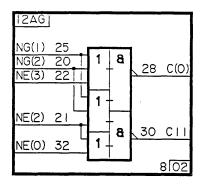
Output Cll is active (LO) with the active (HI) states of the following: * [NG1 OR NG2 OR NE2 OR (NSIGN AND NEO AND NE3)] AND (NEO OR NE2).

60458120 B

^{*} Parentheses were removed from the input pin names in order to make the equations easier to read.

12AG-8 OR/AND Gates.

LOGIC SYMBOL



BIAS LØ = NG(3), NSIGN BIAS HI = NE(1)

NØTE: CØMPATIBLE WITH 12AG TYPES O, 1, 2, AND 3.

OPERATIONAL DESCRIPTON

Output C(0) is active (LO) with the active (HI) states of the following: * (NG1 OR NG2 OR NE3) AND (NG1 OR NG2 OR NE2).

Output Cll is active (LO) with the active (HI) states of the following: * (NG1 OR NG2 OR NE2) AND (NE2 OR NE0).

^{*} Parentheses were removed from the the input pin names in order to make the equations easier to read.

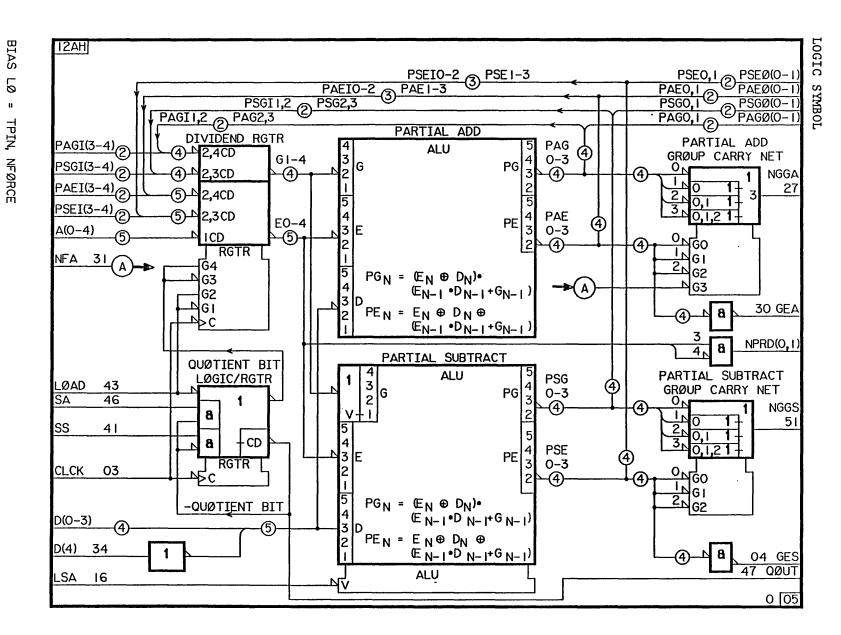
12AH

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	22	V08
A(1)	19	V09
A(2)	06	V10
A(3)	09	V15
A(4)	17	V22
CLCK	03	V01
D(0)	36	V11
D(1)	33	V12
D(2)	35	V25
D(3)	37	V24
D(4)	34	V23
L(0)	26	V40
L(1)	25	V46
L(2)	32	V44
LAT	42	V42
LOAD	43	V07
LSA	16	V39
NFA	31	V43
NFORC	E 01	V02
PAEI(3)	10	V13
PAEI(4) PAGI(3) PAGI(4) PSEI(3)	12 15	V20 V16 V18 V14
PSEI(4) PSGI(3) PSGI(4) SA	11	V21 V17 V19 V05
SS	41	V06
TPIN	44	V03
GEA	30	V27
GES	04	V38
LATO	48	V04
NGGA	27	V29
NGGS	51	V36
NLATO	45	V47
NPRD(0 NPRD(1 PAEO(0 PAEO(1) 07) 29	V48 V45 V32 V30
PAGO(0 PAGO(1 PSEO(0) PSEO(1)) 24 50	V31 V28 V33 V37
PSGO(0) PSGO(1) QOUT Z		V34 V35 V41 V26

		•		
	•			

BIAS

NØNE



	·		

12AH-0 (Cont'd)

OPERATIONAL DESCRIPTION

The 12AH-O array contains the Quotient Bit Logic/Register, Dividend Register, two ALUs which simultaneously add and subtract the divisior to/from the dividend, and carry networks which produce group generates and group enables for each ALU.

Quotient Bit Logic/Register

The Quotient Bit Logic produces one quotient bit per iteration. This logic determines the state of each quotient bit by testing the state of the previous quotient bit (output of the Quotient Bit Register) and the carries from the add and subtract operations (inputs SA and SS respectively).

The equation for the top output from the Quotient Bit Logic and the input to the Quotient Bit Register is: LOAD OR (SA and Quotient Bit) OR (SS and Quotient Bit). The SA and SS inputs are HI when there is a carry from their respective carry networks. These carry networks take the group generates and group enables from 12AH-O arrays and produce the carry signals.

Clock on pin CLCK clocks the result of the Quotient Bit Logic into the Quotient Bit Register.

Quotient Bit Logic and Register Operation

A LO signal on the LOAD input along with clock, starts the divide operation by setting the Quotient Bit Register. This first quotient bit is not used outside the 12AH-O array. Its purpose is to cause a subtract operation during the first iteration.

When the Quotient Bit Register is set, the lower of the two AND gates in the Quotient Bit Logic is enabled to test the result of the subtract operation. If pin SS is HI, the subtract operation was a success and the quotient bit produced by this iteration is also a l (clock again sets the Quotient Bit Register). If pin SS is LO, the subtract operation was not a success and clock clears the Quotient Bit Register. Thus the quotient bit produced by this iteration is a zero.

When the Quotient Bit Register is clear (latest quotient bit equal to 0), the top AND gate is enabled to test the result of the add operation. If pin SA is HI, the add operation was a success and the quotient bit produced by this iteration is a l (clock sets the Quotient Bit Register). If pin SA is LO, the add operation was not a success and the Quotient Bit Register remains clear. Thus the quotient bit produced by this iteration is a 0.

Divident Register

The data portion (top) of the Dividend Register consists of two mux/registers. The top mux/register selects between partial add generate results (PAGI input highway) and partial subtract generate results (PSGI input highway). The bottom mux/register selects between partial add enable results (PAEI input highway), partial subtract enable results (PSEI), and the initial dividend (A input highway).

12AH-0 (Cont'd)

All the partial add and partial subtract results are left-shifted 1 bit position by way of a wired left-shift between the ALU outputs and the Dividend Register inputs. The 2 least-significant bits in each input highway come from the two most-significant bits on the next lower 12AH-O array in the divide network (note the PSEO, PAEO, PSGO, and PAGO output highways). The remaining bits are left-shifted by way of a wired shift on the array.

The LOAD input, the output from the Quotient Bit Logic, and clock control the Dividend Register.

When the LOAD input is LO, gating modifier Gl is active and G2 is inactive. This disables all partial add and partial subtract result inputs and selects the initial dividend inputs (A input highway). Clock clocks the A input highway into the lower portion of the Dividend Register. Clock clears (clocks zeros into) the upper portion of the Dividend Register because G2 is inactive.

When the LOAD input is HI, gating modifier Gl is inactive and G2 is active. This disables the A inputs and allows the Quotient Bit Logic, through G3 and G4, to control the selection of partial add or partial subtract results.

When the output from the Quotient Bit Logic is LO, G3 selects partial subtract results to both portions of the Dividend Register. When the output from the Quotient Bit Logic is HI, G4 selects partial add results. Clock clocks the selected data into the register.

Partial Add

Three data highways enter the Partial Add ALU. Each highway is weighted decimally beginning with one and designated as operand G, E, or D. The G operand is the generates from the Dividend Register, the E operand is the enables (or the initial dividend) from the Dividend Register, and the D operand is the divisor which enters on pins D(0-4). Pin D(4) enters active HI and is inverted to match the rest of the divisor.

Two highways leave the ALU. Each highway is weighted decimally beginning with two. The top highway is the partial add generates designated PG and the bottom highway is the partial add enables designated PE.

Equations in the ALU function show the relationship between the inputs and outputs. For example PG bit 2 = (E bit 2 exclusive OR D bit 2) AND (E bit 1 AND D bit 1 OR G bit 1).

Partial Subtract

The Partial Add and Partial Subtract ALUs are the same except for two small differences. The divisor enters the Partial Subtract ALU active HI (inverted), and input pin LSA (when LO) forces the least-significant bit of the G operand to a one. When LSA is HI, it has no effect on the G operand. Refer to the Partial Add description.

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12AH-0 (Cont'd)

Partial Add Group Carry Network

The Partial Add Group Carry Network receives partial add generates (PAG) and partial add enables (PAE) and determines the group generate (output NGGA) and group enable (output GEA) signals. The NFA input controls gating modifier G3 which gates the NGGA output.

Each PAG input enters an OR function controlled by gating modifiers. The PAE inputs control these gating modifiers.

Output NGGA is active (HI) when NFA is active (LO) and the following equation is active: PAG O OR (PAG 1 AND PAE 0) OR (PAG 2 AND PAE 0 AND PAE 1) OR (PAG 3 AND PAE 0 AND PAE 1 AND PAE 2).

Output GEA is active (LO) when all four PAE signals are LO.

Partial Subtract Group Carry Network

The Partial Subtract Group Carry Network receives partial subtract generates (PSG) and partial subtract enables (PSE) and determines the group generate (output NGGS) and group enable (output GES) signals.

Each PSG input enters an OR function controlled by gating modifiers. The PSE inputs control these gating modifiers.

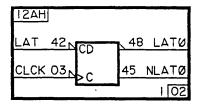
Output NGGS is active (HI) when the following equation is active: PSG 0 OR (PSG 1 AND PSE 0) OR (PSG 2 AND PSE 0 AND PSE 1) OR (PSG 3 AND PSE 0 AND PSE 1 AND PSE 2).

Output GES is active (LO) when all four PSE signals are LO.

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12AH-1 Latch.

LOGIC SYMBOL



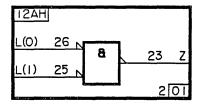
CØMPATIBLE WITH TYPE O BIAS LØ = TPIN, NFØRCE BIAS HI = NØNE

OPERATION DESCRIPTION

Clock on pin CLCK clocks the data on pin LAT into the latch. The latch has an active LO output (LATO) and an active HI output (NLATO).

12AH-2 AND Gate.

LOGIC SYMBOL



COMPATIBLE WITH ALL TYPES BIAS = NONE

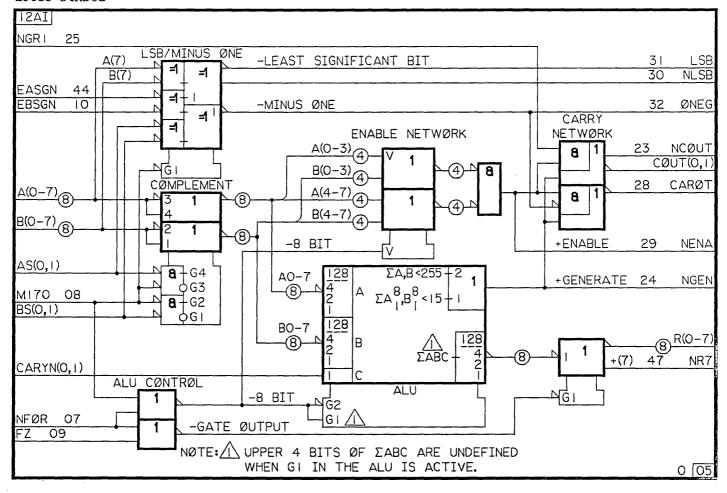
OPERATION DESCRIPTION

(None required.)

12AI

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	20	V03
A(1)	17	V04
A(2)	16	V05
A(3)	11	V06
A(4)	19	V07
A(5)	18	V08
A(6)	15	V09
A(7)	12	V10
AS(0)	22	V01
AS(1)	21	V02
B(0)	38	V13
B(1)	41	V14
B(2)	43	V15
B(3)	45	V16
B(4)	33	V17
B(5)	35	V18
B(6)	37	V19
B(7)	42	V20
BS(0)	36	V11
BS(1)	34	V12
CARYN(0 CARYN(1 CLCK	•	V29 V30 V26
EASGN	44	V24
EBSGN	10	V25
FZ	09	V31
M170	08	V23
NFOR	07	V27
NGR1	25	V28
SEL	46	V32
CAROT	28	V36
COUT(0)	26	V33
COUT(1)	27	V34
LSB	31	V39
NCOUT	23	V35
NENA	29	V38
NGEN	24	V37
NLSB	30	V21
NR7	47	V22
ONEG	32	V40
R(0)	05	V41
R(1)	04	V42
R(2)	02	V43
R(3)	01	V44
R(4)	52	V45
R(5)	49	V46
R(6)	50	V47
R(7)	48	V48

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BIAS LØ = NØNE BIAS HI = SEL

OPERATIONAL DESCRIPTION

LSB/MINUS ONE

Outputs LSB (LO) and NLSB (HI) = (A7 exclusive OR B7) exclusive OR [(EASGN exclusive OR EBSGN) AND M170].

Output ONE $G = (EASGN \ exclusive \ OR \ EBSGN) \ exclusive \ OR \ (AS(0,1)* \ exclusive \ OR \ BS(0,1)* \ AND \ M170.$

^{*} Inputs AS(0) and AS(1) are logically the same. Inputs BS(0) and BS(1) are also logically the same.

Complement

The AS(0,1), BS(0,1) and M170 inputs control the complementing of the A and B input highways. Inputs AS(0) and AS(1) are logically the same. Inputs BS(0) and BS(1) are also logically the same.

When input M170 is HI, both AND gates are inactive making gating modifiers G1 and G3 active. G1 gates the complement of B (active HI) through the function. G3 gates the true state of A (active LO) through the function. When M170 is LO, the signal on pins AS(0,1) controls the state of the A highway and the signal on pins BS(0,1) controls the state of the B highway.

When the top AND gate is active $[M170\ LO\ and\ AS(0,1)\ LO]\ G4$ gates the complement of A through the function.

When the bottom AND gate is active $[M170\ LO\ and\ BS(0,1)\ LO]\ G2$ gates the true state of B through the function.

Enable Network

The enable output (NENA) is a group enable and is active (HI) when there is a 00, 10, or 01 combination in each bit position of the A and B operands. The 8-Bit signal from the ALU Control controls the number of bits in the A and B operands checked for the enable condition.

When the 8-Bit signal is LO, V is inactive and the Enable Network checks all 8 bits. When the 8-Bit signal is HI, V is active and forces an enable condition in the top 4 bits.

ALU

The A and B highways enter the ALU where they are each weighted binarily 1-128 and designated as operands A and B respectively. The carry input enters the ALU active HI, from pins CARYN(0,1), is weighted a binary 1 and designated as operand C.

The ALU produces the summation of A, B, and C and this result is weighted binarily 1-128. The most-significant 4 bits of the result are undefined when gating modifier Gl is active. Gl is active when the 8-Bit signal is HI.

The 8-bit result output highway passes through a gate on the way to the output pins. The Gate Output signal, when LO, gates the result to the output pins. Pins R(0-7) are active LO outputs. Pin NR7 is an active HI copy of the least-significant bit.

The ALU has a generate output (NGEN) which is HI when gating modifier G2 is active and the summation of A and B is less than 255 or when G1 is active and the summation of the least-significant 4 bits of A and B are less than 15.

Carry Network

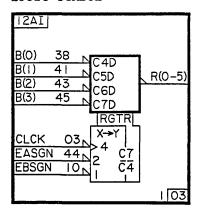
The signal entering pin NGRl is an active HI (+) signal.

Outputs COUT(0,1) are LO and NCOUT is HI when the following equation is active: Generate OR (Enable and NGR1).

Output CAROT is LO when the following equation is active: Generate OR (Minus One AND Enable).

12AI-1 MUX/Register.

LOGIC SYMBOL



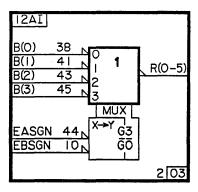
BIAS LØ = SEL, NFØR BIAS HI = CARYN(O,I)

OPERATIONAL DESCRIPTION

Pins EASGN, EBSGN, and clock on pin CLCK are translated to control the mux/register. Translations of 0-3 cause the register to hold.

Translations of 4-7 clock data into the register from pins [B(0-3)] respectively. The register outputs five copies of the selected data (R0-5).

60458120 B



BIAS LØ = SEL, CLK BIAS HI = CARYN(O,I), NFØR

OPERATIONAL DESCRIPTION

Pins EASGN and EBSGN are translated to control the mux.

Translations of 0-3 select data from pins B(0-3) respectively.

The mux outputs five copies of the selected data (R0-5).

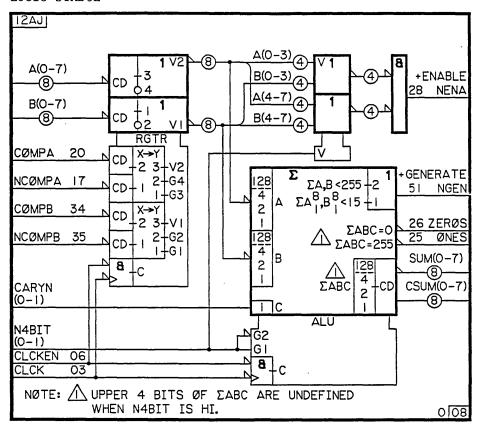
12AJ

DIN	DEAL	VIRT
PIN NAME	REAL PIN	PIN
A(0)	18	V01
A(1)	15	V02
A(2) A(3)	12 09	V03 V04
A(4)	22	V05
A(5)	16	V06
A(6)	11	V07
A(7)	10 20	V08
B(0) B(1)	36 37	V09 V10
B(2)	42	V11
B(3)	43	V12
B(4)	32 38	V13 V14
B(5) B(6)	30 41	V 14 V15
B(7)	44	V16
CARYN(•	V21
CARYN(1	1) 27 03	V35 V22
CLCKEN		V24
COMPA	20	V17
COMPB	34	V19
LTCHOP N4BIT(0)	52 48	V38 V37
N4BIT(1)	01	V36
NCOMPA	17	V18
NCOMPB NFORCE	35 08	V20 V23
CSUM(0)	21	V41
CSUM(1)	24	V42
CSUM(2)	30	V43
CSUM(3)	31 05	V44
CSUM(4)	05 04	V45 V46
CSUM(6)	50	V47
CSUM(7)	47	V48
NENA NGEN	28 51	V34 V33
ONES	25	V40
SUM(0)	19	V25
SUM(1)	23	V26
SUM(2) SUM(3)	29 33	V27 V28
SUM(4)	07	V29
SUM(5)	02	V30
SUM(6) SUM(7)	49 45	V31 V32
ZEROS	26	V32

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12AJ-0 Eight or Four-Bit Adder with Input and Output Registers.

LOGIC SYMBOL



BIAS LØ = NFØRCE, LTCHØP BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Input Register and Complement Network

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the A and B highways and complement controls (COMPA, NCOMPA, COMPB, and NCOMPB) into the input registers.

The outputs from the COMPA and NCOMPA registers are translated to control gating $\,$ modifiers G3 and G4 and OR modifier V2.

A translation of 0 activates no modifiers. This causes the A outputs from the complement network to equal zero because data is not gated out of the input register.

A translation of 1 activates gating modifier G3 which gates the true state of the A input register to the output of the complement network.

60458120 B 1 of 2

12AJ-0 (Cont'd)

A translation of 2 activates gating modifier G4 which gates the complement of the A input register to the output of the complement network.

A translation of 3 activates OR modifier V2 which forces the A complement network outputs to ones (LO).

The output from the COMPB and NCOMPB input registers are translated to control gating modifiers G1 and G2 and OR modifier V1 in the same manner as COMPA and NCOMPA control G3, G4, and V2 respectively.

Enable Network

The enable output (NENA) is a group enable and is active (HI) when there is a 00, 10, or 01 combination in each bit position of the A and B operands. The N4BIT input controls the number of bits in the A and B operands checked for the enable condition.

Input pins N4BIT(0,1) are both connected to the same input signal.

When N4BIT is LO, OR modifier V is inactive and the enable network checks all 8 bits. When N4BIT is HI, V is active and forces an enable condition in the top 4 bits.

ALU

The A and B highways enter the ALU where they are each weighted binarily 1-128 and designated as operands A and B respectively. The carry input enters the ALU on pins CARYN(0,1), is weighted a binary 1, and designated as operand C.

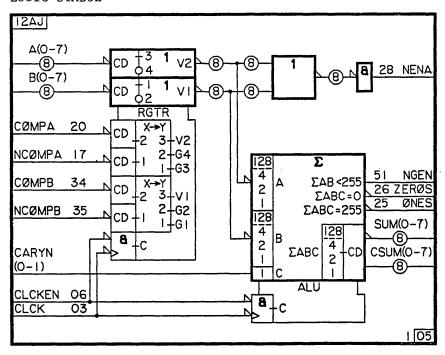
The ALU produces the summation of A, B, and C and this result is weighted binarily 1-128. The most significant 4 bits of the result are undefined when gating modifier Gl is active. Gl is active when N4BIT is HI.

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the result into the output register. SUM(0-7) are active LO result outputs, CSUM(0-7) are active HI result outputs.

Output NGEN is a group generate output and is HI when gating modifier G2 is active and the summation of A and B is less than 255 or when G1 is active and the summation of the least-significant 4 bits of A and B are less than 15.

Output ZEROS is LO when the summation of A, B, and C is equal to O.

Output ONES is LO when the summation of A, B, and C is equal to 255.



BIAS LØ = NFØRCE, N4BIT(O-1), LTCHØP

BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Input Register and Complement Network

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the A and B highways and complement controls (COMPA, NCOMPA, COMPB, and NCOMPB) into the input registers.

The outputs from the COMPA and NCOMPA registers are translated to control gating $\,$ modifiers G3 and G4 and OR modifier V2.

A translation of 0 activates no modifiers. This causes the A outputs from the complement network to equal zero because data is not gated out of the input register.

A translation of l activates gating modifier G3 which gates the true state of the A input register to the output of the complement network.

A translation of 2 activates gating modifier G4 which gates the complement of the A input register to the output of the complement network.

A translation of 3 activates OR modifier V2 which forces the A complement network outputs to ones (LO).

12AJ-1 (Cont'd)

The output from the COMPB and NCOMPB input registers are translated to control gating modifiers G1 and G2 and OR modifier V1 in the same manner as COMPA and NCOMPA control G3, G4, and V2 respectively.

Enable Network

The enable output (NENA) is a group enable and is active (HI) when there is a 00, 10, or 01 combination in each bit position of the A and B operands.

ALU .

The A and B highways enter the ALU where they are each weighted binarily 1-128 and designated as operands A and B respectively. The carry input enters the ALU on pins CARYN(0,1), is weighted a binary 1, and designated as operand C.

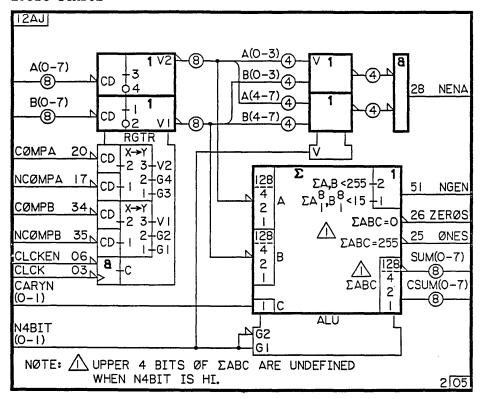
The ALU produces the summation of A, B, and C and this result is weighted binarily 1-128.

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the result into the output register. SUM(0-7) are active LO result outputs, CSUM(0-7) are active HI result outputs.

Output NGEN is a group generate output and is HI when the summation of A and B is less than 255.

Output ZEROS is LO when the summation of A, B, and C is equal to zero.

Output ONES is LO when the summation of A, B, and C is equal to 255.



BIAS LØ = NFØRCE BIAS HI = LTCHØP

OPERATIONAL DESCRIPTION

Input Register and Complement Network

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the A and B highways and complement controls (COMPA, NCOMPA, COMPB, and NCOMPB) into the input registers.

The outputs from the COMPA and NCOMPA registers are translated to control gating $\,$ modifiers G3 and G4 and OR modifier V2.

A translation of 0 activates no modifiers. This causes the A outputs from the complement network to equal zero because data is not gated out of the input register.

A translation of l activates gating modifier G3 which gates the true state of the A input register to the output of the complement network.

A translation of 2 activates gating modifier G4 which gates the complement of the A input register to the output of the complement network.

A translation of 3 activates OR modifier V2 which forces the A complement network outputs to ones (LO).

12AJ-2 (Cont'd)

The output from the COMPB and NCOMPB input registers are translated to control gating modifiers G1 and G2 and G3 modifier G3, G4, and G3 respectively.

Enable Network

The enable output (NENA) is a group enable and is active (HI) when there is a 00, 10, or 01 combination in each bit position of the A and B operands. The N4BIT input controls the number of bits in the A and B operands checked for the enable condition.

Input pin N4BIT(0,1) are both connected to the same input signal.

When N4BIT is LO, OR modifier V is inactive and the enable network checks all 8 bits. When N4BIT is HI, V is active and forces an enable condition in the top 4 bits.

ALU

The A and B highways enter the ALU where they are each weighted binarily 1-128 and designated as operands A and B respectively. The carry input enters the ALU on pins CARYN(0,1), is weighted a binary 1, and designated as operand C.

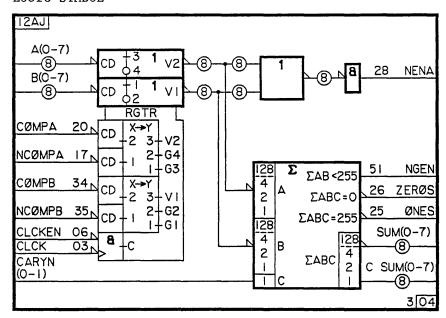
The ALU produces the summation of A, B, and C and this result is weighted binarily 1-128. The most significant 4 bits of the result are undefined when gating modifier Gl is active. Gl is active when N4BIT is HI.

SUM(0-7) are active LO result outputs, CSUM(0-7) are active HI result outputs.

Output NGEN is a group generate output and is HI when gating modifier G2 is active and the summation of A and B is less than 255 or when G1 is active and the summation of the least-significant 4 bits of A and B are less than 15.

Output ZEROS is LO when the summation of A, B, and C is equal to zero.

Output ONES is LO when the summation of A, B, and C is equal to 255.



BIAS LØ = NFØRCE, N4BIT(0-1) BIAS HI = LTCHØP

OPERATIONAL DESCRIPTION

Input Register and Complement Network

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the A and B highways and complement controls (COMPA, NCOMPA, COMPB, and NCOMPB) into the input registers.

The outputs from the COMPA and NCOMPA registers are translated to control gating modifiers G3 and G4 and OR modifier V2.

A translation of 0 activates no modifiers. This causes the A outputs from the complement network to equal zero because data is not gated out of the input register.

A translation of 1 activates gating modifier G3 which gates the true state of the A input register to the output of the complement network.

A translation of 2 activates gating modifier G4 which gates the complement of the A input register to the output of the complement network.

A translation of 3 activates OR modifier V2 which forces the A complement network outputs to ones (LO).

12AJ-3 (Cont'd)

The output from the COMPB and NCOMPB input registers are translated to control gating modifiers G1 and G2 and G3 modifier G3, G4, and G3 respectively.

Enable Network

The enable output (NENA) is a group enable and is active (HI) when there is a 00, 10, or 01 combination in each bit position of the A and B operands.

ALU

The A and B highways enter the ALU where they are each weighted binarily 1-128 and designated as operands A and B respectively. The carry input enters the ALU on pins CARYN(0,1), is weighted a binary 1, and designated as operand C.

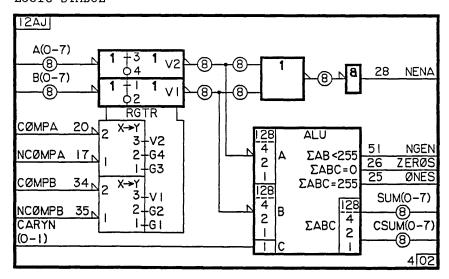
The ALU produces the summation of A, B, and C and this result is weighted binarily 1-128.

SUM(0-7) are active LO result outputs, CSUM(0-7) are active HI result outputs.

Output NGEN is a group generate output and is HI when the summation of A and B is less than 255.

Output ZEROS is LO when the summation of A, B, and C is equal to zero.

Output ONES is LO when the summation of A, B, and C is equal to 255.



BIAS LØ = N4BIT(O-I), LTCHØP, CLCK, CLCKEN BIAS HI = NFØRCE

OPERATIONAL DESCRIPTION

Complement Network

The COMPA and NCOMPA inputs are translated to control gating modifiers G3 and G4 and OR modifier V2.

A translation of 0 activates no modifiers. This causes the A outputs from the complement network to equal zero because data is not gated out through the network.

A translation of l activates gating modifier G3 which gates the true state of the A input highway to the output of the complement network.

A translation of 2 activates gating modifier G4 which gates the complement of the A input highway to the output of the complement network.

A translation of 3 activates OR modifier V2 which forces the A complement network outputs to ones (LO).

The COMPB and NCOMPB inputs are translated to control gating modifiers G1 and G2 and OR modifier V1 in the same manner as COMPA and NCOMPA control G3, G4, and V2 respectively.

Enable Network

The enable output (NENA) is a group enable and is active (HI) when there is a 00, 10, or 01 combination in each bit position of the A and B operands.

12AJ-4 (Cont'd)

ALU

The A and B highways enter the ALU where they are each weighted binarily 1-128 and designated as operands A and B respectively. The carry input enters the ALU on pins CARYN(0,1), is weighted a binary 1, and designated as operand C.

The ALU produces the summation of A, B, and C and this result is weighted binarily 1-128.

SUM(0-7) are active LO result outputs, CSUM(0-7) are active HI result outputs.

Output NGEN is a group generate output and is ${\tt HI}$ when the summation of A and B is less than 255.

Output ZEROS is LO when the summation of A, B, and C is equal to zero.

Output ONES is LO when the summation of A, B, and C is equal to 255.

12AM

PIN NAME	REAL PIN	VIRT PIN
A(0)	16	V01
A(1) A(2)	08 31	V09 V17
A(2) A(3)	51	V17 V25
B(0)	20	V02
B(1) B(2)	09 33	V10 V18
B(3)	48	V26
BS C(0)	12 17	V38
C(0) C(1)	17 06	V03 V11
C(2)	29	V19
C(3) CLCK	49 03	V27 V42
D(0)	21	V04
D(1)	11	V12
D(2) D(3)	36 47	V20 V28
E(0)	22	V05
E(1)	01 24	V13
E(2) E(3)	34 45	V21 V29
ENA	37	V40
F(0) F(1)	23 10	V06 V14
F(2)	32	V22
F(3) G(0)	44 18	V30 V07
G(0) G(1)	18 07	V07 V15
G(2)	38	V23
G(3) H(0)	43 19	V31 V08
H(1)	05	V16
H(2)	35	V24
H(3) NFORCE	46 02	V32 V41
OS(0)	25	V36
OS(1) PI	15 42	V37 V44
RS	52	V44 V39
S(0)	41	V35
S(1) S(2)	28 26	V33 V34
PO	27	V43
Z(0)	24 04	V45 V46
Z(1) Z(2)	30	V47
Z(3)	50	V48

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12AK

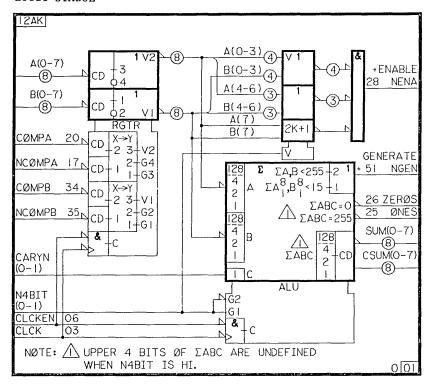
PIN	REAL	VIRT
NAME	PIN	PIN
A(0) A(1)	18 15	V01 V02
A(2)	12	V03
A(3)	09	V04
A(4) A(5)	22 16	V05 V06
A(6) A(7)	11 10	V07 V08
B(0)	36	V09
B(1)	37	V10 V11
B(2) B(3)	42 43	V11
B(4)	32	V13
B(5) B(6)	38 41	V14 V15
B(7)	44	V16
CARYN(0) CARYN(1)	46 27	V21 V35
CLCK	03	V22
CLCKEN COMPA	06 20	V24 V17
COMPB	20 34	V19
N4BIT(0)	48	V37
N4BIT(1) NCOMPA	01 17	V36 V18
NCOMPB	35	V20
NFORCE CSUM(0)	08 21	V23 V41
CSUM(1)	24	V42
CSUM(2) CSUM(3)	30 31	V43 V44
CSUM(4)	05	V45
CSUM(5) CSUM(6)	04 50	V46 V47
CSUM(7)	47	V47
NENA	28	V34
NGEN ONES	51 25	V33 V40
SUM(0)	19	V25
SUM(1) SUM(2)	23 29	V26 V27
SUM(3)	33	V28
SUM(4) SUM(5)	07 02	V29 V30
SUM(6)	49	V31
SUM(7) ZEROS	45 26	V32 V39

60458120 F 1 of 1 ●

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12AK-0 Eight or Four-Bit Adder with Input and Output Registers.

LOGIC SYMBOL



BIAS LØ = NFØRCE BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Input Register and Complement Network

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the A and B highways and complement controls (COMPA, NCOMPA, COMPB, and NCOMPB) into the input registers.

The outputs from the COMPA and NCOMPA registers are translated to control gating $\,$ modifiers G3 and G4 and OR modifier V2.

A translation of 0 activates no modifiers. This causes the A outputs from the complement network to equal zero because data is not gated out of the input register.

A translation of 1 activates gating modifier G3 which gates the true state of the A input register to the output of the complement network.

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12AK-0 (Cont'd)

A translation of 2 activates gating modifier G4 which gates the complement of the A input register to the output of the complement network.

A translation of 3 activates OR modifier V2 which forces the A complement network outputs to ones (LO).

The output from the COMPB and NCOMPB input registers are translated to control gating modifiers G1 and G2 and G3 modifier G1 in the same manner as COMPA and NCOMPA control G3, G4, and G3 respectively.

Enable Network

The enable output (NENA) is a group enable and is active (HI) when there is a 00, 10, or 01 combination in each bit position of A(0-6) and B(0-6) along with a 10 or 01 combination in bit position A(7) and B(7). The N4BIT input controls the number of bits in the A and B operands checked for the enable condition.

Input pins N4BIT(0,1) are both connected to the same input signal.

When N4BIT is LO, OR modifier V is inactive and the enable network checks all 8 bits. When N4BIT is HI, V is active and forces an enable condition in the top 4 bits.

ALU

The A and B highways enter the ALU where they are each weighted binarily 1-128 and designated as operands A and B respectively. The carry input enters the ALU on pins CARYN(0,1), is weighted a binary 1, and designated as operand C.

The ALU produces the summation of A, B, and C and this result is weighted binarily 1-128. The most significant 4 bits of the result are undefined when gating modifier Gl is active. Gl is active when N4BIT is HI.

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the result into the output register. SUM(0-7) are active LO result outputs, CSUM(0-7) are active HI result outputs.

Output NGEN is a group generate output and is HI when gating modifier G2 is active and the summation of A and B is less than 255 or when G1 is active and the summation of the least-significant 4 bits of A and B are less than 15.

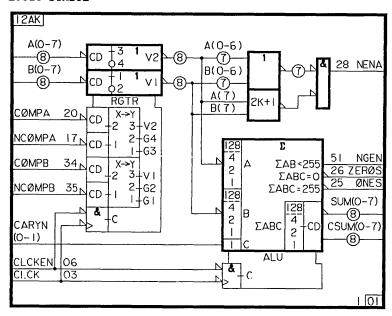
Output ZEROS is LO when the summation of A, B, and C is equal to O.

Output ONES is LO when the summation of A, B, and C is equal to 255.

60458120 F 2 of 2

12AK-1 Eight-Bit Adder with Input and Output Registers.

LOGIC SYMBOL



BIAS LØ = NFØRCE, N4BIT(O-1)

BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Input Register and Complement Network

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the A and B highways and complement controls (COMPA, NCOMPA, COMPB, and NCOMPB) into the input registers.

The outputs from the COMPA and NCOMPA registers are translated to control gating $\,$ modifiers G3 and G4 and OR modifier V2.

A translation of 0 activates no modifiers. This causes the A outputs from the complement network to equal zero because data is not gated out of the input register.

A translation of l activates gating modifier G3 which gates the true state of the Λ input register to the output of the complement network.

A translation of 2 activates gating modifier G4 which gates the complement of the A input register to the output of the complement network.

A translation of 3 activates OR modifier V2 which forces the A complement network outputs to ones (LO).

60458120 F

12AK-1 (Cont'd)

The output from the COMPB and NCOMPB input registers are translated to control gating modifiers G1 and G2 and OR modifier V1 in the same manner as COMPA and NCOMPA control G3, G4, and V2 respectively.

Enable Network

The enable output (NENA) is a group enable and is active (HI) when there is a 00, 10, or 01 combination in each bit position of A(0-6) and B(0-6) along with a 10 or 01 combination in bit position A(7) and B(7).

ALU

The A and B highways enter the ALU where they are each weighted binarily 1-128 and designated as operands A and B respectively. The carry input enters the ALU on pins CARYN(0,1), is weighted a binary 1, and designated as operand C.

The ALU produces the summation of A, B, and C and this result is weighted binarily 1-128.

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the result into the output register. SUM(0-7) are active LO result outputs, CSUM(0-7) are active HI result outputs.

Output NGEN is a group generate output and is HI when the summation of A and B is less than $255\, \mbox{.}$

Output ZEROS is LO when the summation of A, B, and C is equal to zero.

Output ONES is LO when the summation of A, B, and C is equal to 255.

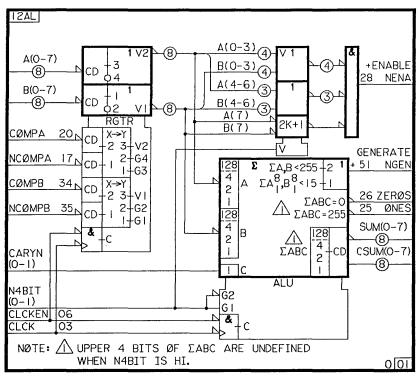
12AL

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	18	V01
A(1)	15	V02
A(2)	12	V03
A(3)	09	V04
A(4)	22	V05
A(5)	16	V06
A(6)	11	V07
A(7)	10	V08
B(0)	36	V09
B(1)	37	V10
B(2)	42	V11
B(3)	43	V12
B(4)	32	V13
B(5)	38	V14
B(6)	41	V15
B(7)	44	V16
CARYN(0)	46	V21
CARYN(1)	27	V35
CLCK	03	V22
CLCKEN	06	V24
COMPA	20	V17
COMPB	34	V19
N4BIT(0)	48	V37
N4BIT(1)	01	V36
NCOMPA	17	V18
NCOMPB	35	V20
NFORCE	08	V23
CSUM(0)	21	V41
CSUM(1)	24	V42
CSUM(2)	30	V43
CSUM(3)	31	V44
CSUM(4)	05	V45
CSUM(5)	04	V46
CSUM(6)	50	V47
CSUM(7)	47	V48
NENA	28	V34
NGEN	51	V33
ONES	25	V40
SUM(0)	19	V25
SUM(1)	23	V26
SUM(2)	29	V27
SUM(3)	33	V28
SUM(4)	07	V29
SUM(5)	02	V30
SUM(6)	49	V31
SUM(7)	45	V32
ZEROS	26	V39

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12AL-O Eight or Four-Bit Adder with Input and Output Registers.

LOGIC SYMBOL



BIAS LØ = NFØRCE BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Input Register and Complement Network

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the A and B highways and complement controls (COMPA, NCOMPA, COMPB, and NCOMPB) into the input registers.

The outputs from the COMPA and NCOMPA registers are translated to control gating $\,$ modifiers G3 and G4 and OR modifier V2.

A translation of 0 activates no modifiers. This causes the A outputs from the complement network to equal zero because data is not gated out of the input register.

A translation of 1 activates gating modifier G3 which gates the true state of the A input register to the output of the complement network.

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12AL-0 (Cont'd)

A translation of 2 activates gating modifier G4 which gates the complement of the A input register to the output of the complement network.

A translation of 3 activates OR modifier V2 which forces the A complement network outputs to ones (LO).

The output from the COMPB and NCOMPB input registers are translated to control gating modifiers G1 and G2 and OR modifier V1 in the same manner as COMPA and NCOMPA control G3, G4, and V2 respectively.

Enable Network

The enable output (NENA) is a group enable and is active (HI) when there is a 00, 10, or 01 combination in each bit position of A(0-6) and B(0-6) along with a 10 or 01 combination in bit position A(7) and B(7). The N4BIT input controls the number of bits in the A and B operands checked for the enable condition.

Input pins N4BIT(0,1) are both connected to the same input signal.

When N4BIT is LO, OR modifier V is inactive and the enable network checks all 8 bits. When N4BIT is HI, V is active and forces an enable condition in the top 4 bits.

ALU

The A and B highways enter the ALU where they are each weighted binarily 1-128 and designated as operands A and B respectively. The carry input enters the ALU on pins CARYN(0,1), is weighted a binary 1, and designated as operand C.

The ALU produces the summation of A, B, and C and this result is weighted binarily 1-128. The most significant 4 bits of the result are undefined when gating modifier Gl is active. Gl is active when N4BIT is HI.

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the result into the output register. SUM(0-7) are active LO result outputs, CSUM(0-7) are active HI result outputs.

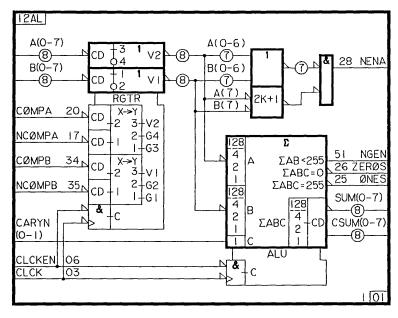
Output NGEN is a group generate output and is HI when gating modifier G2 is active and the summation of A and B is less than 255 or when G1 is active and the summation of the least-significant 4 bits of A and B are less than 15.

Output ZEROS is LO when the summation of A, B, and C is equal to O.

Output ONES is LO when the summation of A, B, and C is equal to 255.

12AL-1 Eight-Bit Adder with Input and Output Registers.

LOGIC SYMBOL



BIAS LØ = NFØRCE, N4BIT(O-1) BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Input Register and Complement Network

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the A and B highways and complement controls (COMPA, NCOMPA, COMPB, and NCOMPB) into the input registers.

The outputs from the COMPA and NCOMPA registers are translated to control gating $\,$ modifiers G3 and G4 and OR modifier V2.

A translation of 0 activates no modifiers. This causes the A outputs from the complement network to equal zero because data is not gated out of the input register.

A translation of 1 activates gating modifier G3 which gates the true state of the A input register to the output of the complement network.

A translation of 2 activates gating modifier G4 which gates the complement of the A input register to the output of the complement network.

A translation of 3 activates OR modifier V2 which forces the A complement network outputs to ones (LO).

12AL-1 (Cont'd)

The output from the COMPB and NCOMPB input registers are translated to control gating modifiers G1 and G2 and OR modifier V1 in the same manner as COMPA and NCOMPA control G3, G4, and V2 respectively.

Enable Network

The enable output (NENA) is a group enable and is active (HI) when there is a 00, 10, or 01 combination in each bit position of A(0-6) and B(0-6) along with a 10 or 01 combination in bit position A(7) and B(7).

ALU

The A and B highways enter the ALU where they are each weighted binarily 1-128 and designated as operands A and B respectively. The carry input enters the ALU on pins CARYN(0,1), is weighted a binary 1, and designated as operand C.

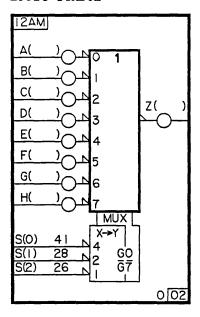
The ALU produces the summation of A, B, and C and this result is weighted binarily 1-128.

Clock on pin CLCK and an enable signal on pin CLCKEN are ANDed together to control clock modifier C. C clocks the result into the output register. SUM(0-7) are active LO result outputs, CSUM(0-7) are active HI result outputs.

Output NGEN is a group generate output and is HI when the summation of A and B is less than $255_{\:\raisebox{1pt}{\text{\circle*{1.5}}}}$

Output ZEROS is LO when the summation of A, B, and C is equal to zero.

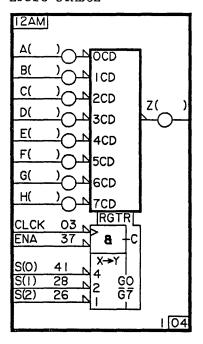
Output ONES is LO when the summation of A, B, and C is equal to 255.



BIAS LØ = NØNE BIAS HI = ØS(O-I)

OPERATIONAL DESCRIPTION

Pins S(0-2) are translated to select one of eight input highways to output highway Z. Translations of 0-7 select input highways A-H respectively.



BIAS LØ = ØS(1), NFØRCE BIAS HI = BS, ØS(0)

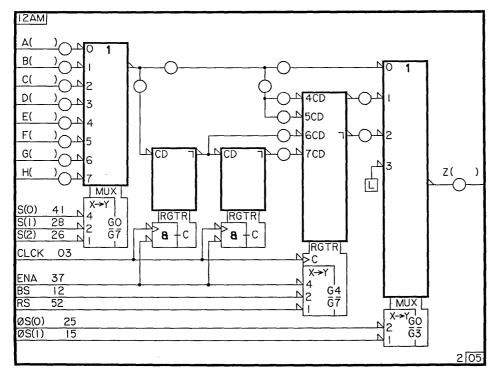
OPERATIONAL DESCRIPTION

Pins S(0-2) are translated to select one of eight input highways to the input of the register. Translations of 0-7 select input highways A-H respectively.

Clock on pin CLCK and an enable signal on pin ENA are ANDed to control clock modifier C. When C is active it clocks the selected highway into the register.

12AM-2 Mux/Variable Length Buffer.

LOGIC SYMBOL



BIAS LØ = NFØRCE BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Input Mux

Pins S(0-2) are translated to select one of eight input highways to the mux output highway. Translations of 0-7 select input highways A-H respectively.

Buffer Ranks 1 and 2

Clock on pin CLCK and an enable signal on pin ${\tt ENA}$ are ${\tt ANDed}$ to control clock modifier C in each of the first two buffer ranks.

When C is active, it clocks the input mux data into the first buffer rank. The output is delayed until clock modifier C becomes inactive 2.5 ns following the LO transition of clock. Thus the following clock clocks the data from rank 1 into rank 2. The output of rank 2 is also delayed until C becomes inactive.

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12AM-2 (Cont'd)

Buffer Rank 3

Buffer rank 3 is a three-input mux to a register. Pins BS and RS select one of three input highways to the input of the register. The enable signal on pin ENA enables the selection. Note that translations of 0-3 (ENA HI) activate no gating modifiers and therefore place zeros at the input to the register.

Translations of 4 and 5 select data from the input mux.

Translations of 6 and 7 select data from buffer ranks 1 and 2 respectively.

Clock on pin CLCK controls clock modifier C which clocks the selected data into the register.

The register has two outputs. The top output is not delayed, i.e., its output follows the content of the register with no delay. The bottom outputs are delayed until clock modifier C becomes inactive.

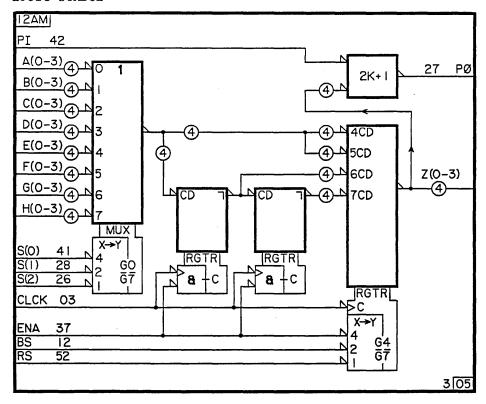
Output Mux

Pins OS(0,1) are translated to select one of four highways to output highway Z.

A translation of O selects data from the input mux.

Translations of 1 and 2 select non-delayed and delayed outputs respectively from buffer rank 3.

A translation of 3 selects LOs.



BIAS LØ = \emptyset S(1), NF \emptyset RCE BIAS HI = \emptyset S(0)

OPERATIONAL DESCRIPTION

Input Mux

Pins S(0-2) are translated to select one of eight input highways to the mux output highway. Translations of 0-7 select input highways A-H respectively.

Buffer Ranks 1 and 2

Clock on pin CLCK and an enable signal on pin ENA are ANDed to control clock modifier C in each of th first two buffer ranks.

When C is active it clocks the input mux data into the first buffer rank. The output is delayed until clock modifier C becomes inactive 2.5 ns following the LO transition of clock. Thus the following clock clocks the data from rank 1 into rank 2. The output of rank 2 is also delayed until C becomes inactive.

12AM-3 (Cont'd)

Buffer Rank 3

Buffer rank 3 is a three-input mux to a register. Pins BS and RS select one of three input highways to the input of the register. The enable signal on pin ENA enables the selection. Note that translations of 0-3 (ENA HI) activate no gating modifiers and therefore place zeros at the input to the register.

Translations of 4 and 5 select data from the input mux.

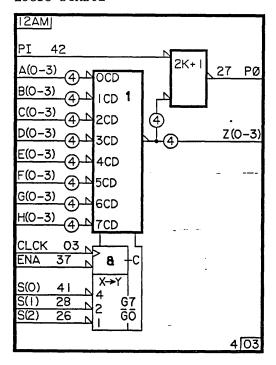
Translations of 6 and 7 select data from buffer ranks 1 and 2 respectively.

Clock on pin CLCK controls clock modifier C which clocks the selected data into the register.

Parity

Output PO is LO when an odd number of its five inputs are LO.

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BIAS LØ = ØS(1), NFØRCE BIAS HI = BS, ØS(0)

OPERATIONAL DESCRIPTION

Mux/Register

Pins S(0-2) are translated to select one of eight input highways to the mux output highway. Translations of 0-7 select input highways A-H respectively.

Clock on pin CLCK and an enable signal on pin ENA are ANDed to control clock modifier C in each of the first two buffer ranks.

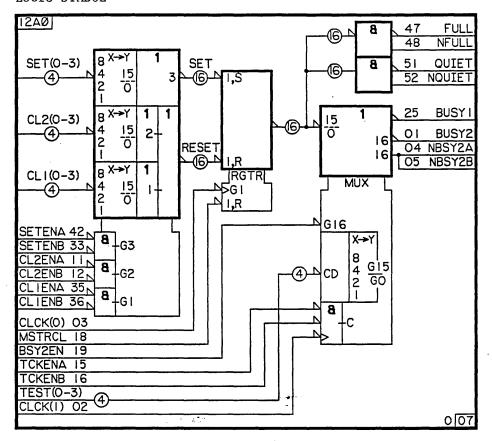
Parity

Output PO is LO when an odd number of its five inputs are LO.

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PIN NAME	REAL PIN	VIRT
BSY2EN	19	V23
CL1(0)	27	V09
CL1(1)	28	V10
CL1(2)	34	V11
CL1(3)	38	V12
CL1ENA	35	V21
CL1ENB	36	V22
CL2(0)	41	V05
CL2(1)	46	V06
CL2(2)	20	V07
CL2(3)	17	V08
CL2ENA	11	V19
CL2ENB	12	V20
CLCK(0)	03	V27
CLCK(1)	02	V28
MSTRCL	18	V31
NFORCE(NFORCE(SET(0) SET(1)		V29 V30 V01 V02
SET(2)	29	V03
SET(3)	37	V04
SETENA	42	V17
SETENB	33	V18
TEST(0)	22	V13
TEST(1)	08	V14
TEST(2)	26	V15
TEST(3)	23	V16
TICKENA	15	V25
TCKENB	16	V26
BUSY1	25	V35
BUSY2	01	V36
FULL	47	V47
NBSY2A	04	V37
NBSY2B	05	V38
NFULL	48	V48
NQUIET QUIET TSTDC1(0 TSTDC1(1	52 51 0) 07	V34 V33 V39 V40
TSTDC1(2 TSTDC1(3 TSTDC2(0 TSTDC2(1	3) 50 3) 24	V41 V42 V43 V44
TSTDC2(2 TSTDC2(3		V45 V46

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BIAS LØ = NFØRCE(O-1) BIAS HI = NØNE

OPERATIONAL DESCRIPTION

The 12AO-O array contains 16 RS-type flip-flops. Each clock period, control codes may selectively set one flip-flop and clear one or two other flip-flops. An output mux selects any one of the 16 flip-flops for output. Other functions test the 16 flip-flops for all ones and all zeros.

RS Flip-Flops

The RS flip-flops are the center function in the symbol. Each of the 16 RS flip-flops has an individual set input (top highway) and a reset input (bottom highway). All 16 flip-flops clear when reset modifier R in the common control block is active. Clock on pin CLCK(0) controls gating modifier Gl which must be active to set, reset, or master clear the flip-flops.

12A0-0 (Cont'd)

A flip-flop sets when its set input is LO and Gl is active. A flip-flop clears when its reset input is LO and Gl is active or the master clear input (pin MSTRCL) is LO and Gl is active.

When a flip-flop tries to set and reset at the same time, its output is unknown.

Set and Clear Selection

The SET(0-3) inputs are translated to make one of 16 set inputs LO. Gating modifier G3 gates the selection to the RS flip-flops. G3 is the result of a two-input AND gate in the common control block.

Input highways CL2(0-3) and CL1(0-3) are each translated to make one of 16 reset inputs LO. Gating modifiers G1 and G2 gate the CL1 and CL2 selections, respectively, to the RS flip-flops. G1 and G2 are each the result of two-input AND gates in the common control block.

Two RS flip-flops reset with the same clock pulse when the CL1 and CL2 codes are different and both selections are gated to the RS flip-flops.

Output Mux

Clock on pin CLCK(1) and inputs TCKENA and TCKENB are ANDed to control clock modifier C. C clocks the output mux select code [inputs TEST(0-3)] into a register in the common control block. The output of the register is translated to select one of 16 inputs, one from each RS flip-flop.

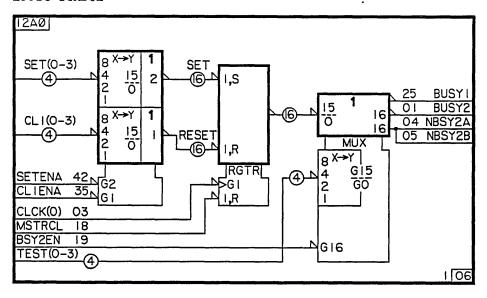
Output pin BUSYl is an ungated active LO output. Gating modifier G16 gates the selection out of the BUSY2 output (active LO) and the NBSY2A and NBSY2B outputs (active HI). The BSY2EN input controls G16.

Full and Quiet Test

The FULL output is LO and the NFULL output is HI when all 16 RS flip-flops are set.

The QUIET output is LO and the NQUIET output is HI when all 16 RS flip-flops are clear.

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BIAS LØ = NFØRCE(O), SETENB, CLIENB, TCKENA, CLCK(I), TCKENB

BIAS HI = CLZENA, NFØRCE(I)

OPERATIONAL DESCRIPTION

The 12AO-1 array contains 16 RS-type flip-flops. Each clock period, control codes may selectively set one flip-flop and clear one other flip-flop. An output mux selects any one of the 16 flip-flops for output.

RS Flip-Flops

The RS flip-flops are the center function in the symbol. Each of the 16 RS flip-flops has an individual set input (top highway) and a reset input (bottom highway). All 16 flip-flops clear when reset modifier R in the common control block is active. Clock on pin CLCK(0) controls gating modifier Gl which must be active to set, reset, or master clear the flip-flops.

A flip-flop sets when its set input is LO and Gl is active. A flip-flop clears when its reset input is LO and Gl is active or the master clear input (pin MSTRCL) is LO and Gl is active.

When a flip-flop tries to set and reset at the same time, its output is unknown.

Set and Clear Selection

The SET(0-3) inputs are translated to make one of 16 set inputs LO. Gating modifier G2 gates the selection to the RS flip-flops. The SETENA input controls G2.

The CL1(0-3) inputs are translated to make one of 16 reset inputs LO. Gating modifier Gl gates the selection to the RS flip-flops. The CL1ENA input controls Gl.

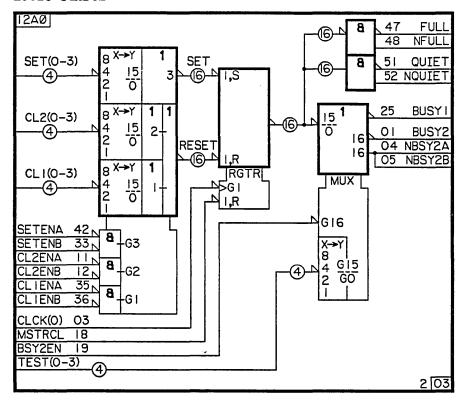
12AO-1 (Cont'd)

Output Mux

The TEST(0-3) inputs are translated to select one of 16 inputs; one from each RS flip-flop.

Output pin BUSYl is an ungated active LO output. Gating modifier G16 gates the selection out of the BUSY2 output (active LO) and the NBSY2A and NBSY2B outputs (active HI). The BSY2EN input controls G16.

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BIAS LØ = NFØRCE(O), TCKENA, TCKENB, CLCK(I)

BIAS HI = NFØRCE(I)

OPERATIONAL DESCRIPTION

The 12AO-2 array contains 16 RS-type flip-flops. Each clock period, control codes may selectively set one flip-flop and clear one or two other flip-flops. An output mux selects any one of the 16 flip-flops for output. Other functions test the 16 flip-flops for all ones and all zeros.

RS Flip-Flops

The RS flip-flops are the center function in the symbol. Each of the 16 RS flip-flops has an individual set input (top highway) and a reset input (bottom highway). All 16 flip-flops clear when reset modifier R in the common control block is active. Clock on pin CLCK(0) controls gating modifier Gl which must be active to set, reset, or master clear the flip-flops.

12AO-2 (Cont'd)

A flip-flop sets when its set input is LO and Gl is active. A flip-flop clears when its reset input is LO and Gl is active or the master clear input (pin MSTRCL) is LO and Gl is active.

When a flip-flop tries to set and reset at the same time, its output is unknown.

Set and Clear Selection

The SET(0-3) inputs are translated to make one of 16 set inputs LO. Gating modifier G3 gates the selection to the RS flip-flops. G3 is the result of a two-input AND gate in the common control block.

Input highways CL2(0-3) and CL1(0-3) are each translated to make one of 16 reset inputs LO. Gating modifiers G1 and G2 gate the CL1 and CL2 selections, respectively, to the RS flip-flops. G1 and G2 are each the result of two-input AND gates in the common control block.

Two RS flip-flops reset with the same clock pulse when the CL1 and CL2 codes are different and both selections are gated to the RS flip-flops.

Output Mux

The TEST(0-3) inputs are translated to select one of 16 inputs; one from each RS flip-flop.

Output pin BUSY1 is an ungated active LO output. Gating modifier G16 gates the selection out of the BUSY2 output (active LO) and the NBSY2A and NBSY2B outputs (active HI). The BSY2EN input controls G16.

Full and Quiet Test

The FULL output is LO and the NFULL output is HI when all 16 RS flip-flops are set.

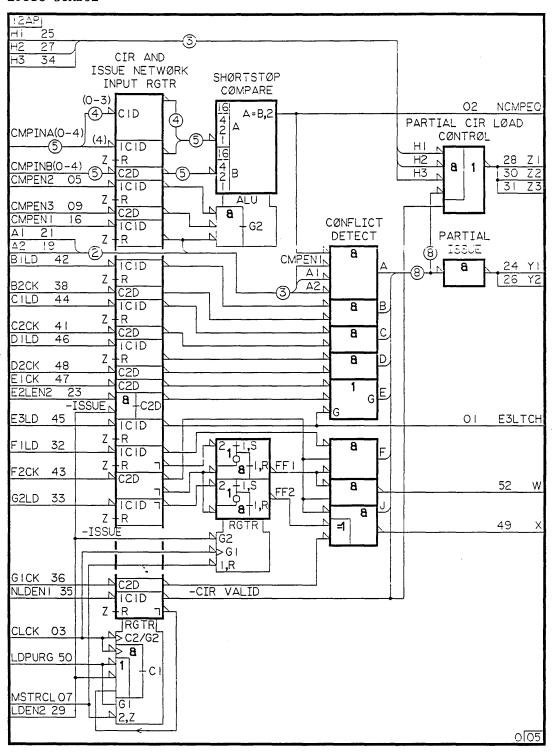
The QUIET output is LO and the NQUIET output is HI when all 16 RS flip-flops are clear.

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12AP

PIN	REAL	VIRT
NAME	PIN	PIN
A1	21	V15
A2	19	V16
B1LD	42	V17
B2CK	38	V18
C1LD	44	V19
C2CK	41	V20
CLCK	03	V39
CMPEN1	16	V11
CMPEN2 CMPEN3 CMPINA	09 (0) 22	V12 V13 V01 V02
CMPINA CMPINA CMPINA CMPINB((3) 06 (4) 20	V03 V04 V05 V06
CMPINB(CMPINB(CMPINB(CMPINB(2) 10 3) 04	V07 V08 V09 V10
D1LD	46	V21
D2CK	48	V22
E1CK	47	V24
E2LEN2	23	V25
E3LD	45	V26
F1LD	32	V27
F2CK	43	V28
G1CK	36	V30
G2LD	33	V31
H1	25	V32
H2	27	V33
H3	34	V34
LDEN2 LDPURG MSTRCL NFORCE	07	V36 V23 V37 V38
NLDEN1 S1 S2 E3LTCH	37 17	V35 V29 V14 V41
NCMPEO W X Y1		V40 V42 V43 V44
Y2	26	V45
Z1	28	V46
Z2	30	V47
Z3	31	V48

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BIAS LØ = NFØRCE BIAS HI = SI, S2

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12AP-0 (Cont'd)

OPERATIONAL DESCRIPTION

The 12AP-O contains a bit-slice of the Issue Network. The Issue Network holds and examines the next instruction and examines processor conditions such as functional unit, register, and result pipeline stage busies to determine whether or not there are conflicts with instructions already in process which will delay the issue of this next instruction.

The Current Instruction Register (CIR), in the Issue Network, holds the next instruction until there are no conflicts and the instruction issues, or the CIR is purged or master cleared.

The Issue Network Input Register, in the Issue Network, samples the processor conditions each clock period.

Parts of these two registers are interspersed down the left side of the symbol. Clock modifier Cl clocks data into the CIR. Clock modifier C2 clocks data into the Issue Network Input register.

Other parts of the Issue Network are the Shortstop Compare ALU (top center of the symbol), two status flip-flops (FF1 and FF2 in the lower center of the symbol), the Conflict Detect network (right center of the symbol), and the Partial CIR Load Control (upper right).

Current Instruction Register (CIR)

Normally the CIR holds valid control words (instructions) until there are no conflicts with instructions already in process. When there are no conflicts, the instruction issues and the CIR can load another control word. When the CIR does not contain a valid control word its control clocks it each clock period until a valid control word enters the CIR. When a valid control word enters the CIR, control stops the CIR clock and again waits for an issue.

Issue is one of three ways of starting the CIR clock while the CIR contains a valid control word. The other two are Purge CIR and Master Clear CCN.

The Purge CIR operation starts the CIR clock and blocks the CIR inputs thus clearing the register. The CIR control continues to clock the CIR until a valid control word enters the register.

The Master Clear CCN operation clears the CIR and again, the CIR control will start clocking the CIR each clock period until a valid control word enters the register.

CIR Control

The CIR is controlled by the Control Word Valid signal on input pin NLDEN1 (input to the bottom register function in the symbol), the Purge CIR signal on pin LDPURG, the Master Clear CCN signal on pin MSTRCL, the Issue signal on pin LDEN2, and clock on pin CLCK.

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12AP-0 (Cont'd)

CIR Operation

There are three conditions which activate the CIR clock modifier C1: CIR Valid signal is HI, Issue signal on input pin LDEN2 is LO, and the Purge CIR signal on input pin LDPURG is LO. This description assumes that each condition is active separately.

The HI state of the CIR Valid signal indicates that the CIR does not contain a valid control word. This signal is ORed with the Purge CIR and Issue signals and ANDed with clock. Thus as long as CIR Valid is HI, clock modifier Cl is active each time clock goes LO. When a valid control word is at the input to the CIR, the Control Word Valid signal on pin NLDENI is LO and the next active Cl sets the CIR Valid bit and clocks a valid control word into the CIR. The CIR Valid signals go LO and CM no longer enables Cl clocks.

The Issue signal on input pin LDEN2 can go LO only when the CIR contains a valid control word and there are no conflicts. When this signal is LO it activates the OR function in the common control block and is ANDed with clock. Thus when clock goes LO, Cl is active clocking new inputs into the CIR. The CIR Valid signal indicates whether or not the new CIR content is a valid control word.

When the Purge CIR signal is LO (input pin LDPURG) the OR function in the common control block is active and gating modifier G1 is inactive. G1 inactive blocks the inputs to most of the CIR. Thus when clock goes LO, C1 active will clear those CIR bits disabled by the inactive G1. Note that the top 4 CIR bits (inputs CMPINA (0-3)) do not have the G1 gate at the input to the CTYR. Therefore C1 active always loads the signals from CMPINA (0-3) into the register. Since the input to the CIR Valid bit (input NLDEN1) is gated by G1, the CIR Valid bit clears indicating that the CIR does not contain a valid control word.

Issue Network Input Register

Clock modifier C2 is active each time clock goes LO. The Issue Network Input Register therefore samples the processor conditions each clock period.

Shortstop Compare ALU

The Shortstop Compare ALU compares operand A X-Register type and number from the CIR with the X Register type and number of the Integer Unit (IGU) result at Result Pipeline (RPL) stage 3. The Compare determines whether or not a shortstop operation will resolve a conflict sooner than waiting for the conflicting instruction to complete.

Five bits each from the CIR and Issue Network Input Register enter the ALU where they are each weighted binarily 1 through 16 and designated as operands A and B respectively.

The ALU compares the A and B operands for equality and gating modifier G2 gates the active HI result out of the ALU to pin NCMPEQ and also to the top AND gate in the Conflict Detect Network.

The AND gate in the common control block of the ALU activates gating modifier G2 when all three inputs to the AND are L0.

12AP-0 (Cont'd)

All three input signals are shortstop enables. Two come from the CIR and the third comes from the Issue Network Input Register.

Status Flip-Flops

The status flip-flops, FF1 and FF2, are RS flip-flops with logic on the inputs to each which makes the set inputs override the reset inputs. When the OR function fed by the set input is active, it blocks the AND function fed by the reset input.

The equation for making set modifier S active for each flip-flop is:

Set input LO AND Issue input LO AND clock

The equation for making reset modifier R active for each flip-flop is:

Clear input LO AND (Set input HI OR Issue input HI) AND clock.

The flip-flops also have a common reset modifier in the common control block which is activated by the Master Clear CCN signal on pin MSTRCL ANDed with clock.

Conflict Detect

The Conflict Detect network is a set of gates which tests the content of the CIR, Issue Network Input Register, Shortstop Compare, Status flip-flops and individual input pins. When any gate is active, indicating a conflict, the active HI output disables the Partial Issue AND gate.

When the CIR Valid signal is HI, indicating that the content of the CIR is not valid, it disables the Partial Issue AND gate.

Outputs Yl and Y2 are both LO when there are no conflicts and the CIR contains a valid control word.

Partial CIR Load Control

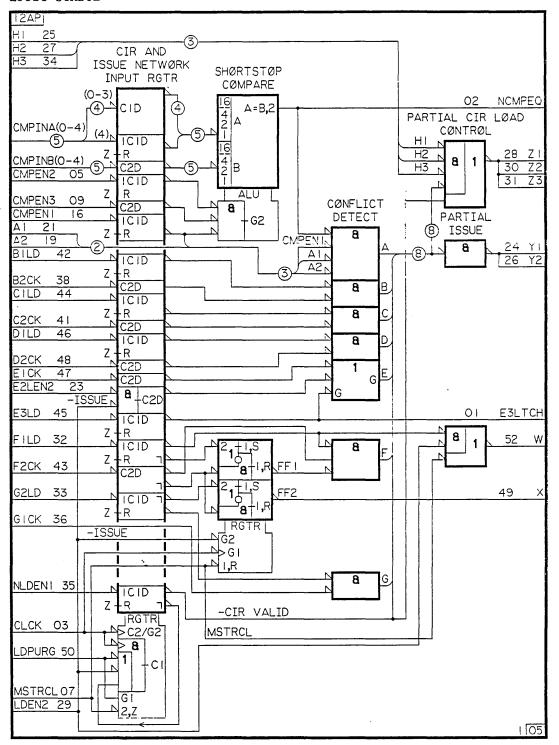
Outputs Z1-3 control the loading of those portions of the CIR not contained in the 12AP arrays.

Inputs H1-3 connect to Partial Issue outputs from other 12AP arrays.

Outputs Z1-3 are LO when the CIR Valid signal is HI OR inputs H1-3 are all LO AND there are no conflicts AND the CIR Valid signal is LO.

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BIAS LØ = S2. NFØRCE

RTAS HT = SI

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12AP-1 (Cont'd)

OPERATIONAL DESCRIPTION

The 12AP-1 contains a bit-slice of the Issue Network. The Issue Network holds and examines the next instruction and examines processor conditions such as functional unit, register, and result pipeline stage busies to determine whether or not there are conflicts with instructions already in process which will delay the issue of this next instruction.

The Current Instruction Register (CIR), in the Issue Network, holds the next instruction until there are no conflicts and the instruction issues, or the CIR is purged or master cleared.

The Issue Network Input Register, in the Issue Network, samples the processor conditions each clock period.

Parts of these two registers are interspersed down the left side of the symbol. Clock modifier Cl clocks data into the CIR. Clock modifier C2 clocks data into the Issue Network Input register.

Other parts of the Issue Network are the Shortstop Compare ALU (top center of the symbol), two status flip-flops (FF1 and FF2 in the lower center of the symbol), the Conflict Detect network (right center of the symbol), and the Partial CIR Load Control (upper right).

Current Instruction Register (CIR)

Normally the CIR holds valid control words (instructions) until there are no conflicts with instructions already in process. When there are no conflicts, the instruction issues and the CIR can load another control word. When the CIR does not contain a valid control word its control clocks it each clock period until a valid control word enters the CIR. When a valid control word enters the CIR, control stops the CIR clock and again waits for an issue.

Issue is one of three ways of starting the CIR clock while the CIR contains a valid control word. The other two are Purge CIR and Master Clear CCN.

The Purge CIR operation starts the CIR clock and blocks the CIR inputs thus clearing the register. The CIR control continues to clock the CIR until a valid control word enters the register.

The Master Clear CCN operation clears the CIR and again, the CIR control will start clocking the CIR each clock period until a valid control word enters the register.

CIR Control

The CIR is controlled by the Control Word Valid signal on input pin NLDEN1 (input to the bottom register function in the symbol), the Purge CIR signal on pin LDPURG, the Master Clear CCN signal on pin MSTRCL, the Issue signal on pin LDEN2, and clock on pin CLCK.

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12AP-1 (Cont'd)

CIR Operation

There are three conditions which activate the CIR clock modifier Cl: CIR Valid signal is HI, Issue signal on input pin LDEN2 is LO, and the Purge CIR signal on input pin LDPURG is LO. This description assumes that each condition is active separately.

The HI state of the CIR Valid signal indicates that the CIR does not contain a valid control word. This signal is ORed with the Purge CIR and Issue signals and ANDed with clock. Thus as long as CIR Valid is HI, clock modifier Cl is active each time clock goes LO. When a valid control word is at the input to the CIR, the Control Word Valid signal on pin NLDEN1 is LO and the next active Cl sets the CIR Valid bit and clocks a valid control word into the CIR. The CIR Valid signals go LO and CM no longer enables Cl clocks.

The Issue signal on input pin LDEN2 can go LO only when the CIR contains a valid control word and there are no conflicts. When this signal is LO it activates the OR function in the common control block and is ANDed with clock. Thus when clock goes LO, Cl is active clocking new inputs into the CIR. The CIR Valid signal indicates whether or not the new CIR content is a valid control word.

When the Purge CIR signal is LO (input pin LDPURG) the OR function in the common control block is active and gating modifier Gl is inactive. Gl inactive blocks the inputs to most of the CIR. Thus when clock goes LO, Cl active will clear those CIR bits disabled by the inactive Gl. Note that the top 4 CIR bits (inputs CMPINA (0-3)) do not have the Gl gate at the input to the CTYR. Therefore Cl active always loads the signals from CMPINA (0-3) into the register. Since the input to the CIR Valid bit (input NLDEN1) is gated by Gl, the CIR Valid bit clears indicating that the CIR does not contain a valid control word.

Issue Network Input Register

Clock modifier C2 is active each time clock goes LO. The Issue Network Input Register therefore samples the processor conditions each clock period.

Shortstop Compare ALU

The Shortstop Compare ALU compares X-Register type and number from the CIR with the X Register type and number of results at specific points in the Result Pipeline (RPL). The result X Register type and number come from RPL stage 3 for Integer Unit results and RPL stage 4 for FloatingPoint results. The Compare determines whether or not a shortstop operation will resolve a conflict sooner than waiting for the conflicting instruction to complete.

Five bits each from the CIR and Issue Network Input Register enter the ALU where they are each weighted binarily 1 through 16 and designated as operands A and B respectively.

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12AP-1 (Cont'd)

The ALU compares the A and B operands for equality and gating modifier G2 gates the active HI result out of the ALU to pin NCMPEQ and also to the top AND gate in the Conflict Detect Network.

The AND gate in the common control block of the ALU activates gating modifier G2 when all three inputs to the AND are LO.

All three input signals are shortstop enables. Two come from the CIR and the third comes from the Issue Network Input Register.

Status Flip-Flops

The status flip-flops, FF1 and FF2, are RS flip-flops with logic on the inputs to each which makes the set inputs override the reset inputs. When the OR function fed by the set input is active, it blocks the AND function fed by the reset input.

The equation for making set modifier S active for each flip-flop is:

Set input LO AND Issue input LO AND clock.

The equation for making reset modifier R active for each flip-flop is:

Clear input LO AND (Set input HI OR Issue input HI) AND clock.

The flip-flops also have a common reset modifier in the common control block which is activated by the Master Clear CCN signal on pin MSTRCL ANDed with clock.

Conflict Detect

The Conflict Detect network is a set of gates which tests the content of the CIR, Issue Network Input Register, Shortstop Compare, Status flip-flops and individual input pins. When any gate is active, indicating a conflict, the active HI output disables the Partial Issue AND gate.

When the CIR Valid signal is HI, indicating that the content of the CIR is not valid, it disables the Partial Issue AND gate.

Outputs Yl and Y2 are both LO when there are no conflicts and the CIR contains a valid control word.

Partial CIR Load Control

Outputs Z1--3 control the loading of those portions of the CIR not contained in the 12AP arrays.

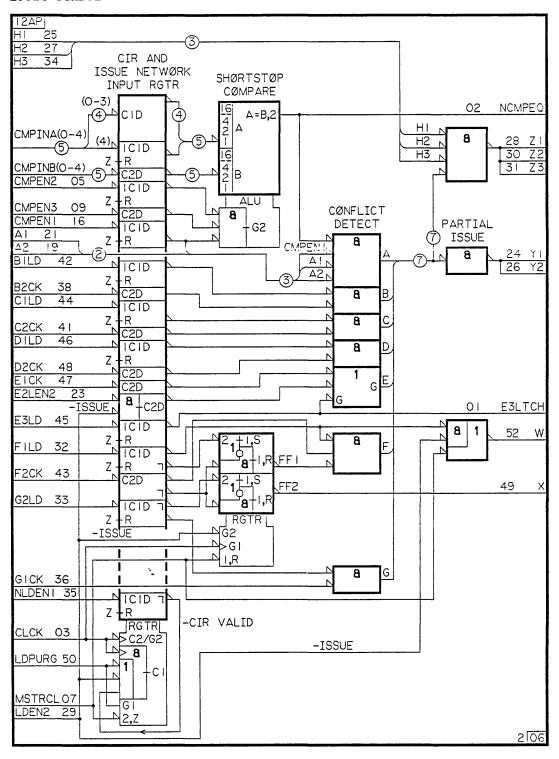
Inputs H1-3 connect to Partial Issue outputs from other 12AP arrays.

Outputs Z1-3 are LO when the CIR Valid signal is HI OR inputs H1-3 are all LO AND there are no conflicts AND the CIR Valid signal is LO.

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LOGIC SYMBOL



BIAS LØ = SI, NFØRCE BIAS HI = S2

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12AP-2 (Cont'd)

OPERATIONAL DESCRIPTION

The 12AP-2 contains a bit-slice of the Issue Network. The Issue Network holds and examines the next instruction and examines processor conditions such as functional unit, register, and result pipeline stage busies to determine whether or not there are conflicts with instructions already in process which will delay the issue of this next instruction.

The Current Instruction Register (CIR), in the Issue Network, holds the next instruction until there are no conflicts and the instruction issues, or the CIR is purged or master cleared.

The Issue Network Input Register, in the Issue Network, samples the processor conditions each clock period.

Parts of these two registers are interspersed down the left side of the symbol. Clock modifier C1 clocks data into the CIR. Clock modifier C2 clocks data into the Issue Network Input register.

Other parts of the Issue Network are the Shortstop Compare ALU (top center of the symbol), two status flip-flops (FF1 and FF2 in the lower center of the symbol), and the Conflict Detect network (right center of the symbol).

Current Instruction Register (CIR)

Normally the CIR holds valid control words (instructions) until there are no conflicts with instructions already in process. When there are no conflicts, the instruction issues and the CIR can load another control word. When the CIR does not contain a valid control word its control clocks it each clock period until a valid control word enters the CIR. When a valid control word enters the CIR, control stops the CIR clock and again waits for an issue.

Issue is one of three ways of starting the CIR clock while the CIR contains a valid control word. The other two are Purge CIR and Master Clear CCN.

The Purge CIR operation starts the CIR clock and blocks the CIR inputs thus clearing the register. The CIR control continues to clock the CIR until a valid control word enters the register.

The Master Clear CCN operation clears the CIR and again, the CIR control will start clocking the CIR each clock period until a valid control word enters the register.

CIR Control

The CIR is controlled by the Control Word Valid signal on input pin NLDEN1 (input to the bottom register function in the symbol), the Purge CIR signal on pin LDPURG, the Master Clear CCN signal on pin MSTRCL, the Issue signal on pin LDEN2, and clock on pin CLCK.

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12AP-2 (Cont'd)

CIR Operation

There are three conditions which activate the CIR clock modifier Cl: CIR Valid signal is HI, Issue signal on input pin LDEN2 is LO, and the Purge CIR signal on input pin LDPURG is LO. This description assumes that each condition is active separately.

The HI state of the CIR Valid signal indicates that the CIR does not contain a valid control word. This signal is ORed with the Purge CIR and Issue signals and ANDed with clock. Thus as long as CIR Valid is HI, clock modifier Cl is active each time clock goes LO. When a valid control word is at the input to the CIR, the Control Word Valid signal on pin NLDEN1 is LO and the next active Cl sets the CIR Valid bit and clocks a valid control word into the CIR. The CIR Valid signal goes LO and CM no longer enables Cl clocks.

The Issue signal on input pin LDEN2 can go LO only when the CIR contains a valid control word and there are no conflicts. When this signal is LO it activates the OR function in the common control block and is ANDed with clock. Thus when clock goes LO, Cl is active clocking new inputs into the CIR. The CIR Valid signal indicates whether or not the new CIR content is a valid control word.

When the Purge CIR signal is LO (input pin LDPURG) the OR function in the common control block is active and gating modifier Gl is inactive. Gl inactive blocks the inputs to most of the CIR. Thus when clock goes LO, Cl active will clear those CIR bits disabled by the inactive Gl. Note that the top 4 CIR bits (inputs CMPINA (0-3)) do not have the Gl gate at the input to the CTYR. Therefore Cl active always loads the signals from CMPINA (0-3) into the register. Since the input to the CIR Valid bit (input NLDENI) is gated by Gl, the CIR Valid bit clears indicating that the CIR does not contain a valid control word.

Issue Network Input Register

Clock modifier C2 is active each time clock goes LO. The Issue Network Input Register therefore samples the processor conditions each clock period.

Shortstop Compare ALU

The Shortstop Compare ALU compares the result X-Register type and number from the CIR with the X Register type and number of the Integer Unit (IGU) result at Result Pipeline (RPL) stage 3. An equal comparison inhibits the X Register busy flip-flops, for the IGU result at RPL stage 3, from clearing if the control word in CIR issues.

Five bits each from the CIR and Issue Network Input Register enter the ALU where they are each weighted binarily 1 through 16 and designated as operands A and B respectively.

The ALU compares the A and B operands for equality and gating modifier G2 gates the active HI result out of the ALU to pin NCMPEQ and also to the top AND gate in the Conflict Detect Network.

The AND gate in the common control block of the ALU activates gating modifier G2 when all three inputs to the AND are L0.

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12AP-2 (Cont'd)

All three input signals are shortstop enables. Two come from the CIR and the third comes from the Issue Network Input Register.

Status Flip-Flops

The status flip-flops, FF1 and FF2, are RS flip-flops with logic on the inputs to each which makes the set inputs override the reset inputs. When the OR function fed by the set input is active, it blocks the AND function fed by the reset input.

The equation for making set modifier S active for each flip-flop is:

Set input LO AND Issue input LO AND clock.

The equation for making reset modifier R active for each flip-flop is:

Clear input LO AND (Set input HI OR Issue input HI) AND clock.

The flip-flops also have a common reset modifier in the common control block which is activated by the Master Clear CCN signal on pin MSTRCL ANDed with clock.

Conflict Detect

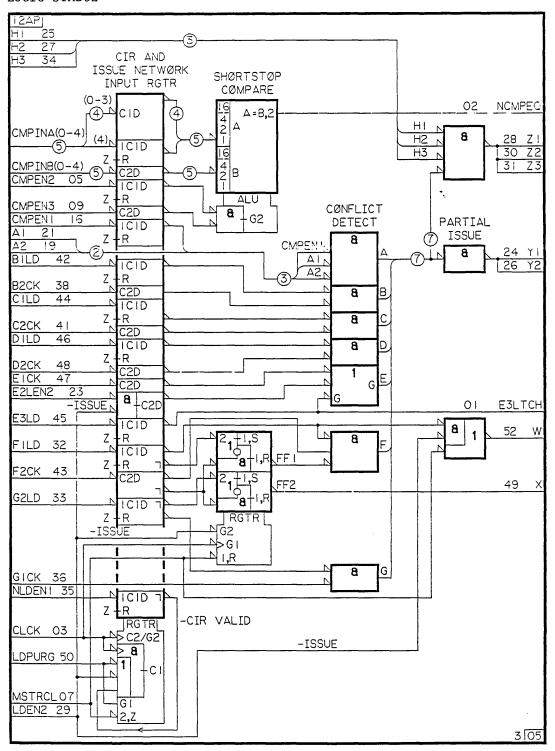
The Conflict Detect network is a set of gates which tests the content of the CIR, Issue Network Input Register, Shortstop Compare, Status flip-flops and individual input pins. When any gate is active, indicating a conflict, the active HI output disables the Partial Issue AND gate.

Outputs Yl and Y2 are both LO when there are no conflicts and the CIR contains a valid control word.

Outputs Z1-3 are LO when inputs H1-3 are all LO AND there are no conflicts.

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LOGIC SYMBOL



BIAS LØ = NFØRCE, SI, S2

BIAS HI = NØNE

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12AP-3 (Cont'd)

OPERATIONAL DESCRIPTION

The 12AP-3 contains a bit-slice of the Issue Network. The Issue Network holds and examines the next instruction and examines processor conditions such as functional unit, register, and result pipeline stage busies to determine whether or not there are conflicts with instructions already in process which will delay the issue of this next instruction.

The Current Instruction Register (CIR), in the Issue Network, holds the next instruction until there are no conflicts and the instruction issues, or the CIR is purged or master cleared.

The Issue Network Input Register, in the Issue Network, samples the processor conditions each clock period.

Parts of these two registers are interspersed down the left side of the symbol. Clock modifier Cl clocks data into the CIR. Clock modifier C2 clocks data into the Issue Network Input register.

Other parts of the Issue Network are the Shortstop Compare ALU (top center of the symbol), two status flip-flops (FFl and FF2 in the lower center of the symbol), and the Conflict Detect network (right center of the symbol).

Current Instruction Register (CIR)

Normally the CIR holds valid control words (instructions) until there are no conflicts with instructions already in process. When there are no conflicts, the instruction issues and the CIR can load another control word. When the CIR does not contain a valid control word its control clocks it each clock period until a valid control word enters the CIR. When a valid control word enters the CIR, control stops the CIR clock and again waits for an issue.

Issue is one of three ways of starting the CIR clock while the CIR contains a valid control word. The other two are Purge CIR and Master Clear CCN.

The Purge CIR operation starts the CIR clock and blocks the CIR inputs thus clearing the register. The CIR control continues to clock the CIR until a valid control word enters the register.

The Master Clear CCN operation clears the CIR and again, the CIR control will start clocking the CIR each clock period until a valid control word enters the register.

CIR Control

The CIR is controlled by the Control Word Valid signal on input pin NLDEN1 (input to the bottom register function in the symbol), the Purge CIR signal on pin LDPURG, the Master Clear CCN signal on pin MSTRCL, the Issue signal on pin LDEN2, and clock on pin CLCK.

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12AP-3 (Cont'd)

CIR Operation

There are three conditions which activate the CIR clock modifier Cl, CIR Valid Signal is HI, Issue signal on input pin LDEN2 is LO, and the Purge CIR signal on input pin LDPURG is LO. This description assumes that each condition is active separately.

The HI state of the CIR Valid signal indicates that the CIR does not contain a valid control word. This signal is ORed with the Purge CIR and Issue signals and ANDed with clock. Thus as long as CIR Valid is HI, clock modifier Cl is active each time clock goes LO. When a valid control word is at the input to the CIR, the Control Word Valid signal on pin NLDEN1 is LO and the next active Cl sets the CIR Valid bit and clocks a valid control word into the CIR. The CIR Valid signal goes LO and CM no longer enables Cl clocks.

The Issue signal on input pin LDEN2 can go LO only when the CIR contains a valid control word and there are no conflicts. When this signal is LO it activates the OR function in the common control block and is ANDed with clock. Thus when clock goes LO, Cl is active clocking new inputs into the CIR. The CIR Valid signal indicates whether or not the new CIR content is a valid control word.

When the Purge CIR signal is LO (input pin LDPURG) the OR function in the common control block is active and gating modifier Gl is inactive. Gl inactive blocks the inputs to most of the CIR. Thus when clock goes LO, Cl active will clear those CIR bits disabled by the inactive Gl. Note that the top 4 CIR bits (inputs CMPINA (0-3)) do not have the Gl gate at the input to the CTYR. Therefore Cl active always loads the signals from CMPINA (0-3) into the register. Since the input to the CIR Valid bit (input NLDEN1) is gated by Gl, the CIR Valid bit clears indicating that the CIR does not contain a valid control word.

Issue Network Input Register

Clock modifier C2 is active each time clock goes LO. The Issue Network Input Register therefore samples the processor conditions each clock period.

Shortstop Compare ALU

The Shortstop Compare ALU compares the result X-Register type and number from the CIR with the X Register type and number of the Floating Point Unit result at Result Pipeline (RPL) stage 4. An equal comparison inhibits the X Register Busy flip-flop, for the Floating Point Unit result at RPL stage 4, from clearing if the control word in CIR issues.

Five bits each from the CIR and Issue Network Input Register enter the ALU where they are each weighted binarily 1 through 16 and designated as operands A and B respectively.

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12AP-3 (Cont'd)

The ALU compares the A and B operands for equality and gating modifier G2 gates the active HI result out of the ALU to pin NCMPEQ and also to the top AND gate in the Conflict Detect Network.

The AND gate in the common control block of the ALU activates gating modifier G2 when all three inputs to the AND are LO.

All three input signals are shortstop enables. Two come from the CIR and the third comes from the Issue Network Input Register.

Status Flip-Flops

The status flip-flops, FF1 and FF2, are RS flip-flops with logic on the inputs to each which makes the set inputs override the reset inputs. When the OR function fed by the set input is active, it blocks the AND function fed by the reset input.

The equation for making set modifier S active for each flip-flop is:

Set input LO AND Issue input LO AND clock.

The equation for making reset modifier R active for each flip-flop is:

Clear input LO AND (Set input HI OR Issue input HI) AND clock.

The flip-flops also have a common reset modifier in the common control block which is activated by the Master Clear CCN signal on pin MSTRCL ANDed with clock.

Conflict Detect

The Conflict Detect network is a set of gates which tests the content of the CIR, Issue Network Input Register, Shortstop Compare, Status flip-flops and individual input pins. When any gate is active, indicating a conflict, the active HI output disables the Partial Issue AND gate.

Outputs Yl and Y2 are both LO when there are no conflicts and the CIR contains a valid control word.

Outputs Z1-3 are LO when inputs H1-3 are all LO AND there are no conflicts.

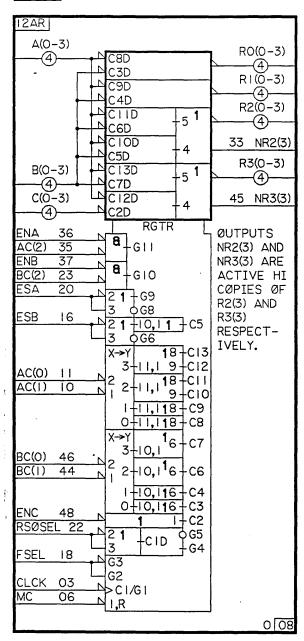
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12AR

PIN NAME	REAL PIN	VIRT
A(0)	19	V01
A(1)	17	V02
A(2)	38	V03
A(3)	32	V04
AC(0)	11	V15
AC(1)	10	V16
AC(2)	35	V22
B(0)	15	V05
B(1)	12	V06
B(2)	42	V07
B(3)	34	V08
BC(0)	46	V17
BC(1)	44	V18
BC(2)	23	V25
C(0)	09	V09
C(1)	08	V10
C(2)	43	V11
C(3)	41	V12
CLCK	03	V19
ENA	36	V24
ENB	37	V27
ENC	48	V38
ESA	20	V13
FSEL MC NFORCE RSOSEL	16 18 06 07 22	V14 V21 V29 V20 V28
NR2(3)	33	V23
NR3(3)	45	V26
R0Z	27	V47
R0(0)	26	V30
R0(1)	25	V31
R0(2)	28	V32
R0(3)	29	V33
R1Z	51	V48
R1(0)	02	V34
R1(1)	01	V35
R1(2)	52	V36
R1(3)	49	V37
R2(0)	21	V39
R2(1)	24	V40
R2(2)	30	V41
R2(3)	31	V42
R3(0)	05	V43
R3(1)	04	V44
R3(2)	50	V45
R3(3)	47	V46

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BIAS LØ = NFØRCE BIAS HI = NØNE TERMINATE PIN ROZ AND RIZ

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OPERATIONAL DESCRIPTION

The data portion of the 12AR-0 array contains six 4-bit registers. Three 4-bit input highways supply data to the registers. Input highway A connects to all six registers. Input highway B connects to the top five registers and input highway C connects only to the bottom register. Control entering the common control block may select each input highway to a separate register each clock. When the controls for two highways select the same register, the data from the two highways is ORed into the register.

This description numbers the registers top-to-bottom 0, 1, 2, 2, 3 and 3. Note that registers 0 and 1 each have their own 4-bit output highways (RO and R1). The outputs from registers 2 and 2 are multiplexed to one 4-bit output highway (R2). Output NR2(3) is an active HI copy of bit 3 of the mux. The outputs from registers 3 and 3 are also multiplexed to one 4-bit output highway (R3). Output NR3(3) is an active HI copy of bit 3 from that mux.

Clock modifier C2 clocks input highway C data into register 3 . Clock modifiers C3 - C7 control the destination registers for input highway B. C8 - C13 control the destination registers for input highway A.

Gating modifiers G4 and G5 select registers 2 or 2 and 3 or 3 through the output muxes.

Input Highway A Control

Input pins AC(0-2), ENA, ESA, FSEL, and CLCK control the destination register for input highway A.

Pins AC(0) and AC(1) are translated to select one of four registers. A translation of 0 selects register 0. A translation of 1 selects register 1. A translation of 2 selects registers 2 and 2. A translation of 3 selects registers 3 and 3.

The register select translations each connect to an OR function where gating modifiers Gll, Gl, Gl, and Gl further modify the selection. For example, in order to activate clock modifier Gll and clock the A input data into register Gll, the Gll and Gl

Gll is the enable for each of the four translations and is controlled by the AND of input pins ENA and AC(2).

Gl is active during the clock's transition to LO on input pin CLCK.

G8 and G9 select between two groups of registers. G8 selects registers 0, 1, 2, and 3, G9 selects registers 2 and 3. Input pins FSEL and ESA control G8 and G9. Pin FSEL controls the inversion of the select input pin ESA. When FSEL is HI, G2 is active and the LO state of pin ESA makes G9 active and G8 inactive. When FSEL is LO, G3 is active. G3 inverts the control of ESA by selecting the active HI state to control G8 and G9.

Input Highway B Control

Input pins BC(0-2), ENB, ESB, FSEL, and CLCK control the destination register for input highway B_{\bullet}

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12AR-0 (Cont'd)

Pins BC(0) and BC(1) are translated to select one of four registers. Translations of 0-3 select registers 0-3 respectively. The selection of register 2' is explained later.

The register select translations each connect to an OR function where gating modifiers G10, G1, and G6 further modify the selections. For example, in order to activate clock modifier G3 which clocks the B input data into register 0, the BC(0,1) translation must be G100 AND G100 AND G101 AND G102 must all be active.

G10 is the enable for each of the translations and is controlled by the AND of input pins ENB and BC(2).

Gl is active during the clock's transition to LO on input pin CLCK.

The OR function connected to input pin ESB selects either register 2 (clock modifier C5 active) or registers 0-3 (G6 active). Pin ESB is the primary control and pin FSEL controls the inversion of the signal on pin ESB. When FSEL is HI, G2 is active and the LO state of pin ESB activates the OR function. When FSEL is LO, G3 is active and the HI state of pin ESB activates the OR function.

C5 is active and clocks B input data into registers 2 when the OR function connected to ESB is active and G10 AND G1 are both active.

G6 is active when the OR function connected to ESB is inactive.

Input Highway C Control

Clock modifier C2 is active and clocks the C input data into register 3 when ENC is LO AND clock on pin CLCK goes LO.

Output Mux Control

Input pin RSOSEL, FSEL, and CLCK control the ouptut mux.

Pin RSOSEL is the select input and pin FSEL controls the inversion of that input. When FSEL is HI G2 gates RSOSEL in active LO. When FSEL is LO, G3 gates RSOSEL in active HI.

The selected state of RSOSEL connects to a 1-bit register which is clocked each time clock on pin CLCK goes LO. When the register is set, G4 is active and selects registers 2 and 3 through the muxes to the outputs. When the register is clear, G5 is active and gates registers 2 and 3 through the muxes to the outputs.

Master Clear

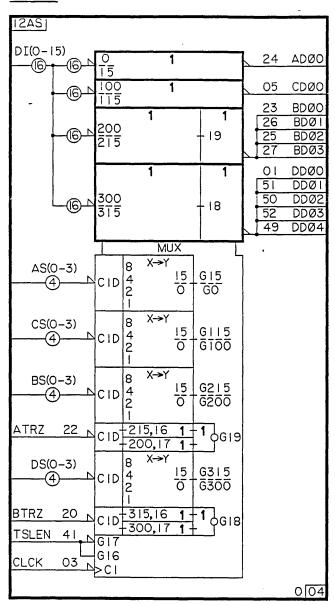
The master clear signal enters pin MC. When MC is LO and clock goes LO (Gl active), reset modifier R is active and clears all registers.

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12AS

DIN	DEAL	MDT
PIN NAME	REAL PIN	VIRT PIN
AS(0) AS(1)	16 19	V20 V19
AS(1) AS(2)	17	V19
AS(3)	21	V17
ATRZ	22	V35
BS(0) BS(1)	34 35	V29 V28
BS(2)	37	V27
BS(3)	30	V26
BTRZ	20	V36 V25
CLCK CS(0)	03 11	V25 V24
CS(1)	06	V23
CS(2)	80	V22
CS(3)	09 18	V21 V01
DI(1)	10	V02
DI(2)	12	V03
DI(3)	15 07	V04 V05
DI(5)	04	V06
DI(6)	33	V07
DI(7)	28 29	V08 V09
DI(9)	32	V10
DI(10)	31	V11
DI(11)	47	V12
DI(12)	38 45	V13 V14
DI(13)	45 36	V14 V15
DI(15)	46	V16
DS(0)	42	V33
DS(1) DS(2)	44 48	V32 V31
DS(3)	43	V30
TSLEN	41	V34
ADO0	02 24	V37 V40
BDO0	24 23	V40 V42
BDO1	26	V43
BDO2	25	V44
BDO3	27 05	V45 V41
DD00	01	V46
DDO1	51	V47
DDO2 DDO3	50 52	V48 V38
DD04	49	V39

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BIAS LØ = NFØRCE BIAS HI = NØNE

12AS-0 (Cont'd)

OPERATIONAL DESCRIPTION

The 12AS-0 contains four separately-controlled 16-to-1 muxes. The same 16-bit input highway (DI(0-15)) connects to each of the four muxes.

Sixteen gating modifiers in each mux gate one of the 16 bits through each mux. For example, gating modifiers G0, G100, G200 and G300 gate input pin DI(0) through their respective muxes and gating modifiers G1, G101, G201, and G301 gate input pin DI(1).

Each time clock on input pin CLCK goes LO, clock modifier Cl becomes active. Cl loads new 4-bit select codes for each mux and control signals ATRZ and BTRZ into registers in the common control block.

The output of each select code register is translated to activate one of 16 gating modifiers.

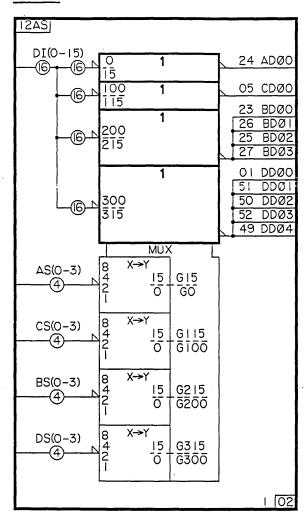
The top two muxes each have one output. The third and fourth muxes output four and five copies, respectively, of their selected bits.

The outputs of the third and fourth muxes are gated by G19 and G18, respectively. The purpose of these gating modifiers is to force zeros on the mux outputs when they are inactive.

G19 is inactive when the register connected to ARTZ is set AND the BS(0-3) register outputs translate to 15 (G215 active) AND input pin TSLEN is HI (G16 active), OR the BS(0-3) register outputs translate to 0 (G200 active) AND input pin TSLEN is LO (G17 active).

G18 is controlled by input pins BTRZ and TSLEN and the 0 and 15 translations from the register for the DS(0-3) select inputs. G18 operates in the same manner as G19.

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BIAS LØ = CLCK BIAS HI = NFØRCE, ATRZ, BTRZ, TSLEN

OPERATIONAL DESCRIPTION

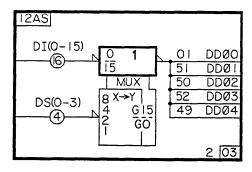
The 12AS-1 contains four separately-controlled 16-to-1 muxes. The same 16-bit input highway (DI(0-15)) connects to each of the four muxes.

Sixteen gating modifiers in each mux gate one of the 16 bits through each mux. For example, gating modifiers G0, G100, G200 and G300 gate input pin DI(0) through their respective muxes and gating modifiers G1, G101, G201, and G301 gate input pin DI(1).

Each select code is translated to activate one of 16 gating modifiers.

The top two muxes each have one output. The third and fourth muxes output four and five copies, respectively, of their selected bits.

12AS-2 16-to-1 Mux.



BIAS LØ = CLCK BIAS HI = NFØRCE, ATRZ, BTRZ, TSLEN

OPERATIONAL DESCRIPTION

The 12AS-2 is a 16-to-1 mux. Gating modifiers GO-G15 gate one of 16 input bits (DI(0-15) respectively) through the mux.

The DS(0-3) inputs are translated to activate one of the 16 gating modifiers.

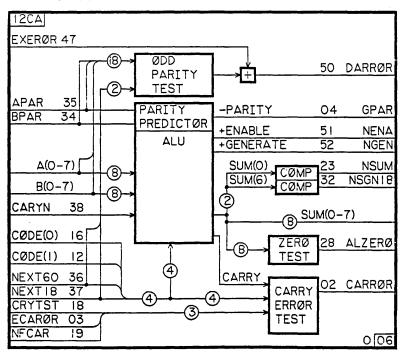
The selected bit connects to five output pins.

12CA

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	11	V01
A(1)	09	V03
A(2)	06	V05
A(3)	01	V07
A(4)	45	V09
A(5)	49	V11
A(6)	48	V12
A(7)	41	V14
APAR	35	V15
B(0)	10	V02
B(1)	05	V04
B(2)	07	V06
B(3)	08	V08
B(4)	44	V10
B(5)	43	V35
B(6)	46	V13
B(7)	42	V36
BPAR	34	V16
C(0)	17	V44
C(1)	20	V45
C(2) CARYN CODE(0) CODE(1)		V48 V38 V31 V32
CRYTST ECAROR EXEROR NEXT18	18 03	V43 V41 V29 V34
NEXT60	36	V33
NFCAR	19	V37
ALZERO CARROF		V30 V40
D	21	V47
DARROF	R 50	V42
GPAR	04	V25
ND	22	V46
NENA NGEN NSGN18 NSUM		V26 V27 V28 V39
SUM(0)	24	V17
SUM(1)	26	V18
SUM(2)	25	V19
SUM(3)	27	V20
SUM(4)	29	V21
SUM(5)	30	V22
SUM(6)	31	V23
SUM(7)	33	V24

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LOGIC SYMBOL

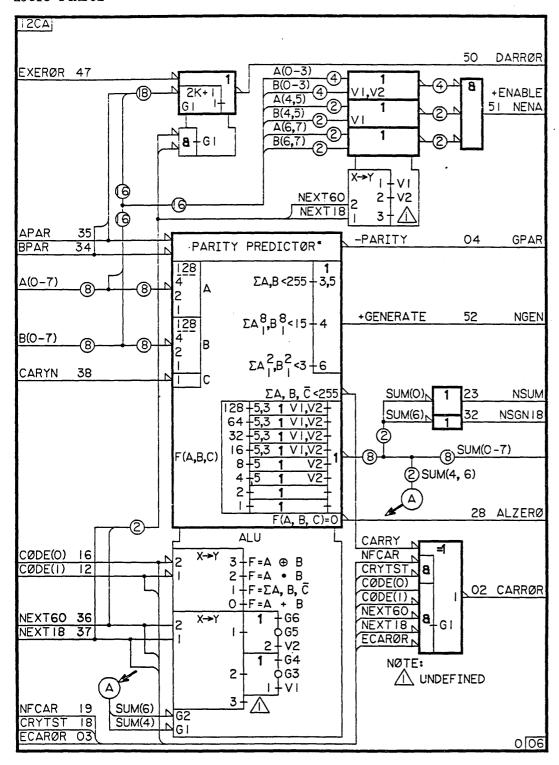


· BIAS NØNE

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagrams. Refer to the ANSI symbol and its description.

LOGIC SYMBOL



BIAS NONE

12CA-0 (Cont'd)

OPERATIONAL DESCRIPTION

Parity Check

The parity check circuit (output DARROR) performs an odd parity check on the two input operands. When NEXT60 and NEXT18 inputs are both LO (no sign extension), Gl will gate the odd parity check result into an OR function with input pin EXEROR. Output pin DARROR will be LO when input pin EXEROR is LO or when there is odd parity on either input operand and there is no sign extension.

Parity Predictor

The asterisk (*) in the Parity Predictor symbol indicates that the symbol is incomplete. Therefore, the following Parity Predictor information cannot be deduced from the symbol.

The Parity Predictor receives the parity bits from the two input operands (APAR and BPAR) and internal inputs from the ALU to determine what the parity of the result will be. Normally the Parity Predictor does not generate parity; it only adjusts it. Bad parity (odd) on one of the two input operands will result in odd parity on the output of the Parity Predictor.

The Parity Predictor works slightly differently when the ALN is in 1 of its 2 sign extension modes. When SUM bit 6 is extended (NEXT18=HI and NEXT60=LO), the parity predictor generates parity. In addition to extending SUM bit 6, the ALU is performing a logical OR function, and the Parity Predictor output is undefined. When SUM bit 4 is extended (NEXT18=LO and NEXT60=HI), the Parity Predictor assumes that B operand bits 0-3 contain even parity.

A Inputs

The 8-bit A highway enters the ALU, is weighted binarily 1-128, and designated as the A operand. It also feeds the parity check network (output DARROR) and the enable network (output NENA).

B Inputs

The 8-bit B highway enters the ALU, is weighted binarily 1-128, and designated as the B operand. It also feeds the parity check network (output DARROR) and the enable network (output NENA).

Carry Input

The carry input enters the ALU on the CARYN pin, is weighted as a binary 1, and designated as the C operand.

ALU Function

The CODE (0-1) inputs control the ALU function. A translation of 3 causes an exclusive OR of the A and B operands; a translation of 2 causes an AND operation; a translation of 1 produces a summation of A, B, and the complement of C; and a translation of 0 produces a logical OR of the A and B operands. For all ALU functions, the operands are aligned according to their binary weights.

The 8-bit result of the ALU function is weighted binarily 1-128 and then it is subjected to modifications by G(gating) and V(OR) modifiers on the way to the SUM (0-7) outputs. When G3 is inactive, result bits 0-3 are blocked and become zeros.

12CA-0 (Cont'd)

When G5 is inactive, result bits 0-5 are blocked and become zeros. When V1 is active, result bits 0-3 are forced to ones; when V2 is active, result bits 0-5 are forced to ones; when V modifiers are inactive they do not modify the result. The sign extension section describes the control of G3, G5, V1, and V2.

Sign Extension

The NEXT60 and NEXT18 inputs, and SUM bits 4 and 6 control sign extension in the ALU.

NEXT60 and NEXT18 inputs LO(translation of 0) causes normal operation with no sign extension. G5 and G3 will both be active and V1, V2, G4, and G6 will be inactive because the translations of 1 and 2 are inactive. This allows the result to pass unaltered out of the ALU and the proper equation to control the generate output (NGEN). Refer to the Generate Output description.

NEXT60 LO and NEXT18 HI (translation of 1) causes sign extension of the upper 6 bits of the ALU. A translation of 1 makes G5 inactive and G6 active. G5 inactive blocks the upper 6 bits of the ALU output and allows V2 to control the upper 6 bits. V2 is controlled by a translation of 1 and G2. G2 is controlled by SUM bit 6. Therefore V2 will follow SUM bit 6. When SUM bit 6 is LO, V2 is active and forces the upper six bits of the SUM output LO. When SUM bit 6 is HI, V2 is inactive and has no effect on the upper 6 zeros which were caused by an inactive G5. Thus for a translation of 1, SUM bit 6 is extended to SUM bits 0-5. G6 active gates the proper equation to control the generate output (NGEN). Refer to the Generate Output description.

NEXT60 HI and NEXT18 LO (translation of 2) sign extends SUM bit 4 to SUM bits 0-3. SUM bit 4 and a translation of 2 control G1, G4, G3, and V1 in the same manner as the extension of Sum bit 6 except it acts on the upper 4 bits instead of the upper 6 bits. (Refer to the previous paragraph for an explanation).

NEXT60 HI and NEXT18 HI (translation of 3) causes undefined results.

Enable Output

The enable output (NENA) is a group enable and will be active (HI) when there is a 00, 10, or 01, combination in each bit position of the A and B operands. NEXT60 and NEXT18 (sign extension control) control the number of bits in the A and B operand which are checked for the enable condition.

For a translation of 0, both V1 and V2 are inactive and have no effect on the B operand as it enters the OR functions. Note that both A and B operands enter active HI because the OR functions are checking for zeros.

A translation of l makes Vl active and this forces the B operand in the upper two OR functions active, enabling the upper 6 bit positions.

A translation of 2 makes V2 active and this forces the B operand in the upper OR function active, enabling the upper 4 bit positions.

A translation of 3 causes undefined results.

Generate Output

The generate output (NGEN) is controlled by equations and gating modifiers G3-6. NEXT60 and NEXT18 control G3-6. Refer to the Sign Extension description.

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12CA-0 (Cont'd)

When there is no sign extension (G3 and G5 both active), the NGEN output will be active (HI) when the summation of A and B are less than 255.

When the upper 4 bits of the result are being extended (G4 active), the NGEN output will be active when the summation of the lower 4 bits of A (binary weights of 8 thru 1) and the lower 4 bits of B are less than 15.

When the upper 6 bits of the result are being extended (G6 active), the NGEN output will be active when the summation of the lower 2 bits (binary weights of 2 and 1) and the lower 2 bits of B are less than 3.

Sum Outputs

Refer to the ALU Function Section for a description of the SUM (0-7) outputs.

NSUM and NSGN18 outputs are active HI copies of SUM (0,6) respectively.

ALZERO Output

ALZERO will be active (LO) when the result of the ALU function is equal to zero.

CARROR Output

CARROR is the result of an exclusive OR between CARRY and the AND of NFCAR and CRYTST. The exclusive OR result is gated out by G1. The AND gate enables G1 for non-extended summation operations only. ECAROR must also be LO.

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12CA-1 AND gate.

LOGIC SYMBOL

12CA			
C(0) 17 C(1) 20	8	21	D
C(1) 20 N $C(2)$ 15 N		22	ND
		J	102

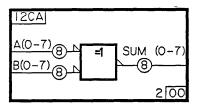
CØMPATIBLE WITH ANY BIAS

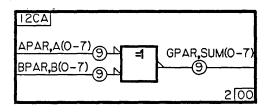
OPERATIONAL DESCRIPTION

(None required.)

12CA-2 Exclusive OR.

LOGIC SYMBOL





BIAS LØ = CØDE(O-I), NEXTI8, NEXT60 BIAS HI = NØNE

OPERATIONAL DESCRIPTION

SUM(0-7) outputs are the result of A(0-7) exclusive OR B(0-7)

The GPAR Output is the result of APAR exclusive OR BPAR.

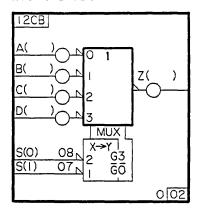
12CB

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	34	V01
A(1)	36	V02
A(2)	37	V03
A(3)	42	V04
A(4) A(5) A(6)	20 18 21	V05 V06 V07 V08
A(7) B(0) B(1) B(2)	12 35 33 38	V09 V10 V11
B(3)	41	V12
B(4)	17	V13
B(5)	15	V14
B(6)	24	V15
B(7)	11	V16
C(0)	32	V17
C(1)	31	V18
C(2)	44	V19
C(3)	45	V20
C(4)	27	V21
C(5)	25	V22
C(6)	19	V23
C(7) CLCK CLCKEN D(0)	48	V24 V38 V36 V25 V26
D(1) D(2) D(3) D(4) D(5)	47 46 43 23 16	V27 V28 V29 V30
D(6)	22	V31
D(7)	02	V32
LATCH	09	V37
S(0)	08	V33
S(1)	07	V34
S(2)	52	V35
P	51	V48
Z(0)	30	V39
Z(1)	49	V40
Z(2)	29	V41
Z(3)	50	V42
Z(4)	28	V43
Z(5)	04	V44
Z(6)	26	V45
Z(7)	05	V46
Z(8)	01	V47

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12CB-0 Four-Input Multiplexer.

LOGIC SYMBOL

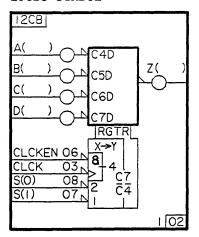


BIAS LØ = CLCKEN, CLCK BIAS HI = S(2), LATCH

OPERATIONAL DESCRIPTION

Pins S(0) and S(1) select one of four input highways to output highway Z.

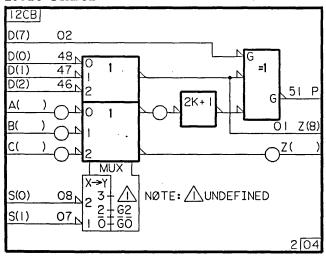
60458120 B



BIAS LØ = LATCH BIAS HI = S(2)

OPERATIONAL DESCRIPTION

Pins S(0) and S(1) select one of four input highways. Pins CLCK and CLCKEN are ANDed to latch the selected data in the register.



NØTE: TØ USE AS A PARITY CHECK NETWØRK PINS D(O-2) ARE THE PARITY BITS FØR THE A, B, AND C TRUNKS RESPECTIVELY. TØ USE AS A PARITY GENERATØR CØNNECT PINS D(O-2) TØ BIAS HI.

BIAS LØ = CLCKEN, CLCK BIAS HI = S(2), LATCH

OPERATIONAL DESCRIPTION

Input Select Control

Pins S(0) and S(1) select one of three input highways and one of three individual input pins through a pair of muxes when the select code equals 0, 1, or 2. The outputs of the muxes are undefined when the select code equals 3.

Parity Check

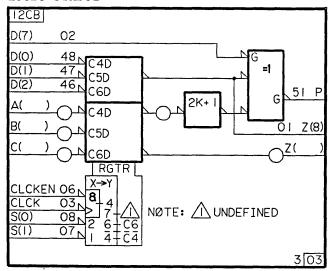
When the 12CB-2 is used for parity checking, input pins D(0), D(1), and D(2) receive the parity bits for input highways A, B, and C respectively. The =1 and 2K+1 functions work together to perform an odd parity check. The 2K+1 performs an odd parity check on the selected data and the result is exclusive ORed with the selected parity bit. Pin D(7) gates the result to output pin P. Output pin P will be LO when pin D(7) is LO and there is odd parity.

Parity Generate

When the 12CB-2 is used for parity generation, input pins D(0), D(1), and D(2) are all biased HI. The =1 and 2K+1 functions work together to generate the parity bit for even parity. The 2K+1 performs an odd parity check on the selected data and the result is exclusive ORed with the HI from the upper mux. Pin D(7) gates the result to output pin P. Output pin P is the new parity bit for the selected data.

12CB-3 Three-Input Multiplexer to a Register with Parity Checking or Parity Generation on the Output of the Register.

LOGIC SYMBOL



NØTE: TØ USE AS A PARITY CHECK NETWØRK PINS D(O-2) ARE THE PARITY BITS FØR THE A, B, AND C TRUNKS RESPECTIVELY. TØ USE AS A PARITY GENERATØR CØNNECT PINS D(O-2) TØ BIAS HI.

BIAS LØ = LATCH BIAS HI = S(2)

OPERATIONAL DESCRIPTION

Input Register Control

Pins S(0) and S(1) select one of three input highways and one of three individual input pins to a pair of registers. Pins CLCK and CLCKEN are ANDed to latch the selected data in the registers. The outputs of the registers are undefined when the output of the control translator equals 7.

Parity Check

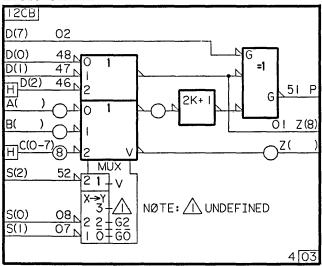
When the 12CB-3 is used for parity checking, input pins D(0), D(1), and D(2) receive the parity bits for input highways A, B, and C respectively. The =1 and 2K+1 functions work together to perform an odd parity check. The 2K+1 performs an odd parity check on the selected data and the result is exclusive ORed with the selected parity bit. Pin D(7) gates the result to output P. Output P will be LO when pin D(7) is LO and there is odd parity.

Parity Generate

When the 12CB-3 is used for parity generation, input pins D(0), D(1), and D(2) are all biased HI. The =1 and 2K+1 functions work together to generate the parity bit for even parity. The 2K+1 performs an odd parity check on the contents of the lower register and the result is exclusive ORed with the HI from the upper register. Pin D(7) gates the result to output pin P. Output pin P is the new parity bit for the data in the lower register.

12CB-4 Three-Input Multiplexer with Parity Generation or Parity Checking and Extension of HI's or LO's when Input Highway C is Selected.

LOGIC SYMBOL



NØTE: TØ USE AS A PARITY CHECK NETWØRK PINS D(O-2) ARE THE PARITY BITS FØR THE A, B, AND C TRUNKS RESPECTIVELY. TØ USE AS A PARITY GENERATØR CØNNECT PINS D(O-2)

TØ BIAS HI.
BIAS LØ = CLCKEN, CLCK
BIAS HI = LATCH, D(2), C(0-7)

OPERATIONAL DESCRIPTION

Input Select and Extension Control

Pins S(0) and S(1) select one of three input highways and one of three individual input pins through a pair of muxes when the select code equals 0, 1, or 2. The outputs of the muxes are undefined when the select code equals 3.

With a select code of 2, pin S(2) controls the extension of HIs or LOs to output highway Z. A select code of 2 causes the selection of input highway C (biased HI) into the lower mux, selects input pin D(2) (biased HI) into the upper mux, and gates input pin S(2) to modifier V.

If pin S(2) is HI during a select code of 2, V will be inactive. With V inactive, output highway Z contains the selected biased HI data.

If pin S(2) is LO during a select code of 2, V will be active forcing output highway Z LO.

The parity generating or parity checking functions are not affected by the V modifier.

Biasing pin D(2) HI insures correct parity (generating or checking) for the extension of LO's or HI's.

12CB-4 (Cont'd)

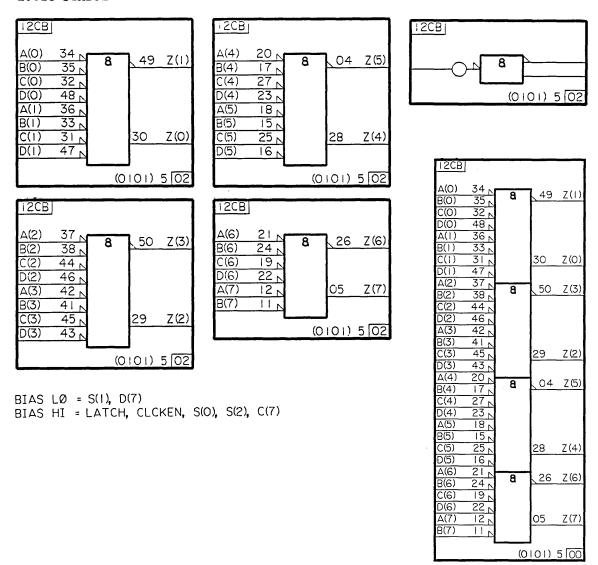
Parity check

When the 12CB-4 is used for parity checking, inputs D(0) and D(1) receive the parity bits for input highways A and B respectively. Pin D(2) is biased HI and is the parity bit for input highway C which is also biased HI. The =1 and 2K+1 functions work together to perform an odd parity check. The 2K+1 performs an odd parity check on the selected data and the result is EXCLUSIVE ORed with the selected parity bit. Pin D(7) gates the results to output pin P. Output pin P will be LO when pin D(7) is LO and there is odd parity.

Parity Generate

When the 12CB-4 is used for parity generation, input pins D(0), D(1), and D(2) are all biased HI. The =1 and 2K+1 functions work together to generate the parity bit for even parity. The 2K+1 performs an odd parity check on the selected data and the result is exclusive ORed with the HI from the upper mux. Pin D(7) gates the result to output pin P. Output pin P is the new parity bit for the selected data.

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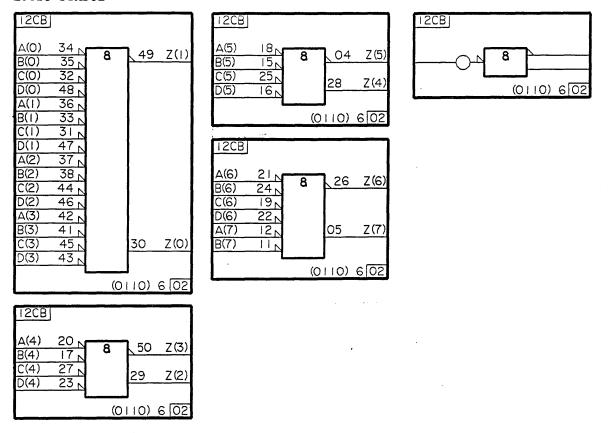
OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (0101) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

12CB-6 AND Gates.

LOGIC SYMBOL



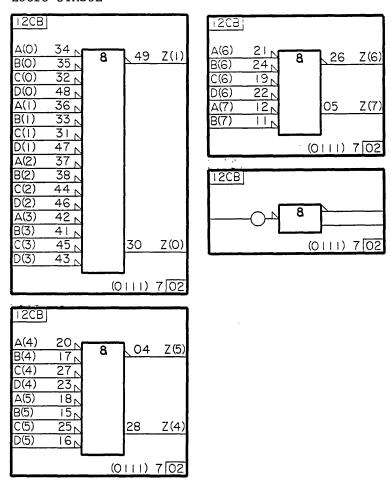
BIAS LØ = S(1), C(7)

BIAS HI = LATCH, CLCKEN, S(O), S(2), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (0110) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.



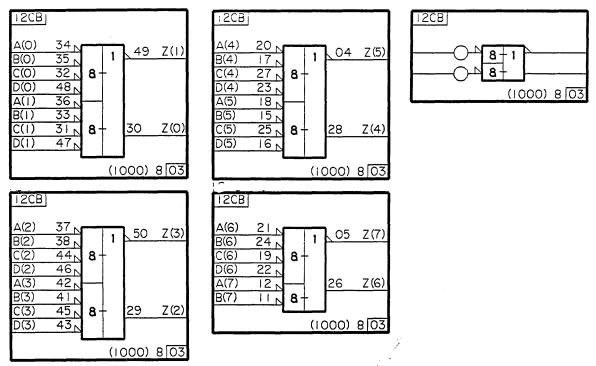
BIAS $L\emptyset = S(1)$, C(7), D(7)BIAS HI = LATCH, CLCKEN, S(0), S(2)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (0111) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

60458120 B

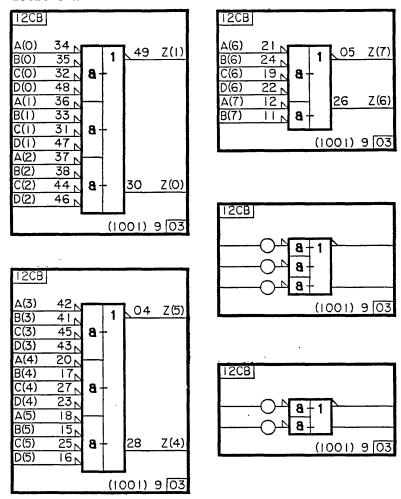


BIAS LØ = S(O) BIAS HI = LATCH, CLCKEN, S(1,2), C(7), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1000) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

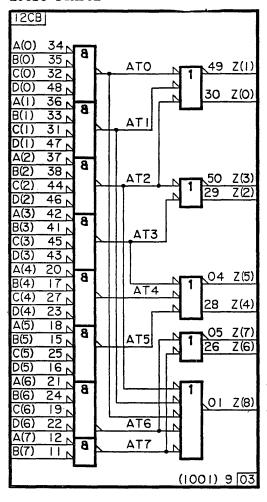


BIAS $L\emptyset = S(0)$, D(7)BIAS HI = LATCH, CLCKEN, S(1,2), C(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1001) in the bottom of each box is for designer reference. It denotes the biased states of pins S(0), S(1), C(7), and D(7) respectively.



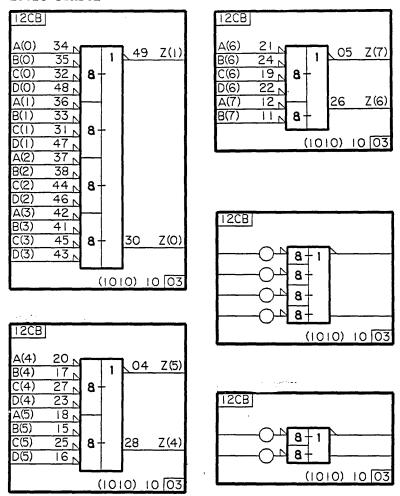
BIAS LØ = S(O), D(7)

BIAS HI = LATCH, CLCKEN, S(1,2), C(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1001) in the bottom of the box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.



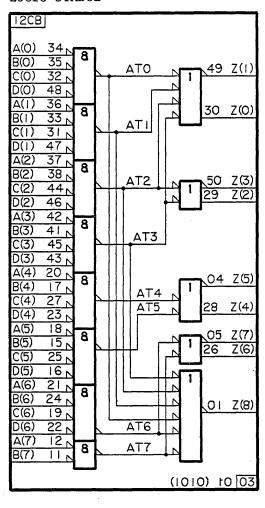
BIAS LØ = S(O), C(7)

BIAS HI = LATCH, CLCKEN, S(1,2), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1010) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

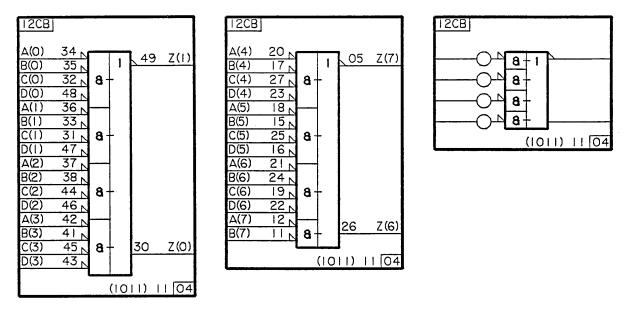


BIAS LØ = S(O), C(7) BIAS HI = LATCH, CLCKEN, S(1,2), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1010) in the bottom of the box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

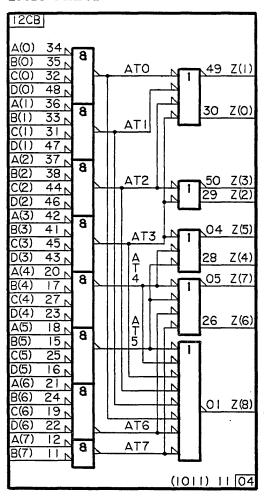


BIAS LØ = S(O), C(7), D(7) BIAS HI = LATCH, CLCKEN, S(1,2)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1011) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

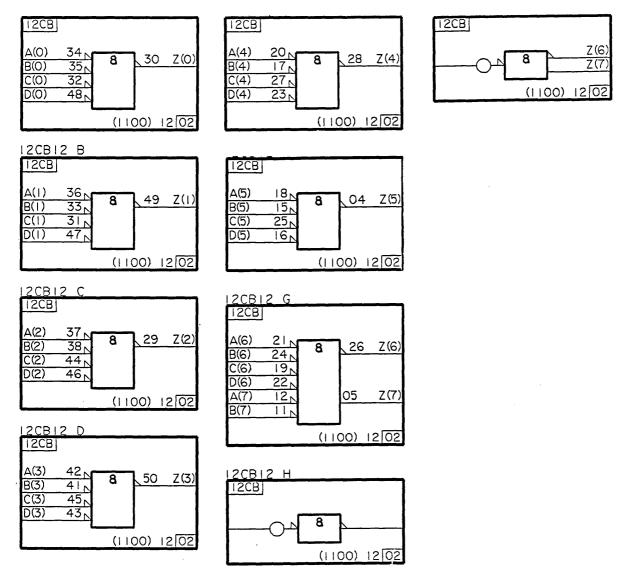


BIAS $L\emptyset = S(0)$, C(7), D(7)BIAS HI = LATCH, CLCKEN, S(1,2)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1011) in the bottom of the box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

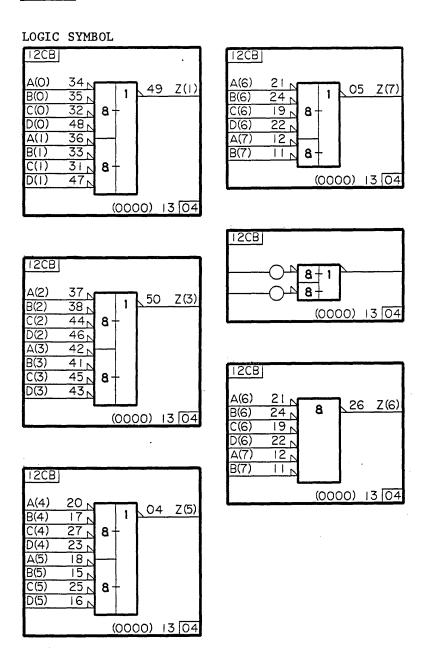


BIAS LØ = S(0,1)BIAS HI = LATCH, CLCKEN, S(2), C(7), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1100) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.



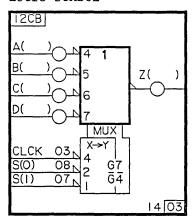
BIAS LØ = NØNE

BIAS HI = LATCH, CLCKEN, S(0-2), C(7), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (0000) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

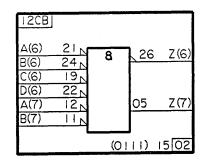


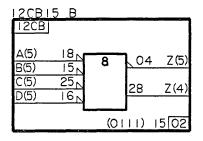
BIAS LØ = CLCKEN BIAS HI = S(2), LATCH

OPERATIONAL DESCRIPTION

Pins S(0) and S(1) select one of four input highways to output highway Z. Pin CLCK is used as a select enable.

12CB			•	
A(2) B(2)	37 N	8	49	Z(1)
C(2)	44		50	Z(3)
D(2)	46 _N			
A(3)	42 _N			
B(3)	41 _N			
C(3)	45 _N		30	Z(O)
D(3)	43 _N		29	Z(2)
	L	(01	11)	15 02



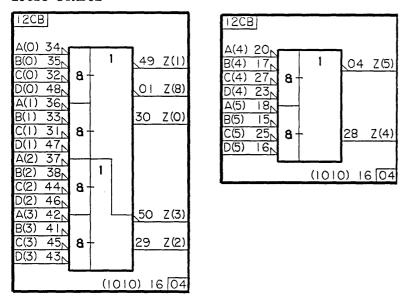


BIAS LØ = S(1), C(7), D(7), A(0), B(0), C(0), D(0), A(1), B(1), C(1), D(1), A(4), B(4), C(4), D(4) BIAS HI = S(0), S(2), LATCH, CLCKEN

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (0111) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

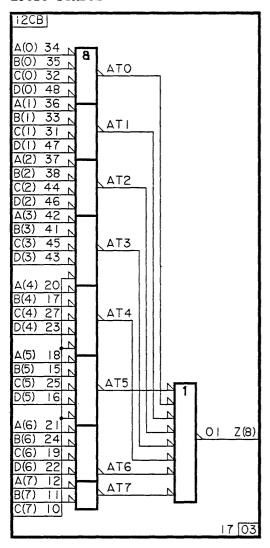


BIAS $L\emptyset = S(0)$, C(7)BIAS HI = A(6-7), LATCH, CLCKEN, S(1,2), D(7)

OPERATIONAL DESCRIPTION

Output pin Z(1) is the OR of all four AND gates. Output pin Z(3) is the OR of the lower two AND gates.

The (1010) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7).



BIAS LØ = S(0), D(7) BIAS HI = LATCH, CLCKEN, S(1,2)

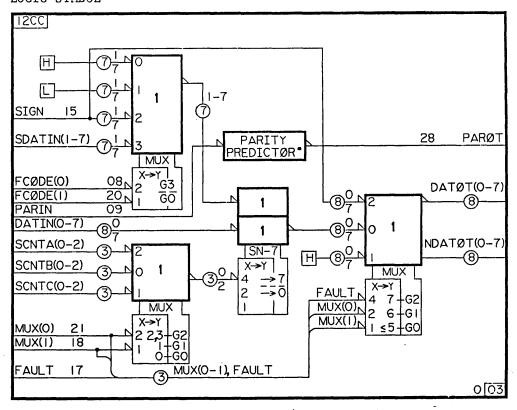
OPERATIONAL DESCRIPTION

(None required.)

12CC

PIN NAME	REAL PIN	VIRT PIN
DATIN(0 DATIN(1 DATIN(2 DATIN(3	1) 41 2) 02	V08 V09 V10 V11
DATIN(4 DATIN(5 DATIN(6 DATIN(7	5) 12 5) 11	V12 V13 V14 V15
FAULT FCODE((FCODE(MUX(0)		V48 V33 V34 V44
MUX(1) PARIN SCNTA(0 SCNTA(1		V45 V16 V35 V38
SCNTA(2 SCNTB(0 SCNTB(1 SCNTB(2)) 34 I) 19	V41 V36 V39 V42
SCNTC(0 SCNTC(1 SCNTC(2 SDATING	1) 22 2) 25	V37 V40 V43 V01
SDATING SDATING SDATING SDATING	(3) 46 (4) 42	V02 V03 V04 V05
SDATING SDATING SIGN	(7) 38 15	V06 V07 V47
DATOT(DATOT(DATOT(DATOT(DATOT(1) 52 2) 45 3) 49	V17 V19 V21 V23 V25
DATOT(DATOT(DATOT(NDATOT	6) 04 7) 05	V27 V29 V31 V18
NDATOT NDATOT NDATOT NDATOT	Γ(2) 48 Γ(3) 47	V20 V22 V24 V46
NDATOT NDATOT NDATOT PAROT	r(6) 03	V28 V30 V32 V46

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BIAS NØNE

OPERATIONAL DESCRIPTION

The 12CC-O consists of five major functional elements, the Shift Data Mux (upper left), the Shift Control Mux (lower left), the Parity Predictor, the Shift Network (lower center), and the Output Mux (lower right).

Parity Predictor

The asterisk in the Parity Predictor symbol indicates that the symbol is incomplete. Therefore, the following Parity Predictor information cannot be deduced from the symbol.

The even parity bit for the DATIN (0-7) data highway enters on pin PARIN. The Parity Predictor receives this parity bit and internal inputs (not shown) to perform its function.

The Parity Predictor does not generate parity. It adjusts even parity based on the input data and the operation performed. Bad parity in will result in bad parity out.

The parity bit output, PAROT, is forced HI when the FAULT input is LO.

Shift Data Mux

The FCODE (0,1) inputs select the data sent to the most-significant 7 bits of the shift network. Since the shift network performs a right (or down) shift, these most-significant bits represent the fill bits which fill in above as the main data byte, DATIN (0-7) is shifted down by the shift network.

A translation of 0 selects zeros (HIs), 1 selects ones (LOs), 2 selects the SIGN input (for sign extensions), and 3 selects the SDATIN (1-7) inputs. The SDATIN (1-7) inputs receive the next 7 bits of higher significance than those received by the DATIN (0-7) inputs.

Shift Control Mux

The MUX (0,1) inputs select one of three sets of shift control inputs for the shift network.

A translation of 0 selects SCNTB (0-2), 1 selects SCNTC (0-2), and 2 or 3 selects SCNTA (0-2).

Shift Network

Two groups of data bits enter the shift network. The 8 least-significant bits come from input pins DATIN (0-7) and the most-significant 7 bits (fill bits) come from the shift data mux. The shift network performs a right (down) end-off shift of 0 to 7-bit positions controlled by the shift count which comes from the Shift Control Mux.

If the shift count, selected by the shift control mux, is 0 there is no shift. The least-significant eight input bits go straight to the outputs. A shift count of 1 shifts the 15 inputs down 1-bit position. Thus the least-significant bit, entering DATIN (7), shifts end-off, and the least-significant fill-bit shifts in to the top bit position of the eight outputs. Shifts of 2 thru 7, operate in the same manner.

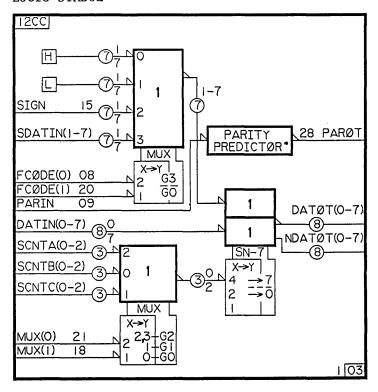
Output Mux

FAULT and MUX (0,1) inputs control the selection of sign extension, shifted data, or zeroes in the Output Mux.

A translation of 5 or less will select shifted data, 6 will select zeroes, and 7 will select sign (extended to all eight bit positions).

NDATOT (0-7) are active HI copies of the DATOT (0-7) active LO outputs.

60458120 B



BIAS LØ = NØNE 'BIAS HI = FAULT

OPERATIONAL DESCRIPTION

The 12CC-1 consists of 4 major functional elements, the Shift Data Mux (upper left), the Shift Control Mux (lower left), the Parity Predictor, and the Shift Network (lower right).

Parity Predictor

The asterisk in the Parity Predictor symbol indicates that the symbol is incomplete. Therefore, the following Parity Predictor information cannot be deduced from the symbol.

The even parity bit for the DATIN (0-7) data highway enters on pin PARIN. The Parity Predictor receives this parity bit and internal inputs (not shown) to perform its function.

The Parity Predictor does not generate parity. It adjusts even parity based on the input data and the operation performed. Bad parity in will result in bad parity out.

Shift Data Mux

The FCODE (0,1) inputs select the data sent to the most-significant 7 bits of the shift network. Since the shift network performs a right (or down) shift, these most-significant bits represent the fill bits which fill in above as the main data byte, DATIN (0-7) is shifted down by the shift network.

A translation of 0 selects zeros (HIs), 1 selects ones (LOs), 2 selects the SIGN input (for sign extension), and 3 selects the SDATIN (1-7) inputs. The SDATIN (1-7) inputs receive the next 7 bits of higher significance than those received by the DATIN (0-7) inputs.

Shift Control Mux

The MUX (0,1) inputs select one of three sets of shift control inputs for the shift network.

A translation of 0 selects SCNTB (0-2), 1 selects SCNTC (0-2), and 2 or 3 selects SCNTA (0-2).

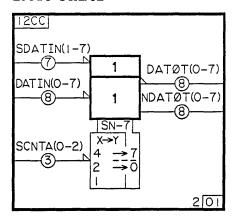
Shift Network

Two groups of data bits enter the shift network. The 8 least-significant bits come from input pins DATIN (0-7) and the most-significant 7 bits (fill bits) come from the shift data mux. The shift network performs a right (down) end-off shift of 0 to 7-bit positions controlled by the shift count which comes from the Shift Control Mux.

If the shift count, selected by the shift control mux is 0, there is no shift. The least-significant 8 input bits go straight to the outputs. A shift count of 1 shifts the 15 inputs down 1-bit position. Thus the least-significant bit entering DATIN (7), shifts end-off, and the least-significant fill-bit shifts in to the top bit position of the eight outputs. Shifts of 2 thru 7 operate in the same manner.

NDATOT (0-7) are active HI copies of the DATOT (0-7) active LO outputs.

60458120 B



BIAS LØ = MUX(O-1), FCØDE(O-1) BIAS HI = FAULT

OPERATIONAL DESCRIPTION

Two groups of data bits enter the shift network. The 8 least-significant bits come from input pins DATIN (0-7) and the most-significant 7 bits (fill bits) come from SDATIN (1-7). The shift network performs a right (down) shift end-off of 0 to 7-bit positions controlled by the shift count on pins SCNTA (0-2).

If the shift count is 0, there is no shift. The least-significant 8 input bits go straight to the outputs. A shift count of 1 shifts the 15 inputs down 1-bit position. Thus the least-significant bit entering DATIN (7) shifts end-off and the least-significant fill-bit shifts in to the top bit position of the eight outputs. Shifts of 2 thru 7 operate in the same manner.

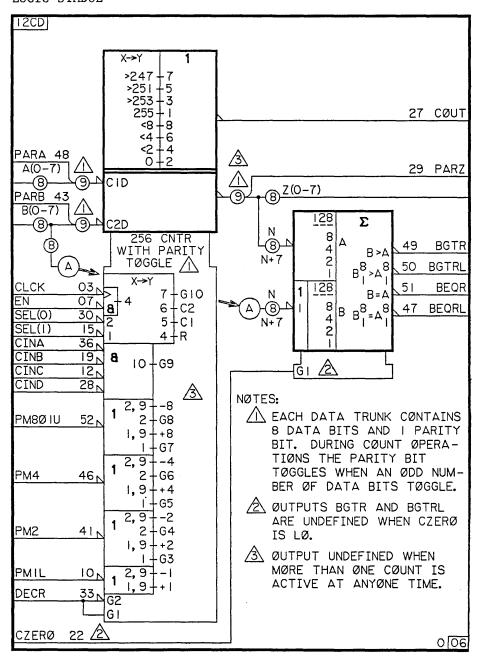
NDATOT (0-7) are active copies of the DATOT (0-7) active LO outputs.

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12CD

PIN	REAL	VIRT
NAME	PIN	PIN
A(0) A(1)	45 42	V10 V12
A(1) A(2)	38	V14
A(3)	35	V16
A(4) A(5)	20 18	V18 V20
A(6)	16	V22
A(7)	11	V24
B(0) B(1)	44 34	V11 V13
B(2)	37	V15
B(3)	32	V17
B(4) B(5)	17 01	V19 V21
B(6)	09	V23
B(7) CINA	06 36	V25 V05
CINB	19	V06
CINC	12 28	V07 V40
CLCK	03	V04
CZERO	22	V46
DECR	33 08	V26 V42
EN	07	V03
NTST	02	V27 V08
PARA PARB	48 43	V08 V09
PM1L	10	V41
PM2 PM4	41 46	V39 V38
PM801U		V37
SEL(0)	30	V01
SEL(1) BEOR	15	V02 V47
BEORL	51 47	V47 V48
BGTR	49	V44
BGTRL COUT	50 27	V45 V43
PARZ	29	V28
Z(0)	31	V29
Z(1) Z(2)	26 23	V30 V31
Z(3)	25	V32
Z(4) Z(5)	24 21	V33 V34
Z(6)	05	V35
Z(7)	04	V36

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BIAS LØ = NTST BIAS HI = DUAL

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12CD-0 (Cont'd)

OPERATIONAL DESCRIPTION

The 12CD-0 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the count in the counter. The count and gating modifiers G1-8 control the carry output (COUT).

The counter is in the middle and has two data input highways A(0-7) and B(0-7) and their parity bits PARA and PARB. The A and B inputs are used to load the counter and output highway Z(0-7) is the counter output. The PARZ output is the parity bit for output highway Z(0-7). During count operations, the parity bit will toggle when an odd number of data bits toggle. The counter has a modulus of 256; i.e., 0 through 255. The counter is also circular; i.e., one count beyond 255 is 0 and one count less than 0 is 255.

The common control block on the bottom contains the control for both the counter and the common output block.

SEL(0,1), EN, and CLCK control the major functions of the counter. A translation of 4 clears the counter, 5 clocks in data from A(0-7) and the parity bit PARA, 6 clocks in data from B(0-7) and parity bit PARB, and 7 initiates a count operation (GlO active).

CINA, B, C, and D are chip enables. They must all be LO to enable a count operation. G9 will be active when a counter operation is initiated (G10 active) and the chip is enabled (CINA-D LO).

DECR controls the direction of the count. When DECR is LO, the counter decrements (G2 active). When DECR is HI, the counter increments (G1 active).

PM801U, PM4, PM2, and PM1L enter OR functions which control the amount of the count (8, 4, 2, or 1) and the carry output. The description will describe a count of 4. The other counts operate in the same manner.

Count Operation

The count will change by 4 when PM4 is LO and PM801U, PM2, and PM1L are HI. PM4 active makes the OR function for a count of 4 active. The active OR function and G2 (decrement) will make G6 active. G6 is used in the common output block to activate the carry output (COUT) when the count in the counter is less than 4. When G1 (increment) is active, G5 will be active. G5 is used in the common output block to activate the carry output (COUT) when the count in the counter is greater than 251.

In addition to controlling the direction of the count, G1 and G2 control the carry output independently from the count amount controls. When the counter contains 255 and G1 is active or when the counter contains 0 and G2 is active, COUT will be active.

When G9 becomes active (count initiated (G10) and chip enabled), G1 and G2 control the direction of the count. G2 AND G9 decrement the counter by $4 \cdot \,$ G1 AND G9 increment the counter by $4 \cdot \,$

The parity bit will toggle when an odd number of data bits toggle.

60458120 B 2 of 3

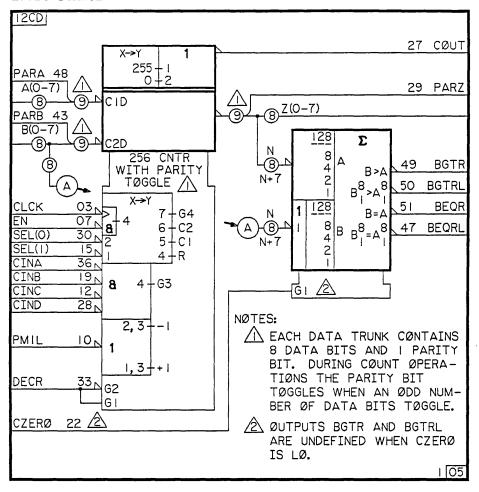
12CD-0 (Cont'd)

Compare Network

The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and designated as operand A. The lower highway comes from B(0-7). It is gated into the compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when B is greater than A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when B is equal to A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.

60458120 B 3 of 3



BIAS LØ = NTST

BIAS HI = DUAL, PM2, PM4, PM8Ø1U

OPERATIONAL DESCRIPTION

The 12CD-1 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into 3 areas from top to bottom. The common output block (above the double line) monitors the count in the counter. The count and gating modifiers Gl,2 control the carry output (COUT).

The counter is in the middle and has two data input highways A(0-7) and B(0-7) and their parity bits PARA and PARB. The A and B inputs are used to load the counter and output highway Z(0-7) is the counter output. The PARZ output is the parity bit for output highway Z(0-7). During count operations, the parity bit will toggle when an odd number of data bits toggle. The counter has a modulus of 256; i.e., 0 through 255. The counter is also circular; i.e., one count beyond 255 is 0 and one count less than 0 is 255.

12CD-1 (Cont'd)

The common control block on the bottom contains the control for both the counter and the common output block.

SEL(0,1), EN, and CLCK control the major functions of the counter. A translation of 4 clears the counter, 5 clocks in data from A(0-7) and the parity bit PARA, 6 clocks in data from B(0-7) and parity bit PARB, and 7 initiates a count operation (G4 active).

CINA, B, C, and D are chip enables. They must all be LO to enable a count operation. G3 will be active when a counter operation is initiated (G4 active) and the chip is enabled (CINA-D LO).

DECR controls the direction of the count. When DECR is LO, the counter decrements (G2 active). When DECR is HI, the counter increments (G1 active).

PML enters the OR function which controls the amount of the count.

Count Operation

In addition to controlling the direction of the count, G1 and G2 are used in the common output block to gate the proper equation for control of COUT. When G1 (increment) is active, and the counter contains a count of 255, COUNT will be active (LO). When G2 is active (decrement), and the counter contains a count of 0, COUT will be active.

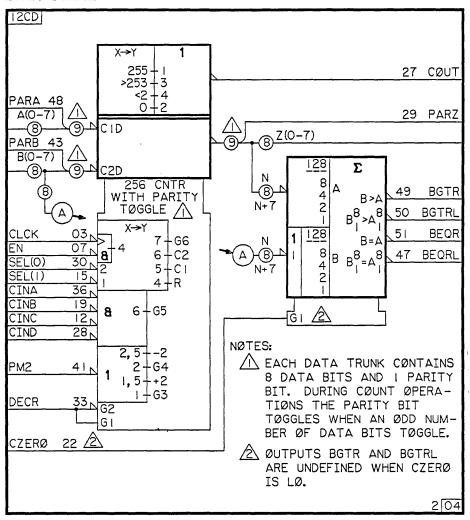
With PMlL active and when G3 becomes active (count initiated (G4) and chip enabled), G1 and G2 control the direction of the count. G2 AND G3 decrement the counter by 1. G1 AND G3 increment the counter by 1.

The parity bit will toggle when an odd number of data bits toggle.

Compare Network

The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and designated as operand A. The lower highway comes from B(0-7). It is gated into the compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when B is greater than A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when B is equal to A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.



BIAS LØ = NTST

BIAS HI = DUAL, PMIL, PM4, PM8ØIU

OPERATIONAL DESCRIPTION

The 12CD-2 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the count in the counter. The count and gating modifiers G1-4 control the carry output (COUT).

The counter is in the middle and has two data input highways A(0-7) and B(0-7) and their parity bits PARA and PARB. The A and B inputs are used to load the counter and output highway Z(0-7) is the counter output. The PARZ output is the parity bit for output

12CD-2 (Cont'd)

highway Z(0-7). During count operations, the parity bit will toggle when an odd number of data bits toggle. The counter has a modulus of 256; i.e., 0 through 255. The counter is also circular; i.e., one count beyond 255 is 0 and one count less than 0 is 255.

The common control block on the bottom contains the control for both the counter and the common output block.

SEL(0,1), EN, and CLCK control the major functions of the counter. A translation of 4 clears the counter, 5 clocks in data from A(0-7) and the parity bit PARA, 6 clocks in data from B(0-7) and parity bit PARB, and 7 initiates a count operation (G6 active).

CINA, B, C, and D are chip enable. They must all be LO to enable a count operation. G5 will be active when a counter operation is initiated (G6 active) and the chip is enabled (CINA-D LO).

DECR controls the direction of the count. When DECR is LO, the counter decrements (G2 active). When DECR is HI, the counter increments (G1 active).

PM2 enters the OR function which controls the amount of the count.

Count Operation

The count will change by 2 when PM2 is LO. PM2 active makes the OR function for a count of 2 active. The active OR function and G2 (decrement) will make G4 active. G4 is used in the common output block to activate the carry output (COUT) when the count in the counter is less than 2. When G1 (increment) is active, G3 will be active. G3 is used in the common output block to activate the carry output (COUT) when the count in the counter is greater than 253.

In addition to controlling the direction of the count, G1 and G2 control the carry output independently from the count amount control. When the counter contains 255 and G1 is active or when the counter contains 0 and G2 is active, COUT will be active.

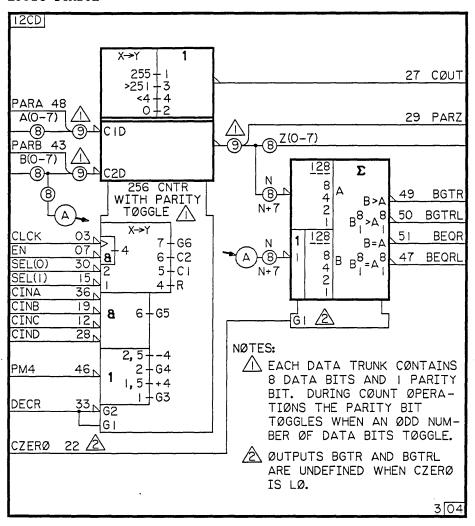
When G5 becomes active (count initiated (G6) and chip enabled), G1 and G2 control the direction of the count. G2 AND G5 decrement the counter by 2. G1 AND G5 increment the counter by 2.

The parity bit will toggle when an odd number of data bits toggle.

Compare Network

The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and designated as operand A. The lower highway comes from B(0-7). It is gated into the compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when B is greater than A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when B is equal to A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.



BIAS LØ = NTST

BIAS HI = DUAL, PM2, PM8Ø1U, PM1L

OPERATIONAL DESCRIPTION

The 12CD-3 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the count in the counter. The count and gating modifiers G1-4 control the carry output (COUT).

The counter is in the middle and has two data input highways A(0-7) and B(0-7) and their parity bits PARA and PARB. The A and B inputs are used to load the counter and output highway Z(0-7) is the counter output. The PARZ output is the parity bit for output

12CD-3 (Cont'd)

highway Z(0-7). During count operations, the parity bit will toggle when an odd number of data bits toggle. The counter has a modulus of 256; i.e., 0 through 255. The counter is also circular; i.e., one count beyond 255 is 0 and one count less than 0 is 255.

The common control block on the bottom contains the control for both the counter and the common output block.

SEL(0,1), EN, and CLCK control the major functions of the counter. A translation of 4 clears the counter, 5 clocks in data from A(0-7) and the parity bit PARA, 6 clocks in data from B(0-7) and parity bit PARB, and 7 initiates a count operation (G6 active).

CINA, B, C, and D are chip enable. They must all be LO to enable a count operation. G5 will be active when a counter operation is initiated (G6 active) and the chip is enabled (CINA-D LO).

DECR controls the direction of the count. When DECR is LO, the counter decrements (G2 active). When DECR is HI, the counter increments (G1 active).

PM4 enters the OR function which controls the amount of the count.

Count Operation

The count will have an amount of 4 when PM4 is LO. PM4 active makes the OR function for a count of 4 active. The active OR function and G2 (decrement) will make G4 active. G4 is used in the common output block to activate the carry output (COUT) when the count in the counter is less than 4. When G1 (increment) is active, G3 will be active. G3 is used in the common output block to activate the carry output (COUT) when the count in the counter is greater than 253.

In addition to controlling the direction of the count, G1 and G2 control the carry output independently from the count amount control. When the counter contains 255 and G1 is active or when the counter contains 0 and G2 is active, COUT will be active.

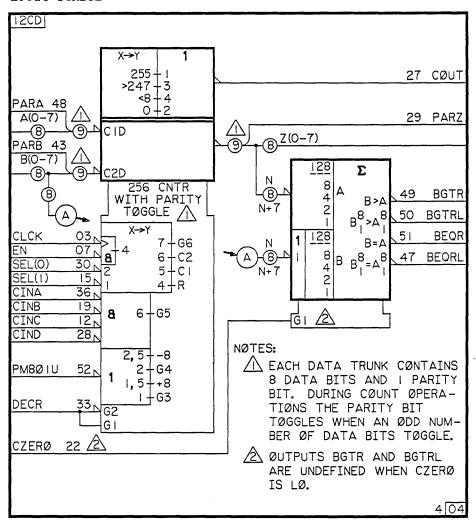
When G5 becomes active (count initiated (G6) and chip enabled), G1 and G2 control the direction of the count. G2 AND G5 decrement the counter by 4. G1 AND G5 increment the counter by 4.

The parity bit will toggle when an odd number of data bits toggle.

Compare Network

The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and designated as operand A. The lower highway comes from B(0-7). It is gated into the compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when B is greater than A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when B is equal to A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.



BIAS LØ = NTST BIAS HI = DUAL, PMIL, PM2, PM4

OPERATIONAL DESCRIPTION

The 12CD-4 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the count in the counter. The count and gating modifiers G1-4 control the carry output (COUT).

The counter is in the middle and has two data input highways A(0-7) and B(0-7) and their parity bits PARA and PARB. The A and B inputs are used to load the counter and output highway Z(0-7) is the counter output. The PARZ output is the parity bit for output

12CD-4 (Cont'd)

highway Z(0-7). During count operations, the parity bit will toggle when an odd number of data bits toggle. The counter has a modulus of 256; i.e., 0 through 255. The counter is also circular; i.e., one count beyond 255 is 0 and one count less than 0 is 255.

The common control block on the bottom contains the control for both the counter and the common output block.

SEL(0,1), EN, and CLCK control the major functions of the counter. A translation of 4 clears the counter, 5 clocks in data from A(0-7) and the parity bit PARA, 6 clocks in data from B(0-7) and parity bit PARB, and 7 initiates a count operation (G6 active).

CINA, B, C, and D are chip enable. They must all be LO to enable a count operation. G5 will be active when a counter operation is initiated (G6 active) and the chip is enabled (CINA-D LO).

DECR controls the direction of the count. When DECR is LO, the counter decrements (G2 active). When DECR is HI, the counter increments (G1 active).

PM801U enters an OR function which controls the amount of the count.

Count Operation

The count will have an amount of 8 when PM801U is LO. PM801U active makes the OR function for a count of 8 active. The active OR function and G2 (decrement) will make G4 active. G4 is used in the common output block to activate the carry output (COUT) when the count in the counter is less than 8. When G1 (increment) is active, G3 will be active. G3 is used in the common output block to activate the carry output (COUT) when the count in the counter is greater than 247.

In addition to controlling the direction of the count, G1 and G2 control the carry output independently from the count amount control. When the counter contains 255 and G1 is active or when the counter contains 0 and G2 is active, COUT will be active.

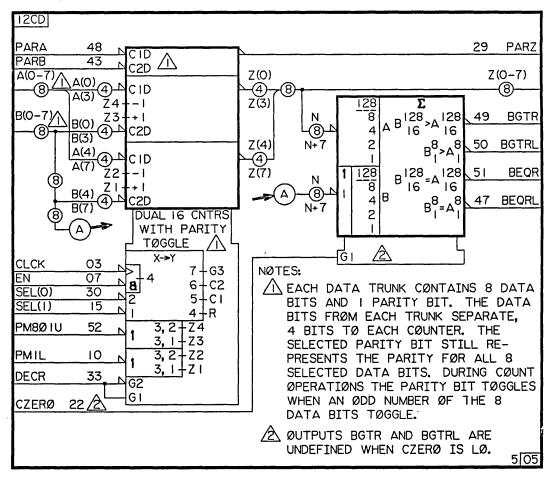
When G5 becomes active (count initiated (G6) and chip enabled), G1 and G2 control the direction of the count. G2 AND G5 decrement the counter by 8. G1 AND G5 increment the counter by 8.

The parity bit will toggle when an odd number of data bits toggle.

Compare Network

The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and designated as operand A. The lower highway comes from B(0-7). It is gated into the compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when B is greater than A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when B is equal to A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.



BIAS LØ = DUAL, CINA, CINB, CINC, CIND, NTST BIAS HI = PM2, PM4

OPERATIONAL DESCRIPTION

The 12CD-5 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into 4 areas from top to bottom. The top area is a parity bit register with two inputs, PARA and PARB. When the counter is loaded, Cl or C2 clock in the selected parity bit which represents the parity for the selected 8-bit data byte. Internal control (not shown) causes the parity bit to toggle when an odd number of bits in the 8-bit byte toggle. PARZ is the parity bit output.

12CD-5 (Cont'd)

The next two areas below the parity bit register are each 4-bit counters. Each counter has two 4-bit highwayed inputs (A and B) and one 4-bit highwayed output (Z). Each counter can increment or decrement by 1 under the control of the Z inputs which are interconnections to the common control block. Each counter has a modulus of 16 (0-15) and counts in a circular manner; i.e., one count beyond 15 is 0, one count less than 0 is 15.

The bottom area is the common control block which contains the control for both counters.

SEL(0,1), EN, and CLCK control the major functions of the counters. A translation of 4 clears both counters and the parity bit register, 5 clocks in A data to each counter and the parity bit for A, 6 clocks in B data to each counter and the parity bit for B, and 7 initiates a count operation (G3 active).

DECR controls the direction of the count for both counters. When DECR is LO, the counter decrements (G2 active). When DECR is HI, the counter increments (G1 active).

PM801U enters an OR function which controls the upper 4-bit counter. PM1L enters an OR function which controls the lower 4-bit counters. Both counters may be active (counting) simultaneously.

Count Operation

PM801U, G3 (count initiated) and G2 (decrement) all active will make Z4 active. Z4 connects to the upper counter and decrements it by 1.

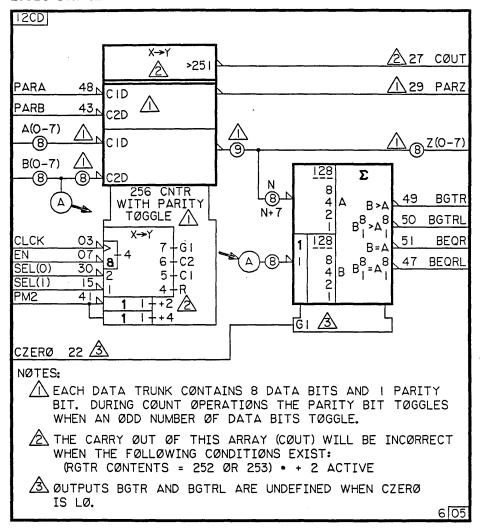
PM801U, G3, and G1 (increment) all active will make Z3 active. Z3 connects to the upper counter and increments it by 1.

PM1L and G1-3 control the lower counter in the same manner as PM801U and G1-3 control the upper counter.

Compare Network

The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and designated as operand A. The lower highway comes from B(0-7). It is gated into compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when the 4 most-significant bits of B are greater than the 4 most-significant bits of A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when the 4 most-significant bits of B are equal to the 4 most-significant bits of B are equal to the 4 least-significant bits of A.



BIAS LØ = PM4, CINA, CINB, CINC, CIND, NTST BIAS HI = DECR, DUAL, PMIL, PM8ØIU

OPERATIONAL DESCRIPTION

The 12CD-6 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into 4 areas from top to bottom. The common output block (above the double line) monitors the count in the counter. If the count is greater than 251, output COUT will be active (LO).

12CD-6 (Cont'd)

The next area below the common output block is a parity bit register with two inputs, PARA and PARB. When the counter is loaded, Cl or C2 clocks in the selected parity bit which represents the parity for the selected 6-bit data byte. Internal control (not shown) causes the parity bit to toggle when an odd number of bits in the 8-bit byte toggle. PARZ is the parity bit output.

The counter is the third area from the top and has two data input highways A(0-7) and B(0-7). The counter data outputs are Z(0-7). The counter has a modulus of 256 (0-255) and counts in a circular manner; i.e., one count beyond 255 is 0.

The bottom area is the common control block which contains the control for the counter.

SEL(0,1), EN, and CLCK control the major functions of the counter. A translation of 4 clears the counter, 5 clocks in data from A(0-7) and the parity bit PARA, 6 clocks in data from B(0-7) and parity bit PARB, and 7 initiates a count operation (Gl active).

PM2 controls the amount of the count by selecting between a count of plus 2 (when LO) or plus 4 (when HI).

Count Operation

When PM2 is HI when G1 becomes active (count initiated) and PM4 is active (LO), the counter increments by 4. When PM2 is LO when G1 becomes active, the counter increments by 2.

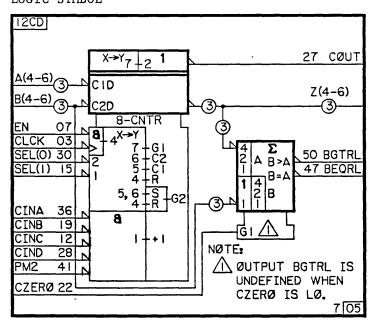
The equation which controls the carry output (COUT) is fixed at greater than 251 and assumes a count of 4 will take place. The proper equation for an increment of 2 is greater than 253. Therefore, when an increment of 2 takes place and the count is 252 or 253, the carry output is not correct.

Compare Network

The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and designated as operand A. The lower highway comes from B(0-7). It is gated into the compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when B is greater than A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when B is equal to A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.

60458120 B



BIAS LØ = A(O-3), B(O-3), DUAL, NTST BIAS HI = DECR, PMIL, PM4, PM8ØIU

OPERATIONAL DESCRIPTION

The 12CD-7 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the count in the counter. The count and gating modifier G2 control the carry output (COUT). When the count is equal to 7 and G2 is active, COUT will be active (LO).

The counter is in the middle and has two data input highways A(4-6) and B(4-6). The counter data outputs are Z(4-6). The counter has a modulus of 8 (0-7) and counts in a circular manner; i.e., one count beyond 7 is 0.

The common control block on the bottom contains the control for both the counter and the common output block.

SEL(0,1), EN, and CLCK control the major functions of the counter. A translation of 4 clears the counter and clears the RS flip-flop which controls G2. A translation of 5 clocks in data from A(4-6) and sets the RS flip-flop making G2 active. A translation of 6 clocks in data from B(4-6) and sets the RS flip-flop (if not previously set) making G2 active. Loading the counter from either input highway makes G2 active. G2 will remain active until the counter is cleared. G2 is used in the common output block. A translation of 7 makes G1 active initiating a count operation.

12CD-7 (Cont'd)

CINA, B, C, and D are chip enables. They enter an AND function with the count enable PM2 and control the count.

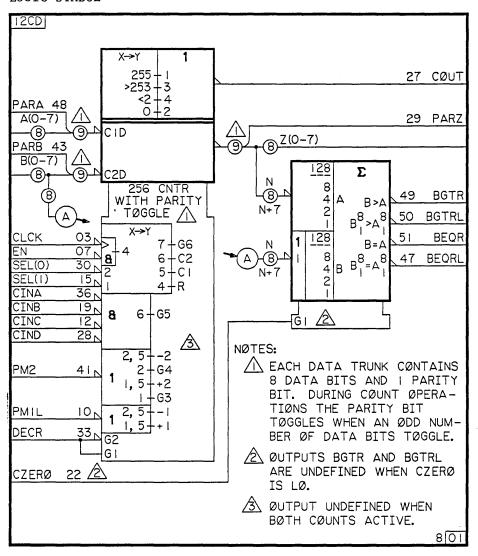
Count Operation

When CINA-D and PM2 are active when Gl (count initiated) becomes active, the counter will increment by l.

Compare Network

The compare network has two 3-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 4 and designated as operand A. The lower highway comes from B(4-6). It is gated into the compare network by CZERO HI, weighted binarily 1 through 4 and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTRL will be active (LO) when B is greater than A. BEQRL will be active (LO) when B is equal to A.



BIAS LØ = NTST BIAS HI = DUAL, PM4, PM8ØIU

OPERATIONAL DESCRIPTION

The 12CD-8 contains two major functional elements, a counter and a compare network

Counter

The counter symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the count in the counter. The count and gating modifiers G1-4 control the carry output (COUT).

12CD-8 (Cont'd)

The counter is in the middle and has two data input highways A(0-7) and B(0-7) and their parity bits PARA and PARB. The A and B inputs are used to load the counter and output highway Z(0-7) is the counter output. The PARZ output is the parity bit for output highway Z(0-7). During count operations, the parity bit will toggle when an odd number of data bits toggle. The counter data outputs are Z(0-7) and the parity bit is PARZ. The counter has a modulus of 256; i.e., 0 through 255. The counter is also circular; i.e., one count beyond 255 is 0 and one count less than 0 is 255.

The common control block on the bottom contains the control for both the counter and the common output block.

SEL(0,1), EN, and CLCK control the major functions of the counter. A translation of 4 clears the counter, 5 clocks in data from A(0-7) and the parity bit PARA, 6 clocks in data from B(0-7) and parity bit PARB, and 7 initiates a count operation (G6 active).

CINA, B, C, and D are chip enables. They must all be LO to enable a count operation. G5 will be active when a count operation is initiated (G6 active) and the chip is enabled (CINA-D LO).

DECR controls the direction of the count. When DECR is LO, the counter decrements (G2 active). When DECR is HI, the counter increments (G1 active).

PM2 and PM1L enter OR functions which control the amount of the count (2 or 1).

Count Operation

The count will change by 2 when PM2 is LO and PM1L is HI. PM2 active makes the OR function for a count of 2 active. The active OR function and G2 (decrement) will make G4 active. G4 is used in the common output block to activate the carry output (COUT) when the count in the counter is less than 2. When G1 (increment) is active, G3 will be active. G3 is used in the common output block to activate the carry output (COUT) when the count in the counter is greater than 253.

In addition to controlling the direction of the count, Gl and G2 can control the carry output independently from the count amount controls. When the counter contains 255 and G1 is active or when the counter contains 0 and G2 is active, COUT will be active.

When G5 becomes active (count initiated (G6) and chip enabled), G1 and G2 control the direction of the count. G2 AND G5 decrement the counter by 2. G1 AND G5 increment the counter by 2.

The count will change by I when PM1L is LO and PM2 is HI. Gl and G2 control the direction of the count and the carry output (COUT).

The parity bit will toggle when an odd number of data bits toggle.

Compare Network

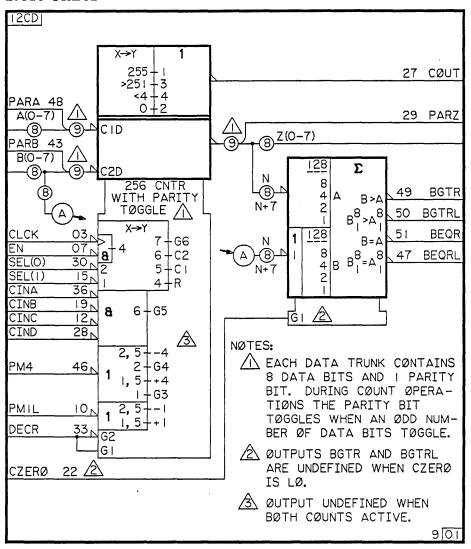
The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and

12CD-8 (Cont'd)

designated as operand A. The lower highway comes from B(0-7). It is gated into the compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when B is greater than A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when B is equal to A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.

60458120 B



BIAS LØ = NTST

BIAS HI = DUAL, PM2, PM8Ø1U

OPERATIONAL DESCRIPTION

The 12CD-9 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the count in the counter. The count and gating modifiers G1-4 control the carry output (COUT).

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12CD-9 (Cont'd)

The counter is in the middle and has two data input highways A(0-7) and B(0-7) and their parity bits PARA and PARB. The A and B inputs are used to load the counter and output highway Z(0-7) is the counter output. The PARZ output is the parity bit for output highway Z(0-7). During count operations, the parity bit will toggle when an odd number of data bits toggle. The counter data outputs are Z(0-7) and the parity bit is PARZ. The counter has a modulus of 256; i.e., 0 through 255. The counter is also circular; i.e., one count beyond 255 is 0 and one count less than 0 is 255.

The common control block on the bottom contains the control for both the counter and the common output block.

SEL(0,1), EN, and CLCK control the major functions of the counter. A translation of 4 clears the counter, 5 clocks in data from A(0-7) and the parity bit PARA, 6 clocks in data from B(0-7) and parity bit PARB, and 7 initiates a count operation (G6 active).

CINA, B, C, and D are chip enables. They must all be LO to enable a count operation. G5 will be active when a count operation is initiated (G6 active) and the chip is enabled (CINA-D LO).

DECR controls the direction of the count. When DECR is LO, the counter decrements (G2 active). When DECR is HI, the counter increments (G1 active).

PM4 and PM1L enter OR functions which control the amount of the count (4 or 1).

Count Operation

The count will change by 4 when PM4 is LO and PM1L is HI. PM4 active makes the OR function for a count of 4 active. The active OR function and G2 (decrement) will make G4 active. G4 is used in the common output block to activate the carry output (COUT) when the count in the counter is less than 4. When G1 (increment) is active, G3 will be active. G3 is used in the common output block to activate the carry output (COUT) when the count in the counter is greater than 251.

In addition to controlling the direction of the count, G1 and G2 can control the carry output independently from the count amount controls. When the counter contains 255 and G1 is active or when the counter contains 0 and G2 is active, COUT will be active.

When G5 becomes active (count initiated (G6) and chip enabled), G1 and G2 control the direction of the count. G2 AND G5 decrement the counter by 4. G1 AND G5 increment the counter by 4.

The count will change by l when PMlL is LO and PM4 is HI. G1 and G2 control the direction of the count and the carry output (COUT).

The parity bit will toggle when an odd number of data bits toggle.

Compare Network

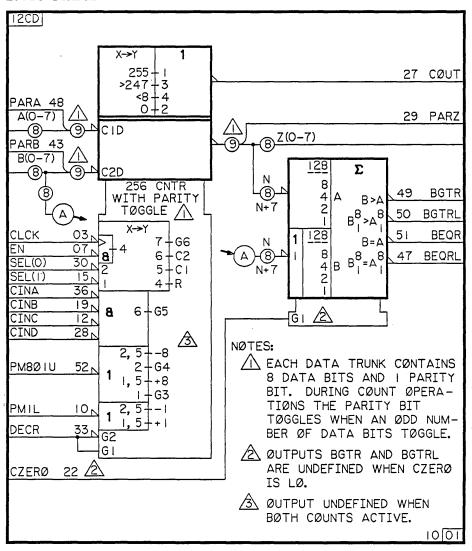
The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and

12CD-9 (Cont'd)

designated as operand A. The lower highway comes from B(0-7). It is gated into the compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when B is greater than A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when B is equal to A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.

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BIAS LØ = NTST BIAS HI = DUAL, PM2, PM4

OPERATIONAL DESCRIPTION

The 12CD-10 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the count in the counter. The count and gating modifiers G1-4 control the carry output (COUT).

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12CD-10 (Cont'd)

The counter is in the middle and has two data input highways A(0-7) and B(0-7) and their parity bits PARA and PARB. The A and B inputs are used to load the counter and output highway Z(0-7) is the counter output. The PARZ output is the parity bit for output highway Z(0-7). During count operations, the parity bit will toggle when an odd number of data bits toggle. The counter data outputs are Z(0-7) and the parity bit is PARZ. The counter has a modulus of 256; i.e., 0 through 255. The counter is also circular; i.e., one count beyond 255 is 0 and one count less than 0 is 255.

The common control block on the bottom contains the control for both the counter and the common output block.

SEL(0,1), EN, and CLCK control the major functions of the counter. A translation of 4 clears the counter, 5 clocks in data from A(0-7) and the parity bit PARA, 6 clocks in data from B(0-7) and parity bit PARB, and 7 initiates a count operation (G6 active).

CINA, B, C, and D are chip enables. They must all be LO to enable a count operation. G5 will be active when a count operation is initiated (G6 active) and the chip is enabled (CINA-D LO).

DECR controls the direction of the count. When DECR is LO, the counter decrements (G2 active). When DECR is HI, the counter increments (G1 active).

PM801U and PM1L enter OR functions which control the amount of the count (8 or 1).

Count Operation

The count will change by 8 when PM801U is LO and PM1L is HI. PM801U active makes the OR function for a count of 8 active. The active OR function and G2 (decrement) will make G4 active. G4 is used in the common output block to activate the carry output (COUT) when the count in the counter is less than 8. When G1 (increment) is active, G3 will be active. G3 is used in the common output block to activate the carry output (COUT) when the count in the counter is greater than 247.

In addition to controlling the direction of the count, G1 and G2 can control the carry output independently from the count amount controls. When the counter contains 255 and G1 is active or when the counter contains 0 and G2 is active, COUT will be active.

When G5 becomes active (count initiated (G6) and chip enabled), G1 and G2 control the direction of the count. G2 AND G5 decrement the counter by 8. G1 AND G5 increment the counter by 8.

The count will change by 1 when PMIL is LO and PM801U is HI. G1 and G2 control the direction of the count and carry output (COUT).

The parity bit will toggle when an odd number of data bits toggle.

Compare Network

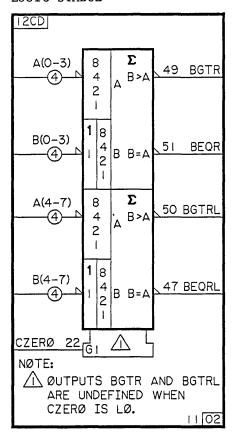
The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and

12CD-10 (Cont d)

designated as operand A. The lower highway comes from B(0-7). It is gated into the compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when B is greater than A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when B is equal to A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.

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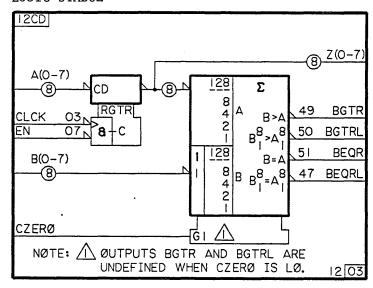


BIAS LØ = CLCK, EN, DUAL, SEL(I) BIAS HI = NTST, SEL(O)

OPERATIONAL DESCRIPTION

The 12CD-11 contains two 4-bit compare networks. Each compare network has two highwayed inputs. The A inputs enter the compare network and are weighted binarily 1-8, and designated as operand A. The B inputs are gated into the compare networks by CZERO HI, weighted binarily 1-8, and designated as operand B.

Each network aligns the two operands according to their weights and compares them. BGTR and BGRTL will be active (LO) when B is greater than A. BEQR and BEQRL will be active when B is equal to A.

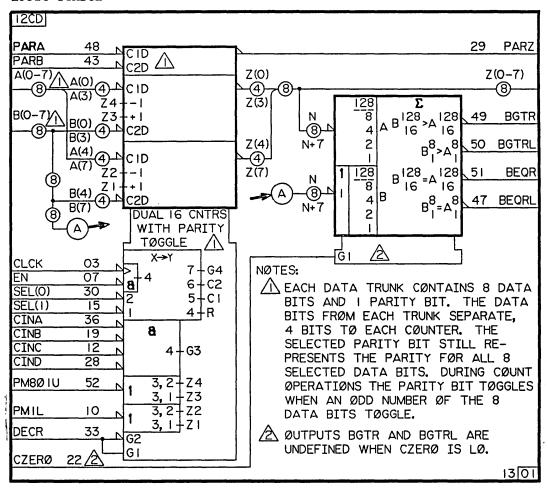


BIAS LØ = NTST, CINA, CINB, CINC, CIND, SEL(I) BIAS HI = DUAL, SEL(O), PMIL, PM2, PM4, PM8ØIU

OPERATIONAL DESCRIPTION

CLCK and EN clock the A(0-7) input highway into a register. The output of the register goes to output pins Z(0-7) and to a compare network where it is weighted binarily 1 through 128 and designated as operand A. Input highway B(0-7) is gated into the compare network by CZERO HI, weighted binarily 1 through 128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when B is greater than A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active when B is equal to A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.



BIAS LØ = DUAL, NTST BIAS HI = PM2, PM4

OPERATIONAL DESCRIPTION

The 12CD-13 contains two major functional elements, a counter and a compare network.

Counter

The counter symbol divides into 4 areas from top to bottom. The top area is a parity bit register with two inputs, PARA and PARB. When the counter is loaded, Cl or C2 clocks in the selected parity bit which represents the parity for the selected 8-bit data byte. Internal control (not shown) causes the parity bit to toggle when an odd number of bits in the 8-bit byte toggle. PARZ is the parity bit output.

12CD-13 (Cont'd)

The next two areas below the parity are each 4-bit counters. Each counter has two 4-bit highwayed inputs (A and B) and one 4-bit highwayed output (Z). Each counter can increment or decrement by 1 under the control of the Z inputs which are interconnections to the common control block. Each counter has a modulus of 16 (0-15) and counts in a circular manner; i.e., one count beyond 15 is 0, one count less than 0 is 15.

The bottom area is the common control block which contains the control for both counters.

SEL(0,1), EN, and CLCK control the major functions of the counters. A translation of 4 clears both counters and the parity bit register, 5 clocks in A data to each counter and the parity bit for A, 6 clocks in B data to each counter and the parity bit for B, and 7 initiates a count operation (G4 active).

CINA, B, C, and D are chip enables. They must all be LO to enable a count operation. G3 will be active when a count operation is initiated (G4 active) and the chip is enabled (CINA-D LO).

DECR controls the direction of the count for both counters. When DECR is LO, the counters decrement (G2 active). When DECR is HI, the counters increment (G1 active).

PM801U enters an OR function which controls the upper 4-bit counter. PM1L enters an OR function which controls the lower 4-bit counters.

Count Operation

PM801U, G3 (count initiated and chip enabled) and G2 (decrement) all active will make Z4 active. Z4 connects to the upper counter and decrements it by 1.

PM801U, G3 and G1 (increment) all active will make Z3 active. Z3 connects to the upper counter and increments it by l.

PM1L and G1-3 control the lower counter in the same manner as PM801U and G1-3 control the upper counter.

Compare Network

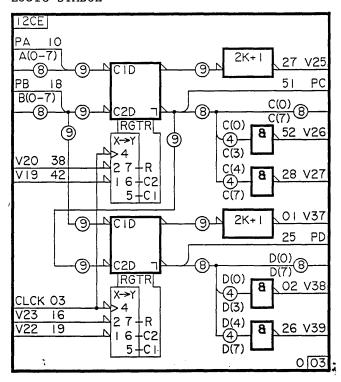
The compare network has two 8-bit highwayed inputs. The upper highway is the data output from the counter. It enters the compare network and is weighted binarily 1 through 128 and designated as operand A. The lower highway comes from B(0-7). It is gated into the compare network by CZERO HI, weighted binarily 1-128, and designated as operand B.

The two operands are aligned according to their weights and compared. Output BGTR will be active (LO) when the 4 most-significant bits of B are greater than the 4 most-significant bits of A. BGTRL will be active when the 4 least-significant bits of B are greater than the 4 least-significant bits of A. BEQR will be active (LO) when the 4 most-significant bits of B are equal to the 4 most-significant bits of A. BEQRL will be active when the 4 least-significant bits of B are equal to the 4 least-significant bits of A.

12CE

PIN	REAL	VIRT
NAM	1	PIN
A(0)	45	V03
A(1) A(2)	46 44	V05
A(2)	44 43	V07 V09
A(4)	34	V11
A(5)	33	V13
A(6)	35 36	V15
A(7) B(0)	36 12	V17 V04
B(1)	08	V04 V06
B(2)	41	V08
B(3)	09	V10
B(4)	17 15	V12 V14
B(5) B(6)	15 20	V14 V16
B(7)	37	V18
CLC		V24
PA	10	V01 V02
PB V19	18 42	V02 V19
V20	38	V20
V21	11	V21
V22 V23	19 16	V22 V23
-		
C(0) C(1)	49 50	V29 V30
C(2)	47	V31
C(3)	48	V32
C(4)	29	V33
C(5)	30 31	V34 V35
C(7)	32	V36
D(0)	07	V41
D(1)	90	V42
D(2) D(3)	05 04	V43 V44
D(4)	22	V45
D(5)	21	V46
D(6)	24 23	V47 V48
PC	23 51	V48 V28
PD	25	V 28 V 40
V25	27	V25
V26	52	V26
V27 V37	28 01	V27 V37
V37	02	V37
V39	26	V39

	•		
		·	



BIAS LØ = NØNE BIAS HI = V21

OPERATIONAL DESCRIPTION

Upper Register

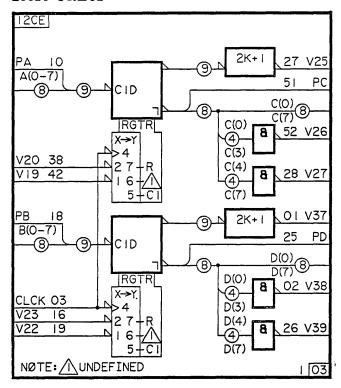
Input pins V19, V20, and CLCK control the upper register. A control translation of 5 clocks inputs A(0-7) and PA, 6 clocks inputs B(0-7) and PB, and 7 clears the register.

The register has two sets of outputs, non-delayed (upper output highway), and delayed (lower output highway). Outputs to the lower highway do not change state to reflect the new register contents until the active dock modifier (Cl or C2) becomes inactive. The CLCK input is dynamic, therefore, the clock modifier is only active for the first 2.5 ns following the clocks transition to L0.

Output pin V25 is active (LO) when an odd number of parity checker inputs are active. Output pins V26 and V27 are active (LO) when the delayed outputs of the register C(0-3) and C(4-7) are active (HI), respectively.

Lower Register

Input pins V22, V23, and CLCK control the lower register. The lower register and its outputs operate in the same manner as the upper register and its outputs. Refer to the Upper Register.



BIAS LØ = NØNE BIAS HI = V21

OPERATIONAL DESCRIPTION

Upper Register

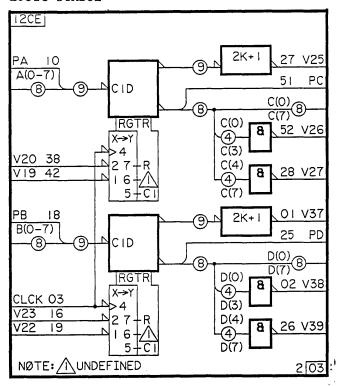
Input pins V19, V20, and CLCK control the upper register. A control translation of 5 clocks inputs A(0-7) and PA, 6 is undefined, and 7 clears the register.

The register has two sets of outputs, nondelayed (upper output highway), and delayed (lower output highway). Outputs to the lower highway do not change state to reflect the new register contents until the active dock modifier (Cl) becomes inactive. The CLCK input is dynamic, therefore, the clock modifier is only active for the first 2.5 ns following the clocks transition to LO.

Output pin V25 is active (L0) when an odd number of parity checker inputs are active. Output pins V26 and V27 are active (L0) when the delayed outputs of the register C(0-3) and C(4-7) are active (HI), respectively.

Lower Register

Input pins V22, V23 and CLCK control the lower register. The lower register and its outputs operate in the same manner as the upper register and its outputs. Refer to the Upper Register.



BIAS LØ = V21 BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Upper Register

Input pins V19, V20, and CLCK control the upper register. A control translation of 5 clocks inputs A(0-7) and PA, 6 is undefined, and 7 clears the register.

Output pin V25 is active (LO) when an odd number of parity checker inputs are active. Output pins V26 and V27 are active (LO) when inputs C(0-3) and C(4-7) are active (HI), respectively.

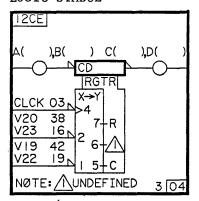
Lower Register

Input pins V22, V23 and CLCK control the lower register. A control translation of 5 clocks inputs B(0-7) and PB, 6 is undefined, and 7 clears the register.

Output pin V37 is active (LO) when an odd number of parity checker inputs are active. Output pins V38 and V39 are active (LO) when input pins D(0-3) and D(4-7) are active (HI), respectively.

12CE-3 16-Bit Register.

LOGIC SYMBOL

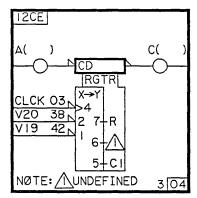


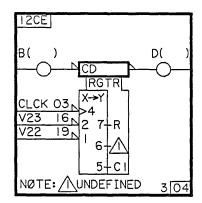
INPUT PINS ARE: A(O-7), B(O-7) ØUTPUT PINS ARE: C(O-7), D(O-7) BIAS LØ = V21, PA, PB BIAS HI = NØNE TERMINATE = V26, V27, V38, V39 OPERATIONAL DESCRIPTION

Input pins V20 and V23 (tied together), V19 and V22 (tied together), and CLCK control the register. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears register.

12CE-3 (Cont'd)

LOGIC SYMBOL

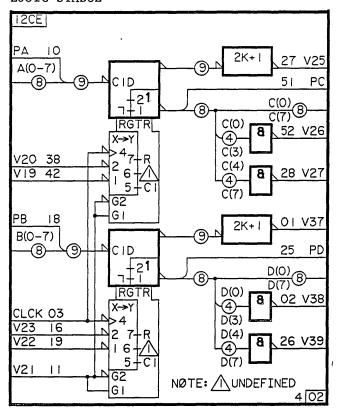




BIAS LØ = V21, PA, PB BIAS HI = NØNE TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Input pins V19, V20, and CLCK or V22, V23, and CLCK control their respective registers. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.



BIAS NØNE

OPERATIONAL DESCRIPTION

Upper Register

Input pins V19, V20 and CLCK control the upper register. Input pin V21 selects between the delayed and not delayed register outputs to the lower output highway. Input pin V21 HI gates the delayed register output and V21 LO gates the non-delayed register output. A control translation of 5 clocks data inputs A(0-7) and PA, 6 is undefined, and 7 clears the register.

Delayed register outputs do not change state to reflect the new register contents until the active clock modifier (Cl) becomes inactive. The CLCK input is dynamic, therefore, the clock modifier is only active for the first 2.5 ns following the clocks transition to LO.

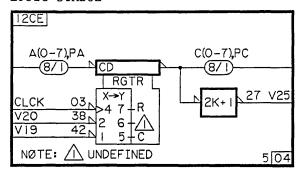
Output pin V25 is active (LO) when an odd number of parity checker inputs are active. Output pins V26 and V27 are active (LO) when input pins C(0-3) and C(4-7) are active (HI), respectively.

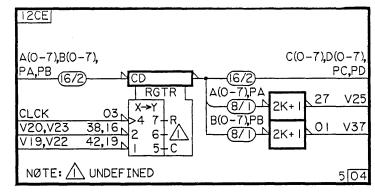
Lower Register

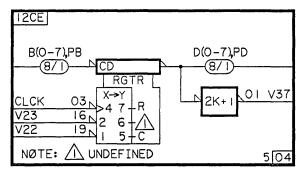
Input pins V22, V23, and CLCK control the lower register. The lower register and its outputs operate in the same manner as the uppper register and its outputs. Refer to the Upper Register.

12CE-5 Registers with Parity.

LOGIC SYMBOL







BIAS LØ = V21 BIAS HI = NØNE

TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Two 8-Bit Registers

Input pins V19, V20, and CLCK or V22, V23, and CLCK control their respective registers. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.

Output pins V25 and V37 are active (LO) when an odd number of parity checker inputs are active.

16-Bit Register with Parity

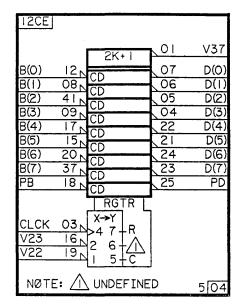
Input pins V19 and V22 (tied together), V20 and V23 (tied together), and CLCK control the register. A control translation of 5 clocks inputs A(0-7), B(0-7), PA, and PB, 6 is undefined, and 7 clears the register.

Output pins V25 and V37 are active (L0) when an odd number of parity checker inputs (A(0-7) and PA, or B(0-7) and PB) are active, respectively.

12CE-5 (Cont'd)

LOGIC SYMBOL

12CE				
	1	2K+ I	27	V25
A(O)	45 _N		49	C(O)
A(1)	46 _N	CD	50	C(1)
A(2)	44	CD	47	C(2)
A(3)	43 _N	CD	48	C(3)
Δ(4)	34 _N	CD	29	C(4)
A(5)	33 _~	CD	30	C(5)
A(6)	35 _N	CD	31	C(6)
Δ(7)	36 _N	CD	32	C(7)
PA	0	CD	51	PC
CLCK V20 V19	03 _N 38 _N 42 _N	RGTR X→Y >4 7 + R 2 6 + \(\) 5 + C		
NØTE	: 🛆	UNDEFINE	ED	504



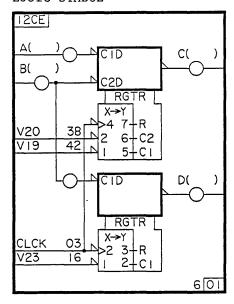
OPERATIONAL DESCRIPTION

Input pins V19, V20, and CLCK or V22, V23, and CLCK control their respective registers. A control translation of 5 clocks input data A(0-7), PA, and B(0-7), PB, 6 is undefined, and 7 clears the register.

The 12CE-5 divides into two areas; the common control block and the common output block.

The common control block (above the double line) contains the odd parity checker. The common output block monitors the outputs of the register.

Output pins V25 and V37 are active (LO) when an odd number of parity checker inputs are active.



BIAS LØ = V21, V22 BIAS HI = NØNE TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

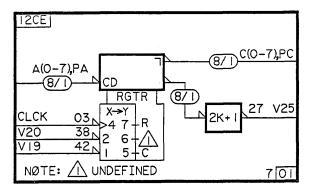
Upper Register

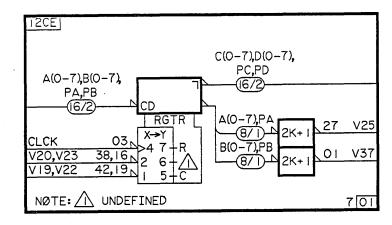
Input pins V19, V20, and CLCK control the upper register. A control translation of 5 clocks input A, 6 clocks input B, and 7 clears the register.

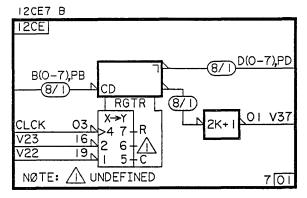
Lower Register

Input pins V23 and CLCK control the lower register. A control translation of 2 clocks input B, and 3 clears the register.

60458120 B







BIAS LØ = NØNE BIAS HI = V21

TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Two 8-Bit Registers with Parity

Input pins V19, V20, and CLCK control the register receiving the A input data. Input pins V22, V23, and CLCK control the register receiving the B input data. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.

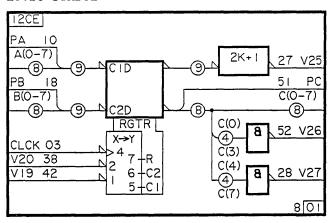
Each register has two sets of outputs, nondelayed (lower output highway), and delayed (upper output highway). Outputs to the upper highway do not change state to reflect the new register contents until the active dock modifier (C) becomes inactive. The CLCK input is dynamic, therefore, the clock modifier is only active for the first 2.5 ns following the clocks transition to LO.

The registers delay the upper outputs, and pass the undelayed lower outputs to their respective parity checkers.

Output pins V25 and V37 are active (LO) when an odd number of their respective parity checker inputs are active.

16-Bit Register with Parity

Input pins V19 and V22 (tied together), V20 and V23 (tied together), and CLCK control the register. The 16-bit register and its outputs operate in the same manner as the 8-bit registers and their outputs. Refer to the 8-Bit Registers with parity.

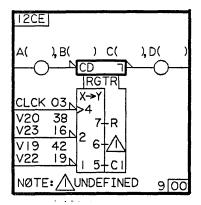


BIAS LØ = V2| BIAS HI = NØNE TERMINATE V38, V39

OPERATIONAL DESCRIPTION

Input pins V19, V20, and CLCK control the register. A control translation of 5 clocks inputs A(0-7) and PA, 6 clocks inputs B(0-7) and PB, and 7 clears the register.

Output pin V25 is active (LO) when an odd number of parity checker inputs are active. Output pins V26 and V27 are active (LO) when inputs C(0-3) and C(4-7) are active (HI), respectively.



INPUT PINS ARE: A(O-7), B(O-7) ØUTPUT PINS ARE: C(O-7), D(O-7)

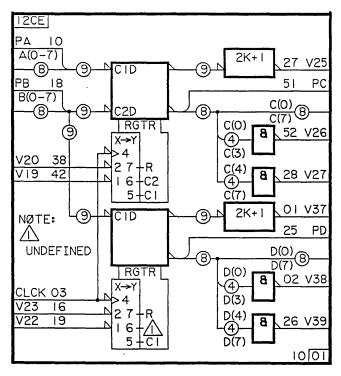
BIAS LØ = PA, PB BIAS HI = V21

TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Input pins V19 and V22 (tied together), V20 and V23 (tied together), and CLCK control the register. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.

The output of the register is delayed until the active clock modifier (C1) becomes inactive. The CLCK input is dynamic, therefore, the clock modifier is only active for the first 2.5 ns following the clocks transition to LO.



BIAS LØ = V21 BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Upper Register

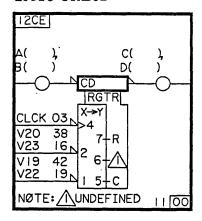
Input pins V19, V20 and CLCK control the upper register. A control translation of 5 clocks inputs A(0-7) and PA, 6 clocks B(0-7) and PB, and 7 clears the register.

Output pin V25 is active (LO) when an odd number of parity checker inputs are active. Output pins V26 and V27 are active (LO) when C(0-3) and C(4-7) are active (HI), respectively.

Lower Register

Input pins V22, V23, and CLCK control the lower register. A control translation of 5 clocks B(0-7) and PB, 6 is undefined, and 7 clears the register.

Output pin V37 is active (LO) when an odd number of parity checker inputs are active. Output pins V38 and V39 are active (LO) when inputs D(0-3) and D(4-7) are active (HI), respectively.

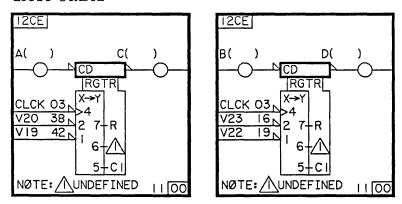


 I. INPUT PINS ARE: A(0-7, PA, B(0-7), PB ØUTPUT PINS ARE: C(0-7), PC, D(0-7), PD

BIAS LØ = V21 BIAS HI = NØNE TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Input pins V19 and V22 (tied together), V20 and V23 (tied together), and CLCK control the register. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.

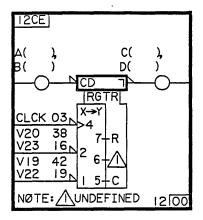


 INPUT PINS ARE: A(0-7), PA, B(0-7), PB ØUTPUT PINS ARE: C(0-7), PC, D(0-7), PD

BIAS LØ = V2IBIAS HI = NØNETERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Input pins V19, V20, and CLCK or V22, V23, and CLCK control their respective registers. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.



BIAS LØ = NØNE

BIAS HI = V21 TERMINATE = V26, V27, V38, V39

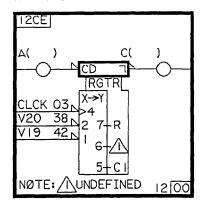
NØTES:

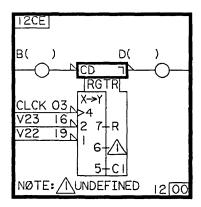
I. INPUT PINS ARE: A(0-7, PA, B(0-7), PB ØUTPUT PINS ARE: C(0-7), PC, D(0-7), PD

OPERATIONAL DESCRIPTION

Input pins V19 and V22 (tied together), V20 and V23 (tied together), and CLCK control the register. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.

The register outputs do not change state until the active clock modifier (C) becomes inactive. The CLCK input is dynamic, therefore, the clock modifier is only active for the first 2.5 ns following the clocks transition to LO.





INPUT PINS ARE: A(0-7), PA, B(0-7), PB ØUTPUT PINS ARE: C(0-7), PC, D(0-7), PD

BIAS LØ = NØNE BIAS HI = V21

TERMINATE = V26, V27, V38, V39

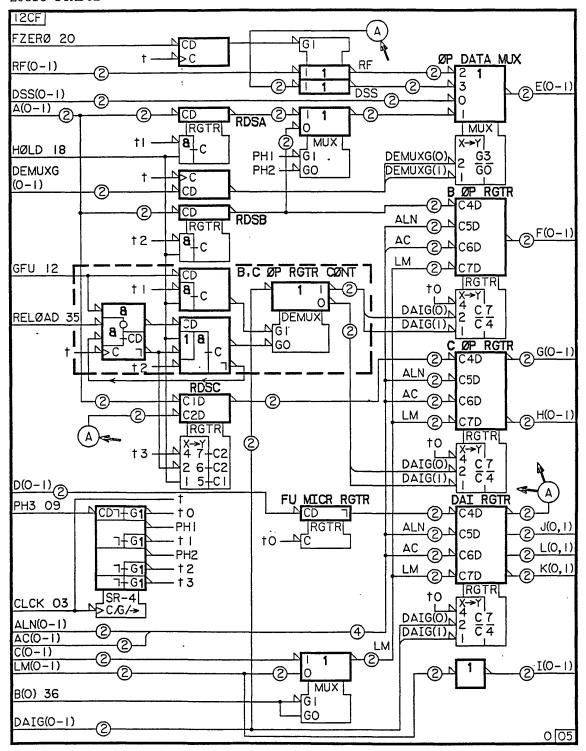
OPERATIONAL DESCRIPTION

Input pins V19 and V22 and CLCK or V22, V23, and CLCK control their respective registers. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.

The register outputs do not change state until the active clock modifier (C) becomes inactive. The CLCK input is dynamic, therefore, the clock modifier is only active for the first 2.5 ns following the clocks transition to LO.

12CF

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	37	V13
A(1)	52	V15
AC(0)	33	V31
AC(1)	46	V32
ALN(0)	38	V33
ALN(1)	43	V34
B(0)	36	V12
B(1) C(0) C(1)	15 41 48 03	V14 V43 V44 V45
D(1)	42 44	V37 V38 V29
DAIG(1) DEMUXO	27 G(0)10 G(1)08	V30 V01 V02
DSS(0)	16	V07
DSS(1)	11	V10
FZERO	20	V03
GFU	12	V35
HOLD	18	V47
LM(0)	32	V41
LM(1)	45	V42
MODE	34	V11
PH3	09	V46
RELOAD	35	V36
RF(0)	17	V08
RF(1)	06 07	V09 V18
E(0)	19	V05
E(1)	22	V06
F(0)	30	V16
F(1)	31	V17
G(0)	51	V19
G(1)	04	V20
H(0)	01	V23
H(1)	02	V24
I(0)	50	V39
I(1)	49	V40
J(0)	23	V25
J(1)	21	V26
K(0)	25	V27
K(1)	29	V28
L(0) L(1) U	26 24 05 47	V21 V22 V48 V04



BIAS LØ = NØNE

BIAS HI = MØDE, B(1)

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12CF-0 (Cont'd)

OPERATIONAL DESCRIPTION

The 12CF-0 performs major register and mux functions in the Operand Issue. These functions are the RDSA, RDSB, and RDSC registers, the Operand Data Mux, B and C Operand Registers, and the DAI Register. The 12CF-0 also contains a clock network (lower left symbol) which produces phased clocks for internal use, a control network for the B and C Operand Registers, and miscellaneous registers and mux functions. The miscellaneous registers and mux functions will be explained along with the major functions.

Clock Network

The clock network consists of a shift register which loads a single bit (input pin PH3) and shifts it down through 4-bit positions. Each transition to LO of the CLCK input activates the C and G modifiers and causes a right shift of 1-bit position. The C (clock) modifier clocks in the state of the PH3 input to the top bit position of the shift register. The G (gating) modifier gates the delayed outputs from the shift register to produce the tO, t1, t2, and t3 clocks. The shift right causes the previous contents of each bit position to shift down 1-bit position. The PH1 and PH2 clocks are not gated or delayed and therefore always follow the contents of their respective bit positions. The timing diagram on the following page shows the inputs to the clock network and its outputs.

RDSA Register (second symbol from the top on the left side)
When input pin HOLD is HI, new data will clock into the RDSA Register each Tl time. When
HOLD is LO, the clock modifier C cannot become active at Tl time and the register holds the
data.

RDSB Register

When input pin HOLD is HI, new data will clock into the RDSB Register each T2 time. When HOLD is LO, the clock modifier C cannot become active at T2 time and the register holds the data.

RDSC Register

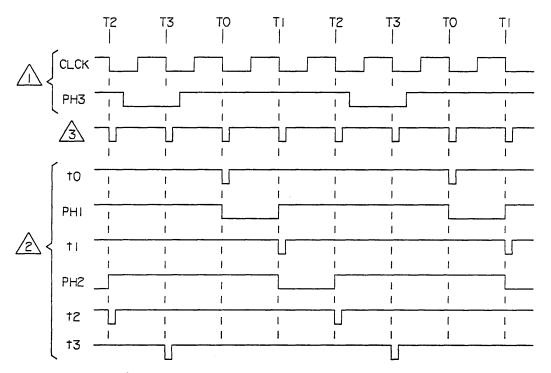
The RDSC Register has two highwayed inputs. The top highway is the normal data path and is clocked in at t3 time by a control translation of 5. Note that HOLD must be HI in order to clock in the normal data path. When HOLD is LO, the RDSC Register either holds its contents at T3 time (translation of 4) or clocks in the lower highway (translation of 6).

The lower highway is used for reloading the RDSC Register during a functional unit shortstop of the C operand when HOLD is LO. In this case a translation of 6 will clock in the lower highway which comes from the output of the DAI Register. A translation of 7 also clocks in the lower highway, but this translation is not used.

The B, C Operand Register Control paragraph explains the control for the selection of the lower data path to the RDSC Register.

Operand Data Mux (symbol in the upper right corner)
Two select signals control the selection of one of 4 input highways. These two select signals enter the array on pins DEMUXG(0) and (1) and are clocked into a register controlled by clock (t) from pin CLCK.

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NØTES: \(\int \) INPUTS TØ THE CLØCK CKT IN THE CF ARRAY.

CLØCK CKT ØUTPUTS (INTERNAL TØ THE CF ARRAY).

ØUTPUT ØF THE ØN-CHIP CLØCK SHAPER. THE CLØCK SHAPER FØRMS A 2.5 NS PULSE ØN THE LEADING EDGE ØF THE ACTIVE LØ CLØCK INPUT (CLCK). THE ANSI SYMBØL USES THE DYNAMIC INDICATØR (>) TØ SHØW THIS CLØCK SHAPER.

12CF-0 (Cont'd)

A control translation of 0 selects data from input pins DSS(0-1).

A control translation of 1 selects the output from a 2-input mux. The mux selects RDSA or RDSB data under the control of PH1 and PH2 from the clock network. RDSA data goes through the mux during phase 1 (PH1) time and RDSB data goes through the mux during phase 2 (PH2) time.

A control translation of 2 selects data from input pins RF(0-1). This data passes through a gate which can allow it to pass (Gl active) or block it forcing zeros (Gl inactive). The control for this gate enters pin FZERO and is clocked into a register by clock (t) from pin CLCK. When the register is active, its output is HI, deactivating Gl in the gate and forcing zeros on the gate's output highways. When the register is inactive, its output is LO, activating Gl in the gate and allowing the highways to pass.

A control translation of 3 selects data from the output of the DAI Register. The DAI Register is on the input to the Register File and the Operand Data Mux is on the output of the Register File. Thus, a control translation of 3 causes a Register File shortstop. The data from the DAI Register also passes through the gate which can force zeros.

B Operand Register

Two select signals and tO clock select one of 4 input highways and clock the contents into the register. The select signals come from a DEMUX which is explained in the B, C Operand Register Control paragraph.

A control translation of 4 clocks in data from the RDSB Register. This is the normal path where the contents of the RDSB Register become the B operand sent to the ALN.

Control translations of 5, 6, and 7 clock in data from the ALN, AC, and LM, respectively. These are functional unit shortstop paths because the data is being taken from the output paths of the functional units and sent to the input of the ALN.

C Operand Register

Two select signals and tO clock select one of 4 input highways and clock the contents into the register. The select signals come from a DEMUX which is explained in the B, C Operand Register Control paragraph.

A control translation of 4 clocks in data from the RDSC Register. This is the normal path where the contents of the RDSC Register become the C operand sent to the ALN or to Address Control.

Control translations of 5, 6 and 7 clock in data from the ALN, AC, and LM, respectively. These are functional unit shortstop paths because the data is being taken from the output paths of the functional units and sent to the input of the ALN or AC.

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B, C Operand Register Control (enclosed by dashed line)

The major functions of the B, C Operand Register Control are the B Operand Select Enable Register (top CD function), the C Operand Select Enable flip-flop (bottom CD function), the Reload Control Register (left CD function), and the DEMUX.

There are 4 modes of operation. For descriptive purposes these modes are called Normal, Functional Unit Shortstop, Hold, and Reload.

Normal

Normal operation implies that operands are flowing smoothly from the RDSB and RDSC Registers to the B and C Operand Registers with no interruptions of flow (holds).

Inputs HOLD, GFU (functional unit shortstop), and RELOAD are all HI. Thus all three CD functions in the B, C Operand Register Control are inactive. This makes GO and Gl in the DEMUX inactive forcing the DAIG(0-1) controls to zeros for both the B and C Operand Registers. At TO time the B and C Operand Register Control translators will both be 4, clocking in data from the RDSB and RDSC Register respectively.

Functional Unit Shortstop

During a functional unit shortstop operation, the B and/or C Operand Registers receive data from the output paths of the functional units. This data is tapped off at the input to the DAI Register. The DAIG(0-1) inputs select the shortstopped functional unit (ALN, AC, or LM) and the DEMUX routes this control to the proper operand register(s).

Inputs HOLD and RELOAD are HI and GFU (functional unit shortstop) is LO. When GFU is LO during the tl clock, the B Operand Select Enable Register (top CD function) is set (active). When GFU is LO during the t2 clock, the C Operand Select Enable Flip-Flop (lower CD function) is set. This activates GO and/or Gl in the DEMUX and gates the DAIG(0-1) control to the B and/or C Operand Registers which at TO time clock in the selected functional unit.

Hold

The HOLD input, when LO, interrupts the flow of data during normal or functional unit shortstop operations. This is due to the Address Control or Local Memory unit not being able to accept new operands. Thus the RDSA, RDSB, and RDSC Registers and the B, C Operand Register Control must hold until the functional unit can again accept operands.

When the HOLD input is LO, the C (clock) modifiers for RDSA, RDSB, RDSC and B Operand Select Enable Registers, and the C Operand Select Enable Flip-Flop are all inactive causing these circuits to hold their contents. When the C Operand Select Enable Flip-Flop is set (functional unit shortstop of C) while HOLD is LO, a reload operation will take place. Refer to Reload.

Reload .

A reload operation takes place when there is a functional unit shortstop of C (C Operand Select Enable Flip-Flop set) and the HOLD input becomes LO. The reload operation will reset the C Operand Select Enable Flip-Flop and clock DAI Register output data into the RDSC Register.

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12CF-0 (Cont'd)

When the RELOAD input goes LO, the AND gate it enters will become active because the C Operand Select Enable Flip-Flop is set. The active AND gate deactivates the data input to the C Operand Select Enable Flip-Flop and also allows the t clock (pin CLCK) to set the Reload Control Register. The Reload Control Register then performs two functions. First, it enables the clock circuits for the C Operand Select Enable Flip-Flop so at T2 time it will reset. Thus GO in the DEMUX will become inactive and force zeros to the C Operand Register control selecting the data path from the RDSC Register. Second, at T3 time the RDSC Register control translator will decode a 6 which will clock in data from the output of the DAI Register. Since the C Operand Select Enable Flip-Flop resets at T2 time, the AND gate which RELOAD entered becomes inactive. This allows the Reload Control Register to clear the next time clock goes LO.

DAI Register

Two select signals and the tO clock select one of 4 input highways and clock the contents into the register.

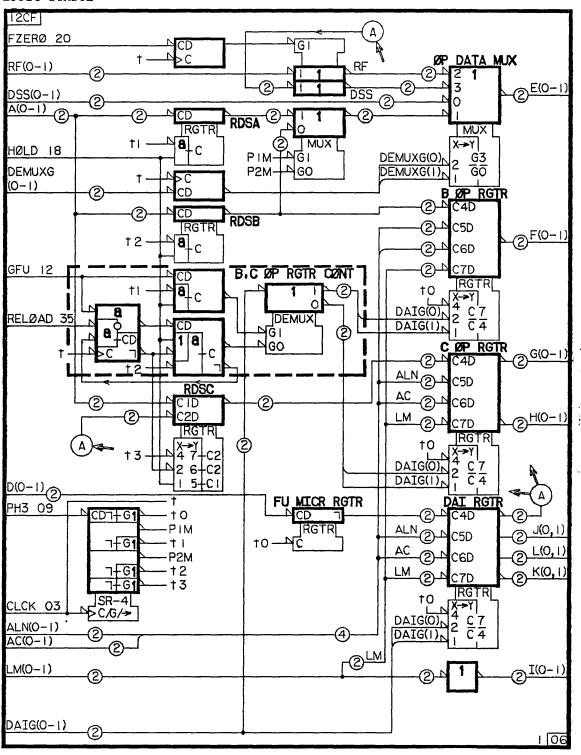
A control translation of 4 clocks in the output of the Functional Unit Micrand Register. This register clocked in data from pins D(0-1) at the previous TO time.

Control translations of 5, 6, and 7 clock in data from the ALN, AC, and LM, respectively. The LM data comes through a mux controlled by pin B(0). When B(0) is LO, the LM data comes from pins C(0-1). When B(0) is HI, the LM data comes from pins LM(0-1).

Data which enters on pins LM(0-1) also passes unaltered to output pins I(0-1).

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BIAS LØ = NØNE

BIAS HI = MØDE. B(O-1)

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12CF-1 (Cont'd)

OPERATIONAL DESCRIPTION

The 12CF-1 performs major register and mux functions in the Operand Issue. These functions are the RDSA, RDSB, and RDSC Registers, the Operand Data Mux, B and C Operand Registers, and the DAI Register. The 12CF-1 also contains a clock network (lower left symbol) which produces phased clocks for internal use, a control network for the B and C Operand Registers, and miscellaneous registers and mux functions. The miscellaneous registers and mux functions will be explained along with the major functions.

Clock Network

The clock network consists of a shift register which loads a single bit (input pin PH3) and shifts it down through 4-bit positions. Each transition to LO of the CLCK input activates the C and G modifiers and causes a right shift of 1-bit position. The C (clock) modifier clocks in the state of the PH3 input to the top bit position of the shift register. The G (gating) modifier gates the delayed outputs from the shift register to produce the tO, t1, t2, and t3 clocks. The shift right causes the previous contents of each bit position to shift down 1-bit position. The PH1 and PH2 clocks are not gated or delayed and therefore always follow the contents of their respective bit positions. The timing diagram on the following page shows the inputs to the clock network and its outputs.

RDSA Register (second symbol from the top on the left side)
When input pin HOLD is HI, new data will clock into the RDSA Register each Tl time. When HOLD is LO, the clock modifier C cannot become active at Tl time and the register holds the data.

RDSB Register

When input pin HOLD is HI, new data will clock into the RDSB Register each T2 time. When HOLD is LO, the clock modifier C cannot become active at T2 time and the register holds the data.

RDSC Register

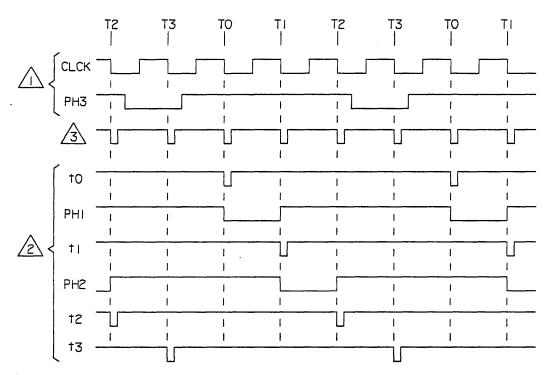
The RDSC Register has two highwayed inputs. The top highway is the normal data path and is clocked in at T3 time by a control translation of 5. Note that HOLD must be HI in order to clock in the normal data path. When HOLD is LO, the RDSC Register either holds it contents at T3 time (translation of 4) or clocks in the lower highway (translation of 6).

The lower highway is used for reloading the RDSC Register during a functional unit shortstop of the C operand when HOLD is LO. In this case a translation of 6 will clock in the lower highway which comes from the output of the DAI Register. A translation of 7 also clocks in the lower highway, but this translation is not used.

The B, C Operand Register Control paragraph explains the control for the selection of the lower data path to the RDSC Register.

Operand Data Mux (symbol in the upper right corner)
Two select signals control the selection of one of 4 input highways. These two select signals enter the array on pins DEMUXG (0) and (1) and are clocked into a register controlled by clock (t) from pin CLCK.

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NØTES: \(\int \) INPUTS TØ THE CLØCK CKT IN THE CF ARRAY.

CLØCK CKT ØUTPUTS (INTERNAL TØ THE CF ARRAY).

ØUTPUT ØF THE ØN-CHIP CLØCK SHAPER. THE CLØCK SHAPER FØRMS A 2.5 NS PULSE ØN THE LEADING EDGE ØF THE ACTIVE LØ CLØCK INPUT (CLCK). THE ANSI SYMBØL USES THE DYNAMIC INDICATØR (>) TØ SHØW THIS CLØCK SHAPER.

12CF-1 (Cont'd)

A control translation of 0 selects data from input pins DSS(0-1).

A control translation of 1 selects output from a 2-input mux. The mux selects RDSA or RDSB data under the control of PH1 and PH2 from the clock network. RDSA data goes through the mux during phase 1 (PH1) time and RDSB data goes through the mux during phase 2 (PH2) time.

A control translation of 2 selects data from input pins RF(0-1). This data passes through a gate which can allow it to pass (Gl active) or block it forcing zeros (Gl inactive). The control for this gate enters pin FZERO and is clocked into a register by clock t from pin CLCK. When the register is active, its output is HI, deactivating Gl in the gate and forcing zeros on the gate's output highways. When the register is inactive, its output is LO, activating Gl in the gate and allowing the highways to pass.

A control translation of 3 selects data from the output of the DAI Register. The DAI Register is on the input to the Register File and the Operand Data Mux is on the output of the Register File. Thus a control translation of 3 causes a Register File shortstop. The data from the DAI Register also passes through the gate which can force zeros.

B Operand Register

Two select signals and tO clock select one of 4 input highways and clock the contents into the register. The select signals come from a DEMUX which is explained in the B, C Operand Register Control paragraph.

A control translation of 4 clocks in data from the RDSB Register. This is the normal path where the contents of the RDSB Register become the B operand sent to the ALN.

Control translations of 5, 6, and 7 clock in data from the ALN, AC, and LM respectively. These are functional unit shortstop paths because the data is being taken from the output paths of the functional units and sent to the input of the ALN.

C Operand Register

Two select signals and t0 clock select one of 4 input highways and clock the contents into the register. The select signals come from a DEMUX which is explained in the B, C Operand Register Control paragraph.

A control translation of 4 clocks in data from the RDSC Register. This is the normal path where the contents of the RDSC Register become the C operand sent to the ALN or to Address Control.

Control translations of 5, 6, and 7 clock in data from the ALN, AC, and LM, respectively. These are functional unit shortstop paths because the data is being taken from the output paths of the functional unit and sent to the input of he ALN or AC.

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B, C Operand Register Control (enclosed by dashed line)

The major functions of the B, C Operand Register Control are the B Operand Select Enable Register (top CD function), the C Operand Select Enable flip-flop (bottom CD function), the Reload Control Register (left CD function), and the DEMUX.

There are 4 modes of operation. For descriptive purposes these modes are called Normal, Functional Unit Shortstop, Hold, and Reload.

Normal

Normal operation implies that operands are flowing smoothly from the RDSB and RDSC Registers to the B and C Operand Register with no interruptions of flow (holds).

Inputs HOLD, GFU (functional unit shortstop), and RELOAD are all HI. Thus all three CD functions in the B, C Operand Register Control are inactive. This makes GO and Gl in the DEMUX inactive forcing the DAIG(0-1) controls to zeros for both the B and C Operand Registers. At TO time the B and C Operand Registers Control translators will both be 4, clocking in data from the RDSB and RDSC Registers, respectively.

Functional Unit Shortstop

During a functional unit shortstop operation, the B and/or C Operand Registers receive data from the output paths of the functional units. This data is tapped off at the input to the DAI Register. The DAIG(0-1) inputs select the shortstopped functional unit (ALN, AC, or LM) and the DEMUX routes this control to the proper operand register(s).

Inputs HOLD and RELOAD are HI and GFU (functional unit shortstop) is LO. When GFU is LO during the tl clock, the B Operand Select Enable Register (top CD function) is set (active). When GFU is LO during the t2 clock, the C Operand Select Enable Flip-Flop (lower CD function) is set. This activates GO and/or Gl in the DEMUX and gates the DAIG(0-1) control to the B and/or C Operand Registers which at TO time clock in the selected functional unit.

Hold

The HOLD input, when LO, interrupts the flow of data during normal or functional unit shortstop operations. This is due to the Address Control or Local Memory unit not being able to accept new operands. Thus the RDSA, RDSB, and RDSC Registers and the B, C Operand Register Control must hold until the functional unit can again accept operands.

When the HOLD input is LO, the C (clock) modifiers for RDSA, RDSB, RDSC and B Operand Select Enable Registers, and the C Operand Select Enable Flip-Flop are all inactive causing these circuits to hold their contents. When the C Operand Select Enable Flip-Flop is set (functional unit shortstop of C) while HOLD is LO, a reload operations will take place. Refer to Reload.

Roload

A reload operation takes place when there is a functional unit shortstop of C (C Operand Select Enable Flip-Flop set) and the HOLD input becomes LO. The reload operation will reset the C Operand Select Enable Flip-Flop and clock DAI Register output data into the RDSC Register.

12CF-1 (Cont'd)

When the RELOAD input goes LO, the AND gate it enters will become active because the C Operand Select Enable Flip-Flop is set. The active AND gate deactivates the data input to the C Operand Select Enable Flip-Flop and also allows the t clock (pin CLCK) to set the Reload Control Register. The Reload Control Register then performs two functions. First, it enables the clock circuits for the C Operand Select Enable Flip-Flop so at T2 time it will reset. Thus GO in the DEMUX will become inactive and force zeros to the C Operand Register control selecting the data path from the RDSC Register. Second, at T3 time the RDSC Register control translator will decode a 6 which will clock in data from the output of the DAI Register. Since the C Operand Select Enable Flip-Flop resets at T2 time, the AND gate which RELOAD entered becomes inactive. This allows the Reload Control Register to clear the next time clock goes LO.

DAI Register

Two select signals and the t0 clock, select one of 4 input highways and clock the contents into the register.

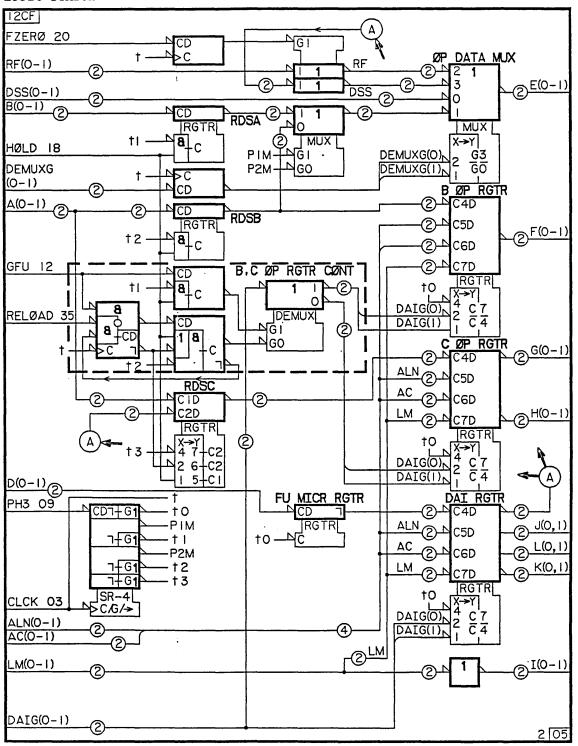
A control translation of 4 clocks in the output of the Functional Unit Micrand Register. This register clocked in data from pins D(0-1) at the previous TO time.

Control translation of 5, 6 and 7 clock in data from the ALN, AC, and LM respectively.

Data which enters on pins LM(0-1) also passes unaltered to output pins I(0-1).

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LOGIC SYMBOL



BTAS LØ = MØDF BIAS HI = NØNE

OPERATIONAL DESCRIPTION

The 12CF-2 performs major register and mux functions in the Operand Issue area. These functions are the RDSA, RDSB, and RDSC registers, the Operand Data Mux, B and C Operand Registers, and the DAI Register. The 12CF-2 also contains a clock network (lower left symbol) which produces phased clocks for internal use, a control network for the B and C Operand Registers, and miscellaneous registers and mux functions. The miscellaneous registers and mux functions will be explained along with the major functions.

Clock Network

The clock network consists of a shift register which loads a single bit (input pin PH3) and shifts it down through 4-bit positions. Each transition to LO of the CLCK input activates the C and G modifiers and causes a right shift of 1-bit position. The C (clock) modifier clocks in the state of the PH3 input to the top bit position of the shift register. The G (gating) modifier gates the delayed outputs from the shift register to produce the tO, t1, t2, and t3 clocks. The shift right causes the previous contents of each bit position to shift down 1-bit position. The PH1 and PH2 clocks are not gated or delayed and therefore always follow the contents of their respective bit positions. The timing diagram on the following page shows the inputs to the clock network and its outputs.

RDSA Register (second symbol from the top on the left side)

When input pin HOLD is HI, new data will clock in to the RDSA Register each Tl time. When HOLD is LO, the clock modifier C cannot become active at Tl time and the register holds the data.

RDSB Register

When input pin HOLD is HI, new data will clock in to the RDSB Register each T2 time. When HOLD is LO, the clock modifier C cannot become active at T2 time and the register holds the data.

RDSC Register

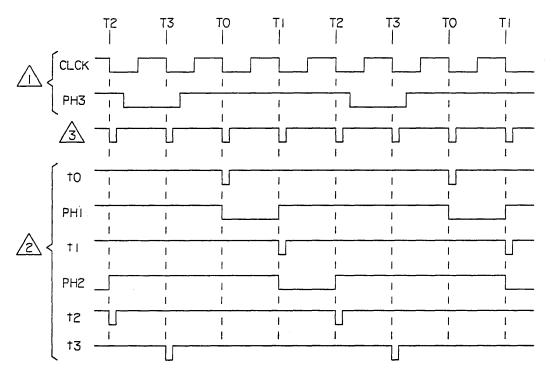
The RDSC Register has two highwayed inputs. The top highway is the normal data path and is clocked in at T3 time by a control translation of 5. Note that HOLD must be HI in order to clock in the normal data path. When HOLD is LO, the RDSC Register either holds it contents at T3 time (translation of 4) or clocks in the lower highway (translation of 6).

The lower highway is used for reloading the RDSC Register during a functional unit shortstop of the C Operand when Hold is LO. In this case a translation of 6 will clock in the lower highway which comes from the output of the DAI Register. A translation of 7 also clocks in the lower highway, but this translation is not used.

The B, C Operand Register Control paragraph explains the control for the selection of the lower data path to the RDSC Register.

Operand Data Mux (symbol in the upper right corner)
Two select signals control the selection of one of 4 input highways. These two select signals enter the array on pins DEMUXG (0) and (1) and are clocked into a register controlled by clock (t) from pin CLCK.

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NØTES: \(\hat{\Delta} \) INPUTS TØ THE CLØCK CKT IN THE CF ARRAY.

CLØCK CKT ØUTPUTS (INTERNAL TØ THE CF ARRAY).

ØUTPUT ØF THE ØN-CHIP CLØCK SHAPER. THE CLØCK SHAPER FØRMS A 2.5 NS PULSE ØN THE LEADING EDGE ØF THE ACTIVE LØ CLØCK INPUT (CLCK). THE ANSI SYMBØL USES THE DYNAMIC INDICATØR (>) TØ SHØW THIS CLØCK SHAPER.

12CF-2 (Cont'd)

A control translation of 0 selects data from input pins DSS(0-1).

A control translation of 1 selects the output from a 2-input mux. The mux selects RDSA or RDSB data under the control of PH1 and PH2 from the clock network. RDSA data goes through the mux during phase 1 (PH1) time and RDSB data goes through the mux during phase 2 (PH2) time.

A control translation of 2 selects data from input pins RF(0-1). This data passes through a gate which can allow it to pass (G1 active) or block it forcing zeros (G1 inactive). The control for this gate enters pin FZERO and is clocked into a register by clock (t) from pin CLCK. When the register is active, its output is HI, deactivating G1 in the gate and forcing zeros on the gate's output highways. When the register is inactive, its output is LO, activating G1 in the gate and allowing the highways to pass.

A control translation of 3 selects data from the output of the DAI Register. The DAI Register is on the input to the Register File and the Operand Data Mux is on the output of the Register File. Thus a control translation of 3 causes a Register File Shortstop. The data from the DAI Register also passes through the gate which can force zeros.

B Operand Register

Two select signals and tO clock select one of 4 input highways and clock the contents into the register. The select signals come from a DEMUX which is explained in the B, C Operand Register Control paragraph.

A control translation of 4 clocks in data from the RDSB Register. This is the normal path where the contents of the RDSB Register become B operand sent to the ALN.

Control translations of 5, 6, and 7 clock in data from the ALN, AC, and LM, respectively. These are functional unit shortstop paths because the data is being taken from the output paths of the functional units and sent to the input of the ALN.

C Operand Register

Two select signals and tO clock select one of 4 input highways and clock the contents into the register. The select signals come from a DEMUX which is explained in the B, C Operand Register Control paragraph.

A control translation of 4 clocks in data from the RDSC Register. This is the normal path where the contents of the RDSC Register become the C operand sent to the ALN or to Address Control.

Control translations of 5, 6, and 7 clock in data from the ALN, AC, and LM, respectively. These are functional unit shortstop paths because the data is being taken from the output paths of the functional units and sent to the input of the ALN or AC.

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12CF-2 (Cont'd)

B, C Operand Register Control (enclosed by dashed line)

The major functions of the B, C Operand Register Control are the B Operand Select Enable Register (top CD function), the C Operand Select Enable Flip-Flop (bottom CD function), the Reload Control Register (left CD function), and the DEMUX.

There are 4 modes of operation. For descriptive purposes these modes are called Normal, Functional Unit Shortstop, Hold, and Reload.

Normal

Normal operation implies that operands are flowing smoothly from the RDSB and RDSC Registers to the B and C Operand Register with no interruptions of flow (holds).

Inputs HOLD, GFU (functional unit shortstop), and RELOAD are all HI. Thus all three CD functions in the B, C Operand Register Control are inactive. This makes GO and Gl in the DEMUX inactive forcing the DAIG(0-1) controls to zeros for both the B and C Operand Registers. At TO time the B and C Operand Registers Control translators will both be 4, clocking in data from the RDSB and RDSC Registers, respectively.

Functional Unit Shortstop

During a functional unit shortstop operation, the B and/or C Operand Registers receive data from the output paths of the functional units. This data is tapped off at the input to the DAI Register. The DAIG(0-1) inputs select the shortstopped functional unit (ALN, AC, or LM) and the DEMUX routes this control to the proper operand register(s).

Inputs HOLD and RELOAD are HI and GFU (functional unit shortstop) is LO. When GFU is LO during the tl clock, the B Operand Select Enable Register (top CD function) is set (active). When GFU is LO during the t2 clock, the C Operand Select Enable Flip-Flop (lower CD function) is set. This activates GO and/or Gl in the DEMUX and gates the DAIG(0-1) control to the B and/or C Operand Registers which at TO time clock in the selected functional unit.

Ho1d

The HOLD input, when LO, interrupts the flow of data during normal or functional unit shortstop operations. This is due to the Address Control or Local Memory unit not being able to accept new operands. Thus the RDSA, RDSB, and RDSC Registers and the B, C Operand Register Control must hold until the functional unit can again accept operands.

When the HOLD input is LO, the C (clock) modifiers for RDSA, RDSB, RDSC, and B Operand Select Enable Register, and the C Operand Select Enable Flip-Flop are all inactive, causing these circuits to hold their contents. When the C Operand Select Enable Flip-Flop is set (functional unit shortstop of C) while HOLD is LO, a reload operation will take place. Refer to Reload.

Reload

A reload operation takes place when there is a functional unit shortstop of C (C Operand Select Enable Flip-Flop set) and the HOLD input becomes LO. The reload operation will reset the C Operand Select Enable Flip-Flop and clock DAI Register output data into the RDSC Register.

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12CF-2 (Cont'd)

When the RELOAD input goes LO, the AND gate it enters will become active because the C Operand Select Enable Flip-Flop is set. The active AND gate deactivates the data input to the C Operand Select Enable Flip-Flop and also allows the t clock (pin CLCK) to set the Reload Control Register. The Reload Control Register then performs two functions. First, it enables the clock circuits for the C Operand Select Enable Flip-Flop so at T2 time it will reset. Thus GO in the DEMUX will become inactive and force zeros to the C Operand Register control selecting the data path from the RDSC Register. Second, at T3 time the RDSC Register control translator will decode a 6 which will clock in data from the output of the DAI Register. Since the C Operand Select Enable Flip-Flop resets at T2 time, the AND gate which RELOAD entered becomes inactive. This allows the Reload Control Register to clear the next time clock goes LO.

DAI Register

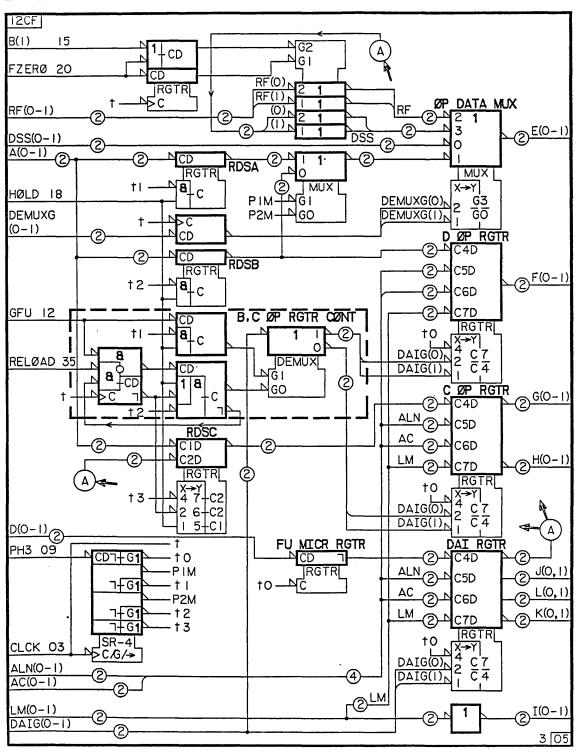
Two select signals and the t0 clock, select one of 4 input highways and clock the contents into the register.

A control translation of 4 clocks in the output of the Functional Unit Micrand Register. This register clocked in data from pins D(0-1) at the previous TO time.

Control translations of 5, 6, and 7 clock in data from the ALN, AC, and LM, respectively.

Data which enters on pins LM(0-1) also passes unaltered to output pins I(0-1).

60458120 B



BIAS LØ = NØNE

BIAS HI = MØDE, B(O)

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OPERATIONAL DESCRIPTION

The 12CF-3 performs major register and mux functions in the Operand Issue area. These functions are the RDSA, RDSB, and RDSC registers, the Operand Data Mux, B and C Operand Registers, and the DAI Register. The 12CF-3 also contains a clock network (lower left symbol) which produces phased clocks for internal use, a control network for the B and C Operand Registers, and miscellaneous registers and mux functions. The miscellaneous registers and mux functions will be explained along with the major functions.

Clock Network

The clock network consists of a shift register which loads a single bit (input pin PH3) and shifts it down through 4-bit positions. Each transition to LO of the CLCK input activates the C and G modifiers and causes a right shift of 1-bit position. The C (clock) modifier clocks in the state of the PH3 input to the top bit position of the shift register. The G (gating) modifier gates the delayed outputs from the shift register to produce the tO, t1, t2, and t3 clocks. The shift right causes the previous contents of each bit position to shift down 1-bit position. The PH1 and PH2 clocks are not gated or delayed and therefore always follow the contents of their respective bit positions. The timing diagram on the following page shows the inputs to the clock network and its outputs.

RDSA Register (second symbol from the top on the left side)

When input pin HOLD is HI, new data will clock in to the RDSB Register each T2 time. When HOLD is LO, the clock modifier C cannot become active at T2 time and the register holds the data.

RDSB Register

When input pin HOLD is HI, new data will clock into the RDSB Register each T2 time. When HOLD is LO, the clock modifier C cannot become active at T2 time and the register holds the data.

RDSC Register

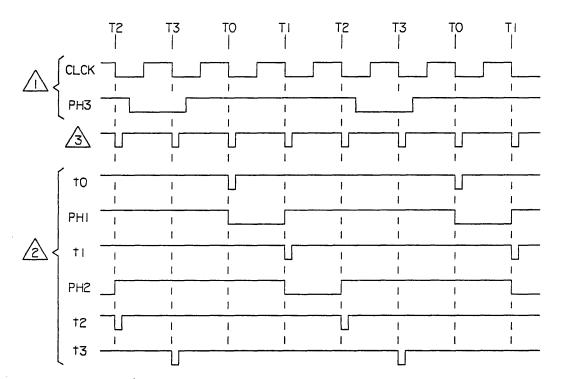
The RDSC Register has two highwayed inputs. The top highway is the normal data path and is clocked in at T3 time by a control translation of 5. Note that HOLD must be HI in order to clock in the normal data path. When HOLD is LO, the RDSC Register either holds it contents at T3 time (translation of 4) or clocks in the lower highway (translation of 6).

The lower highway is used for reloading the RDSC Register during a functional unit shortstop of the C Operand when Hold is LO. In this case a translation of 6 will clock in the lower highway which comes from the output of the DAI Register. A translation of 7 also clocks in the lower highway, but this translation is not used.

The B, C, Operand Register Control paragraph explains the control for the selection of the lower data path to the RDSC Register.

Operand Data Mux (symbol in the upper right corner)
Two select signals control the selection of one of 4 input highways. These two select signals enter the array on pins DEMUXG (0) and (1) and are clocked into a register controlled by clock (t) from pin CLCK.

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NØTES: / INPUTS TØ THE CLØCK CKT IN THE CF ARRAY.

CLØCK CKT ØUTPUTS (INTERNAL TØ THE CF ARRAY).

ØUTPUT ØF THE ØN-CHIP CLØCK SHAPER. THE CLØCK SHAPER FØRMS A 2.5 NS PULSE ØN THE LEADING EDGE ØF THE ACTIVE LØ CLØCK INPUT (CLCK). THE ANSI SYMBØL USES THE DYNAMIC INDICATØR (>) TØ SHØW THIS CLØCK SHAPER.

12CF-3 (Cont'd)

A control translation of 0 selects data from input pins DSS(0-1).

A control translation of 1 selects the output from a 2-input mux. The mux selects RDSA or RDSB data under the control of PH1 and PH2 from the clock network. RDSA data goes through the mux during phase 1 (PH1) time and RDSB data goes through the mux during phase 2 (PH2) time.

A control translation of 2 selects data from input pins RF(0-1). This data passes through a gate which can allow each bit to pass (Gl and G2 active) or block either or both bits forcing zeros (Gl and/or G2 inactive). The control for this gate enters pins FZERO and B(1) and is clocked into registers by clock from pin CLCK. The register which controls Gl in the gate requires FZERO LO at T time in order to become active. The register which controls G2 in the gate requires either B(1) or FZERO LO to become active. When either register is active, its output is HI, thereby deactivating Gl or G2 in the gate and forcing a zero(s) on the output of the gate. When either register is inactive, its output is LO, thereby activating Gl or G2 in the gate and allowing the bit(s) to pass.

A control translation of 3 selects data from the output of the DAI Register. The DAI Register is on the input to the Register File and the Operand Data Mux is on the output of the Register File. Thus a control translation of 3 causes a Register File Shortstop. The data from the DAI Register also passes through the gate which can force zeros.

B Operand Register

Two select signals and tO clock select one of 4 input highways and clock the contents into the register. The select signals come from a DEMUX which is explained in the B, C Operand Register Control paragraph.

A control translation of 4 clocks in data from the RDSB Register. This is the normal path where the contents of the RDSB Register become the B Operand sent to the ALN.

Control translations of 5, 6, and 7 clock in data from the ALN, AC, and LM, respectively. These are functional unit shortstop paths because the data is being taken from the output paths of the functional units and sent to the input of the ALN.

C Operand Register

Two select signals and TO clock select one of 4 input highways and clock the contents into the register. The select signals come from a DEMUX which is explained in the B, C, Operand Register Control paragraph.

A control translation of 4 clocks in data from the RDSC Register. This is the normal path where the contents of the RDSC Register become the C operand sent to the ALN or to Address Control.

Control translations of 5, 6, and 7 clock in data from the ALN, AC, and LM, respectively. These are functional unit shortstop paths because the data is being taken from the output paths of the functional units and sent to the input of the ALN or AC.

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B, C Operand Register Control (enclosed by dashed line)

The major functions of the B, C Operand Register Control are the B Operand Select Enable Register (top CD function), the C Operand Select Enable flip-flop (bottom CD function), the Reload Control Register (left CD function), and the DEMUX.

There are 4 modes of operation. For descriptive purposes these modes are called Normal, Functional Unit Shortstop, Hold, and Reload.

Normal

Normal operation implies that operands are flowing smoothly from the RDSB and RDSC Registers to the B and C Operand Register with no interruptions of flow (holds).

Inputs HOLD, GFU (functional unit shortstop), and RELOAD are all HI. Thus all three CD functions in the B, C Operand Register Control are inactive. This makes GO and Gl in the DEMUX inactive forcing the DAIG(0-1) controls to zeros for both the B and C Operand Registers. At TO time the B and C Operand Registers Control translators will both be 4, clocking in data from the RDSB and RDSC Register, respectively.

Functional Unit Shortstop

During a functional unit shortstop operation, the B and/or C Operand Registers receive data from the output paths of the functional units. This data is topped off at the input to the DAI Register. The DAIG(0-1) inputs select the shortstopped functional unit (ALN, AC, or LM) and the DEMUX routes this control to the proper operand register(s).

Inputs HOLD and RELOAD are HI and GFU (functional unit shortstop) is LO. When GFU is LO during the tl clock, the B Operand Select Enable Register (top CD function) is set (active). When GFU is LO during the t2 clock, the C Operand Select Enable Flip-Flop (lower CD function) is set. This activates GO and/or Gl in the DEMUX and gates the DAIG(0-1) control to the B and/or C Operand Registers which at TO time clock in the selected functional unit.

Hold

The HOLD input, when LO, interrupts the flow of data during normal or functional unit shortstop operations. This is due to the Address Control or Local Memory unit not being able to accept new operands. Thus the RDSA, RDSB, and RDSC Registers and the B, C Operand Register Control must hold until the functional unit can again accept operands.

When the HOLD input is LO, the C (clock) modifiers for RDSA, RDSB, RDSC, and B Operand Select Enable Register, and the C Operand Select Enable Flip-Flop are all inactive, causing these circuits to hold their contents. When the C Operand Select Enable Flip-Flop is set (functional unit shortstop of C) while HOLD is LO, a reload operation will take place. Refer to Reload.

Reload

A reload operation takes place when there is a functional unit shortstop of C (C Operand Select Enable Flip-Flop set) and the HOLD input becomes LO. The reload operation will reset the C Operand Select Enable Flip-Flop and clock DAI Register output data into the RDSC Register.

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12CF-3 (Cont'd)

When the RELOAD input goes LO, the AND gate it enters will become active because the C Operand Select Enable Flip-Flop is set. The active AND gate deactivates the data input to the C Operand Select Enable Flip-Flop and also allows the t clock (pin CLCK) to set the Reload Control Register. The Reload Control Register then performs two functions. First, it enables the clock circuits for the C Operand Select Enable Flip-Flop so at T2 time it will reset. Thus GO in the DEMUX will become inactive and force zeros to the C Operand Register control selecting the data path from the RDSC Register. Second, at T3 time the RDSC Register control translator will decode a 6 which will clock in data from the output of the DAI Register. Since the C Operand Select Enable Flip-Flop resets at T2 time, the AND gate which RELOAD entered becomes inactive. This allows the Reload Control Register to clear the next time clock goes LO.

DAI Register

Two select signals and the t0 clock, select one of 4 input highways and clock the contents into the register.

A control translation of 4 clocks in the output of the Functional Unit Micrand Register. This register clocked in data from pins D(0-1) at the previous T0 time.

Control translations of 5, 6, and 7 clock in data from the ALN, AC, and LM, respectively.

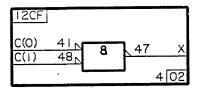
Data which enters on pins LM(0-1) also passes unaltered to output pins I(0-1).

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12CF-4 AND Gate.

LOGIC SYMBOL



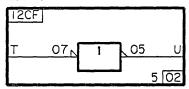
BIAS = THIS CKT CANNOT BE USED WITH THE CF ARRAY BIASED TO TYPE O. IT IS COMPATIBLE WITH TYPES 1, 2, AND 3. OUTPUT PIN X IS CAPABLE OF DRIVING 8 LOADS.

OPERATIONAL DESCRIPTION

(None required.)

12CF-5 Fanout.

LOGIC SYMBOL



BIAS = THIS CKT IS SEPARATE FROM ALL ØTHER FUNCTIONS OF THE CF ARRAY. IT IS THEREFORE NOT AFFECTED BY ANY BIAS.

OUTPUT PIN U IS CAPABLE OF DRIVING 8 LOADS.

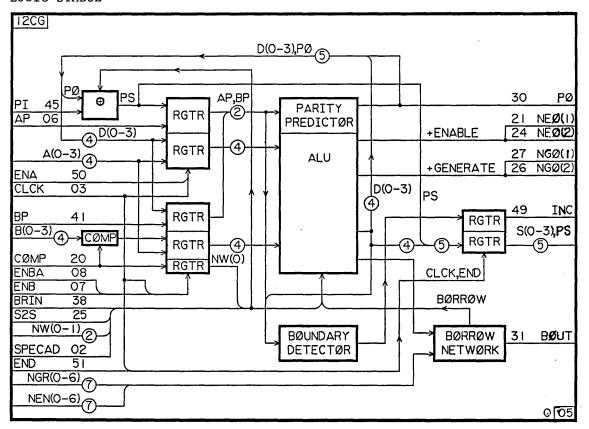
OPERATIONAL DESCRIPTION

(None required.)

12CG

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	29	V06
A(1)	28	V08
A(2)	23	V10
A(3)	11	V12
AP	06	V04
B(0)	42	V05
B(1)	36	V07
B(2)	19	V09
B(3)	10	V11
BP	41	V01
BRIN	38	V03
CLCK	03	V35
COMP	20	V13
ENA	50	V36
ENB	07	V37
ENBA	08	V39
END	51	V38
NEN(0)	33	V23
NEN(1)	34	V24
NEN(2)	46	V25
NEN(3)	44	V26
NEN(4)	17	V27
NEN(5)	15	V28
NEN(6)	12	V21
NGR(0)	32	V14
NGR(1)	35	V15
NGR(2)	48	V16
NGR(3)	43	V17
NGR(4)	22	V18
NGR(5)	18	V19
NGR(6)	16	V20
NW(0)	37	V22
NW(1)	09	V30
PI	45	V02
SPECAD	02	V40
S2S	25	V29
BOUT	31	V48
INC	49	V41
NEO(1)	21	V33
NEO(2)	24	V34
NGO(1)	27	V31
NGO(2)	26	V32
PO	30	V42
PS	47	V43
S(0)	52	V44
S(1)	01	V45
S(2)	04	V46
S(3)	05	V47

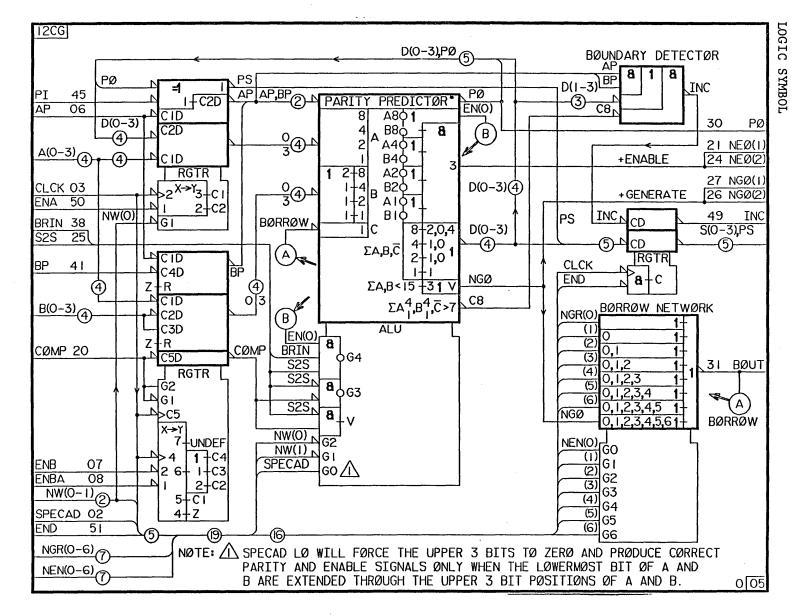
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BIAS = NØNE

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagrams. Refer to the ANSI symbol and its description.



BIAS = NØNE

OPERATIONAL DESCRIPTION

The 12CG-O consists of seven major functional elements: the A Operand Register (upper left), B Operand Register (lower left), Parity Predictor (in the top of the ALU symbol), ALU, Boundary Detector, Output Register (right center), and the Borrow Network.

A Operand Register

Input pins ENA and CLCK control the selection and clocking of data and parity into the A Operand Register.

A control translation of 3 clocks in data from pins A(0-3) and parity from pin AP.

A control translation of 2 clocks in data from the output of the ALU and also clocks in the exclusive OR of the output parity bit PO and input pin PI. Pin PI is the parity bit for the other 4-bit slice of an 8-bit group.

Input pin NW(0) LO gates the output of the exclusive OR.

B Operand Register

Input pins ENB, ENBA, CLCK, and COMP control the selection and clocking of data into the B Operand Register.

A control translation of 4 clears the parity bit portion of the register (top) and the data portion of the register (center).

A control translation of 5 clocks in data from pins A(0-3) and parity from pin AP.

A control translation of 6 clocks in the B input highway parity bit from pin BP. A control translation of 6 with additional control from input pin COMP also controls the selection and clocking of data from the B input highway. Input pin COMP will select inverted (active HI) B input data for subtract operations and select (active LO) B input data for add operations. COMP is LO for subtract operations and HI for add operations.

A control translation of 7 causes undefined results.

Clock entering pin CLCK also clocks the COMP input into a register.

Parity Predictor

The asterisk in the Parity Predictor symbol indicates that the symbol is incomplete. Therefore the following Parity Predictor information cannot be deduced from the symbol.

The Parity Predictor receives the parity bits from the two input operands and internal inputs from ALU to determine what the parity of the result will be. The Parity Predictor does not generate parity; it adjusts it. Bad parity (odd) on one of the two input operands will result in odd parity on the output of the Parity Predictor.

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When the SPECAD input is LO, the Parity Predictor will properly adjust parity only when the least-significant bit of the A and B operands are extended up through the upper 3-bit positions of their respective operands.

Arithmetic and Logical Unit (ALU)

The ALU is a variable width adder. It can add all 4 bits of the A operand to all 4 bits of the B operand, or it can add only the least-significant 3 bits of each, or the most-significant bit of each, or the least-significant bit of each, or none of each. The Variable Width Control paragraph describes the variable width controls.

A Operand Inputs

The 4-bit A operand comes from the A Operand Register. It enters the ALU where it is weighted binarily 1 through 8 and designated as the A operand.

B Operand Inputs

The 4-bit B operand comes from the B Operand Register. It enters the ALU and passes through an OR function where gating modifier Gl gates the least-significant 3-bits and G2 gates the most-significant bit. The 4-bits are then weighted binarily 1 through 8 and designated as the B operand. Control of the gating modifiers is dealt with in the Variable Width Control paragraph.

Borrow Input

The BORROW input comes from the Borrow Network. It enters the ALU, is given a binary weight of 1, and designated as operand C.

EN(0) Output

The EN(0) output is the most-significant bit-enable. It will be HI when either or both of the most-significant bits of the A and B operands are inactive.

NEO(1,2) Outputs

Pins NEO(1) and NEO(2) are copies of the same group enable signal. This signal will be HI when all bit enables are active. A bit enable is active when either or both of the A and B operand bits in that position are inactive. Gating modifier G3 gates the group enable out of the ALU. G3 is described in the Generate Output paragraph.

D(0-3) Outputs

The D(0-3) outputs are the summation of A, B, and the complement of C. This summation is weighted binarily 1 through 8 and passed through an OR function where gating modifiers control each bit. G2, G0, and G4 must all be active to gate the most-significant bit (weighted 8). G1 and G0 must both be active to gate the bits weighted 2 and 4. G1 also gates the least-significant bit. The Variable Width paragraph describes the G0-2 gating modifiers and the G4 control paragraph describes G4.

Generate Output

Pins NGO(1) and NGO(2) are copies of the same generate signal. This signal will be HI when the summation of A and B are less than 15 AND G3 is active. The generate signal will also be active when V is active. V is active when the COMP signal is HI and input pin S2S is LO.

The lower two AND gates in the common control block control G3 and V. In actual use, input pin S2S is used dynamically only on the array which processes the most-significant 4-bits in the adder. It indicates two's complement when LO and one's complement when HI. Input S2S is biased HI on all lower arrays. Thus on the array which processes the most-significant 4-bits, V active will force a generate when there is a two's complement add (COMP HI) or block the generate (G3 inactive) for a two's complement subtract (COMP LO). G3 inactive also blocks the group enable. Refer to the NEO(1,2) Output paragraph.

C8 Output

The C8 output will be active (LO) when the summation of the 3 least-significant bits of A and B and the complement of C are greater than 7. C8 is used in the Boundary Detector.

Variable Width Control

For the explanation of the variable width control, assume that G4 in the common control block is active. G4 is used only in the output of the most-significant result bit of each 4-bit group in the adder. The G4 control paragraph explains its use.

The NW(0-1) and SPECAD inputs control the width of the ALU.

When NW(0-1) and SPECAD are all LO, GO-2 are all active. This gates in the entire B operand and gates out the entire sum to D(0-3). Thus the ALU operated on the full width (all 4-bits) of its 4-bit group of the adder.

When NW(0) is HI, G2 is inactive. This blocks the most-significant bit of the B operand and the most-significant bit of the result. The reason for blocking the B operand bit is to force an enable in that bit position. Note that the enable output looks for zeros in either operand for each bit position. Thus with NW(0) HI, the upper result bit was forced to zero and its bit position enabled.

When NW(1) is HI, G1 is inactive. This blocks the lower 3-bits of the B operand and the lower 3-bits of the result. The reason for blocking the B operand bits is to force enables in these bit positions. Note that the enable output looks for zeros in either operand for each bit position. Thus with NW(1) HI, the lower three result bits are forced to zero and their bit positions enabled.

NW(0) and (1) may work separately or together. With both HI, the entire ALU result would be forced to zero and the group enable would be active (HI).

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When input SPECAD is LO, it forces zeros in the upper 3-bits of the ALU result. When SPECAD is LO, the least-significant bits of A and B must be extended (externally) through the upper 3-bit positions of A and B. This extension allows the enables and parity to operate properly.

G4 Control

The 12CG array uses an add algorithm which cannot be deduced from the symbol. Each bit of the result is translated by using not only the borrow into its bit position but also the borrow into the next more-significant bit position. This larger add algorithm maximizes the number of single component failures (inside the array) which causes a parity error in the result.

This algorithm is entirely internal for the lower 3-bits in each array and need not be shown on the symbol. The most-significant bit of each array however must receive the borrow into the next higher bit position. This borrow enters input pin BRIN and comes from the BOUT output from the next more significant array in the adder. The most-significant array receives the borrow from the least-significant array.

Input pin S2S is used dynamically only on the most-significant array in the adder. It indicates two's complement when LO and one's complement when HI. Input S2S is biased HI on all arrays of lower significance in the adder.

When EN(0), BRIN, and S2S are all HI, G4 becomes inactive and blocks the most-significant bit.

Boundary Detector

The Boundary Detector output equals C8 • $(D(1)+D(2)+D(3)+(\overline{AP} \bullet \overline{BP}))$.

Output Register

Input pin END is ANDed with clock from input pin CLCK and clocks in the 4-bit result from D(0-3), its parity bit PS, and the result of the Boundary Detector.

Borrow Network

The Borrow Network receives active HI generates (input pins NGR(0-6)) and active HI enables (NEN(0-6)) from each array in the adder and determines the borrow. The Borrow Network output goes to the ALU and to output pin BOUT where it is sent to the next lower array (refer to G4 control).

Each NGR input enters an OR function which is controlled by gating modifiers. These gating modifiers are controlled by the NEN inputs.

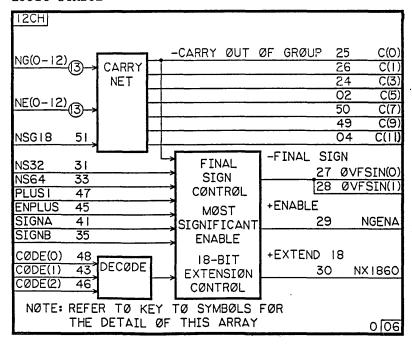
BOUT will be active (LO) when NGR(0) is active OR NGR(1) AND NEN(0) are active, OR NGR(2) AND NEN(0-1) are active, etc.

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12CH

PIN	REAL	VIRT
NAME	PIN	PIN
CHSEL	37	V06
CODE(0)		V01
CODE(1)	43 46	V02 V03
ENPLUS	45	V05
NE(0)	18	V12
NE(1)	17	V15
NE(2)	20	V16
NE(3) NE(4)	21 23	V19 V20
NE(5)	16	V23
NE(6)	11	V24
NE(7)	12	V27
NE(8) NE(9)	42 08	V28 V31
NE(9)	03	V31
NE(11)	06	V35
NE(12)	01	V36
NG(0) NG(1)	15 19	V11 V13
NG(1)	34	V13
NG(2)	22	V17
NG(4)	32	V18
NG(5)	38	V21
NG(6) NG(7)	36 10	V22 V25
NG(7)	52	V25
NG(9)	09	V29
NG(10)	44	V30
NG(11)	07	V33
NG(12) NSGN18	05 51	V34 V40
NS32	31	V10
NS64	33	V09
PLUS1	47	V04
SIGNA	41	V07
SIGNB	35	V08
C(0) C(1)	25 26	V41 V42
C(3)	24	V43
C(5)	02	V44
C(7)	50 40	V45
C(9) C(11)	49 04	V46 V47
NGENA	29	V38
NX1860	30	V39
OVFSIN(0) 27 1) 28	V48 V37
1 2 4 1 2114/	., 20	43/

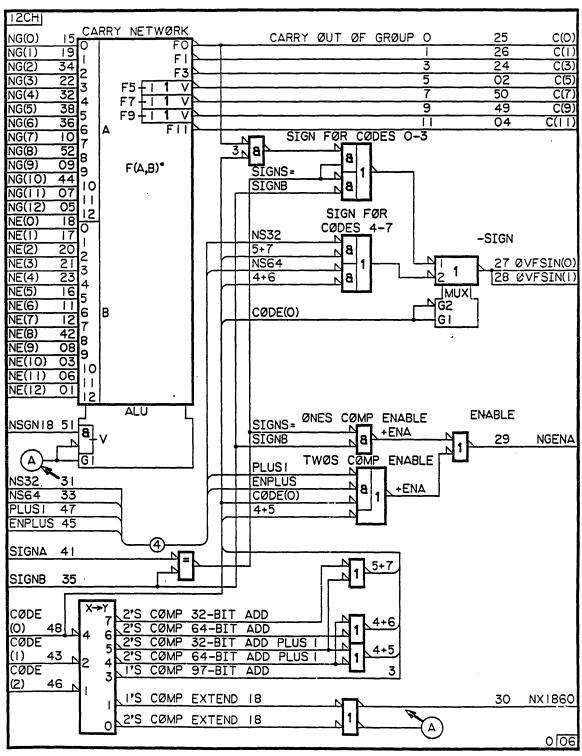
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BIAS LØ = CHSEL BIAS HI = NØNE

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagrams. Refer to the ANSI symbol and its description.



BIAS LØ = CHSEL BIAS HI = NØNE

OPERATIONAL DESCRIPTION

The 12CH-0 symbol contains several functions: a carry network, a code translator (lower portion of symbol), AND/OR logic which determines sign and enable, and an output mux which selects the sign.

Carry Network

The Carry Network function is performed by an ALU whose outputs are a function of the A and B groups of inputs. The asterisk (*) following the qualifying symbol (F(A,B)*) indicates that the symbol is incomplete. Therefore, the following Carry Network information cannot be deduced from the symbol.

Active HI generates enter the array on pins NG(0-12), are weighted decimally 0-12, and designated as group A. Active HI enables enter the array on pins NE(0-12), are weighted decimally 0-12, and designated as group B.

The carry network has 7 outputs designated as F0, 1, 3, 5, 7, 9, and 11. Each output is a function of the A and B groups of inputs (refer to the Carry Network Output Equations paragraph).

Outputs F5, 7 and 9 are further controlled by gating modifier G1 and OR modifier V. G1 gates the F5, 7 and 9 outputs to output pins C(5), C(7), and C(9), respectively. G1 is active when there are code translations of 2 through 7 (not 0 or 1). V forces the F5, 7, and 9 outputs active (LO). V is active when input NSGN18 is HI AND there are code translations of 0 or 1.

Code Translation

A 3-bit code enters the array on pins CODE(0-2) and is translated. Translations of 0 and 1 are 0Red and control the carry network and output NX1860. Translations of 3-7 control the sign and enable functions.

Sign Select Mux

CODE(0) selects between the outputs of two sign networks. CODE(0) is HI for codes 0-3 and LO for codes 4-7.

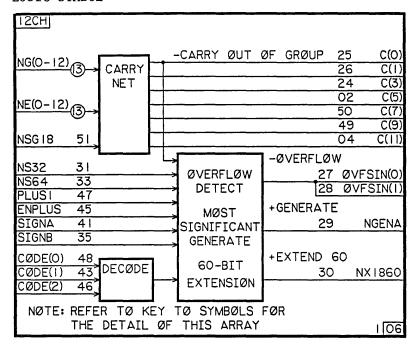
60458120 B

Carry Network Output Equations

The following equations assume active HI Carry Network inputs and produce active LO results.

```
+ A1 • B0
FFO=AO
                            F1=A1 + A2 \bullet B1
                                                      F3=A3 + A4 \bullet B3
        + A2 • BO • B1
                                  + A3 • B1 • B2
                                                             + A5 • B3 • B4
        + A3 • B0-2
                                  + A4 \bullet B1-3
                                                             + A6 • B3-5
        + A4 \bullet B0-3
                                 + A5 • B1-4
                                                             + A7 \bullet B3-6
        + A5 • B0-4
                                 + A6 • B1-5
                                                            + A8 • B3-7
        + A6 • B0-5
                                 + A7 • B1-6
                                                            + A9 • B3-8
        + A7 • B0-6
                                 + A8 • B1−7
                                                            + A10 • B3-9
        + A8 ● B0-7
                                 + A9 • B1-8
                                                            + A11 • B3-10
        + A9 • B0-8
                                 + A10 • B1-9
                                                            + A12 • B3-11
        + A10 • B0-9
                                 + All • Bl-10
                                                            + A0 • B3-12
        + A11 • B0-10
                                 + A12 • B1-11
                                                            + A1 • B3-12 • B0
        + A12 • B0-11
                                 + A0 • B1-12
                                                             + A2 • B3-12 • B0 • B1
FF5=A5 + A6 ● B5
                            F7=A7 + A8 \bullet B7
                                                      F9=A9 + A10 \bullet B9
        + A7 • B5 • B6
                                  + A9 • B7 • B8
                                                             + A11 • B9 • B10
        + A8 • B5-7
                                  + A10 • B7-9
                                                             + A12 • B9-11
        + A9 • B5-8
                                  + All • B7-10
                                                             + A0 • B9-12
        + A10 • B5-9
                                  + A12 • B7-11
                                                            + A1 • B9-12 • B0
        + A11 • B5-10
                                  + A0 • B7-12
                                                            + A2 • B9-12 • B0 • B1
        + A12 • B5-11
                                 + A1 • B7-12 • B0
                                                            + A3 • B9-12 • B0-2
        + A0 • B5-12
                                 + A2 • B7-12 • B0 • B1
                                                            + A4 • B9-12 • B0-3
        + A1 • B5-12 • B0
                                 + A3 • B7-12 • B0-2
                                                            + A5 • B9-12 • B0-4
        + A2 • B5-12 • B0 • B1 + A4 • B7-12 • B0-3
                                                            + A6 • B9-12 • B0-5
        + A3 • B5-12 • B0-2
                                 + A5 • B7-12 • B0-4
                                                            + A7 • B9−12 • B0−6
        + A4 • B5-12 • B0-3
                                  + A6 • B7−12 • B0−5
                                                            + A8 • B9-12 • B0-7
F11=A11 + A12 • B11
        + AO • B11 • B12
        + A1 • B11 • B12 • B0
        + A2 • B11 • B12 • B0 • B1
        + A3 • B11 • B12 • B0-2
        + A4 • B11 • B12 • B0-3
        + A5 • B11 • B12 • B0-4
        + A6 • B11 • B12 • B0-5
        + A7 • B11 • B12 • B0-6
        + A8 • B11 • B12 • B0-7
        + A9 • B11 • B12 • B0-8
        + A10 • B11 • B12 • B0-9
```

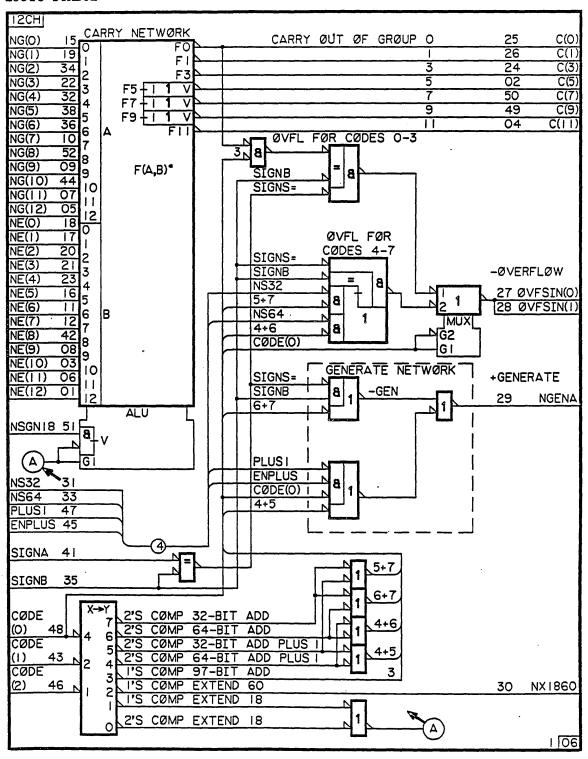
60458120 B



BIAS LØ = NØNE BIAS HI = CHSEL

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagrams. Refer to the ANSI symbol and its description.



BIAS LØ = NØNE

BIAS HI = CHSEL

12CH-1 (Cont'd)

OPERATIONAL DESCRIPTION

The 12CH-1 symbol contains several functions: a carry network, a code translator (lower portion of symbol), logic which determines overflow and generate, and an output mux which selects the overflow.

Carry Network

The Carry Network function is performed by an ALU whose outputs are a function of the A and B groups of inputs. The asterisk (*) following the qualifying symbol (F(A,B)*) indicates that the symbol is incomplete. Therefore, the following Carry Network information cannot be deduced from the symbol.

Active HI generates enter the array on pins NG(0-12), are weighted decimally 0-12, and designated as group A. Active HI enables enter the array on pins NE(0-12), are weighted decimally 0-12, and designated as group B.

The carry network has 7 outputs designated as F0, 1, 3, 5, 7, 9, and 11. Each output is a function of the A and B groups of inputs (refer to the Carry Network Output Equations paragraph).

Outputs F5, 7 and 9 are further controlled by gating modifier G1 and OR modifier V. G1 gates the F5, 7 and 9 outputs to output pins C(5), C(7), and C(9), respectively. G1 is active when there are code translations of 2 through 7 (not 0 or 1). V forces the F5, 7, and 9 outputs active (L0). V is active when input NSGN18 is HI AND there are code translations of 0 or 1.

Code Translation

A 3-bit code enters the array on pins CODE(0-2) and is translated. Translations of 0 and 1 are ORed and control the Carry Network. A translation of 2 controls output pin NX1860 and translations of 3-7 control the overflow and generate functions.

Overflow For Codes 0-3

The equation for the output of the OVFL FOR CODES 0-3 network is:

((CARRY OUT OF GROUP 0 • code translation of 3)=SIGNB) • SIGNS EQUAL

Overflow for Codes 4-7

The equation for the output of the OVFL FOR CODES 4-7 network is:

SIGNS EQUAL • (SIGNB=(NS32 • Codes 5 or 7) + (NS64 • codes 4 or 6))

Overflow Select Mux

CODE(0) selects between the outputs of two overflow networks. CODE(0) is HI for codes 0-3 and LO for codes 4-7.

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12CH-1 (Cont'd)

Carry Network Output Equations

The following equations assume active HI Carry Network inputs and produce active LO results.

```
F3=A3 + A4 \bullet B3
F0=A0
        + A1 ● B0
                            F1=A1 + A2 \bullet B1
        + A2 • B0 • B1
                                  + A3 • B1 • B2
                                                              + A5 • B3 • B4
        + A3 \bullet B0-2
                                  + A4 • B1-3
                                                              + A6 • B3-5
                                + A5 \bullet B1-4
        + A4 \bullet B0-3
                                                             + A7 • B3-6
        + A5 • B0-4
                                  + A6 \bullet B1-5
                                                             + A8 \bullet B3-7
        + A6 • B0-5
                                  + A7 • B1-6
                                                             + A9 • B3-8
        + A7 • B0-6
                                  + A8 • B1 -7
                                                             + A10 • B3-9
        + A8 • B0-7
                                  + A9 • B1-8
                                                             + A11 • B3-10
        + A9 • B0-8
                                  + A10 • B1-9
                                                             + A12 • B3-11
                                  + All • Bl-10
        + A10 \bullet B0-9
                                                             + A0 • B3−12
        + A11 • B0-10
                                  + A12 \bullet B1-11
                                                            + A1 • B3−12 • B0
        + A12 • B0-11
                                  + A0 • B1-12
                                                             + A2 • B3-12 • B0 • B1
F5=A5
        + A6 • B5
                            F7=A7 + A8 \bullet B7
                                                       F9=A9 + A10 - B9
        + A7 • B5 • B6
                                  + A9 • B7 • B8
                                                              + A11 • B9 • B10
        + A8 • B5-7
                                  + A10 • B7-9
                                                              + A12 • B9-11
        + A9 • B5-8
                                  + A11 • B7-10
                                                              + A0 • B9-12
        + A10 • B5-9
                                  + A12 • B7-11
                                                             + A1 ● B9-12 ● B0
        + A11 • B5-10
                                  + A0 • B7-12
                                                             + A2 • B9-12 • B0 • B1
        + A12 • B5-11
                                  + A1 • B7-12 • B0
                                                             + A3 • B9-12 • B0-2
        + A0 • B5-12
                                  + A2 • B7-12 • B0 • B1
                                                             + A4 • B9-12 • B0-3
        + A1 • B5−12 • B0
                                  + A3 • B7-12 • B0-2
                                                             + A5 • B9-12 • B0-4
        + A2 • B5−12 • B0 • B1
                                  + A4 • B7-12 • B0-3
                                                             + A6 • B9-12 • B0-5
        + A3 ◆ B5-12 ◆ B0-2
                                  + A5 • B7-12 • B0-4
                                                             + A7 • B9-12 • B0-6
        + A4 • B5-12 • B0-3
                                  + A6 • B7-12 • B0-5
                                                             + A8 • B9-12 • B0-7
F11=A11 + A12 • B11
        + A0 • B11 • B12
        + A1 • B11 • B12 • B0
        + A2 • B11 • B12 • B0 • B1
        + A3 • B11 • B12 • B0-2
        + A4 • B11 • B12 • B0-3
        + A5 • B11 • B12 • B0-4
        + A6 • B11 • B12 • B0-5
        + A7 • B11 • B12 • B0-6
        + A8 • B11 • B12 • B0-7
        + A9 • B11 • B12 • B0-8
        + A10 • B11 • B12 • B0-9
```

12CH-2 Carry Network (Block Diagram).

LOGIC SYMBOL

12CH							
NG(0-12)	CARRY	CARRY	ØUT	ØF	GRØUP		C(O)
NE(0-12)	NET-					26	C(1)
(3)	WØRK					24	C(3)
						02	C(5)
						50	C(7)
						49	C(9)
i l						04	C(II)
		<u>.</u>				ć	2 05

BIAS LØ = CØDE(1-2), CHSEL, SIGNB BIAS HI = NSGN18, NS32, NS64, PLUS1, ENPLUS, CØDE(O), SIGNA

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagrams. Refer to the ANSI symbol and its description.

12CHI					
12CH					
I	CA	RRY	NETWØRK		
NG(O)	15			. 25	C(O)
NG(1)	15 O	Į.	FO	25 26	C(0)
NG(2)	34	ł	FI	20	
NG(3)	34 2 3 32 4 38 5 36 6	Į		24	C(3)
NG(4)	- 동등 3	Ì	F3	02	C(E)
NG(5)	35 4	1	F5	50	C(5) C(7) C(9)
NG(6)	- 38 5	١.	F7	30	C(1)
NO(6)	- 38 6	Α	F9	49	C(S)
NG(7)	22 3 32 4 38 5 36 6 10 7	1	FII	V4-	C(I I)
NG(8)	52 8 09 9 44 10 07 11 05 12 18 0				
NG(9)	9 9	l	F(A,B)*		
NG(10)	44 07 10	1			
NG(11)	97	l			ı
NG(12)	05 12	1			
NE(O)	180	i			
NE(1)	17				1
NE(2)	20 21 23 4 16 5				
NE(3)	2113	ļ	İ		- 1
NE(4)	23 4				- 1
NE(5)	165	l	,		
NE(6)	1116	В			
NE(7)	21 3 23 4 16 5 11 6 12 7 42 8 08 9 03 10	٦			i
NE(8)	42 6	1	1		1
NE(9)	08 08 9				
NE(10)	03 10	1			1
NE(11)	<u>oe</u> 1	1			
NE(12)	01 12				
	12			!	
					2 05

BIAS LØ = CØDE(1-2), CHSEL, SIGNB

BIAS HI = NSGN18, NS32, NS64, PLUSI, ENPLUS, CØDE(O), SIGNA

OPERATIONAL DESCRIPTION

The Carry Network function is performed by an ALU whose outputs are a function of the A and B groups of inputs. The asterisk (*) following the qualifying symbol (F(A,B)*) indicates that the symbol is incomplete. Therefore, the following Carry Network information cannot be deduced from the symbol.

Active HI generates enter the array on pins NG(0-12), are weighted decimally 0-12, and designated as group A. Active HI enables enter the array on pins NE(0-12), are weighted decimally 0-12, and designated as group B.

The carry network has 7 outputs designated as F0, 1, 3, 5, 7, 9, and 11. Each output is a function of the A and B groups of inputs (refer to the Carry Network Output Equations paragraph).

12CH-2 (Cont'd)

Carry Network Output Equations

The following equations assume active HI Carry Network inputs and produce active LO results.

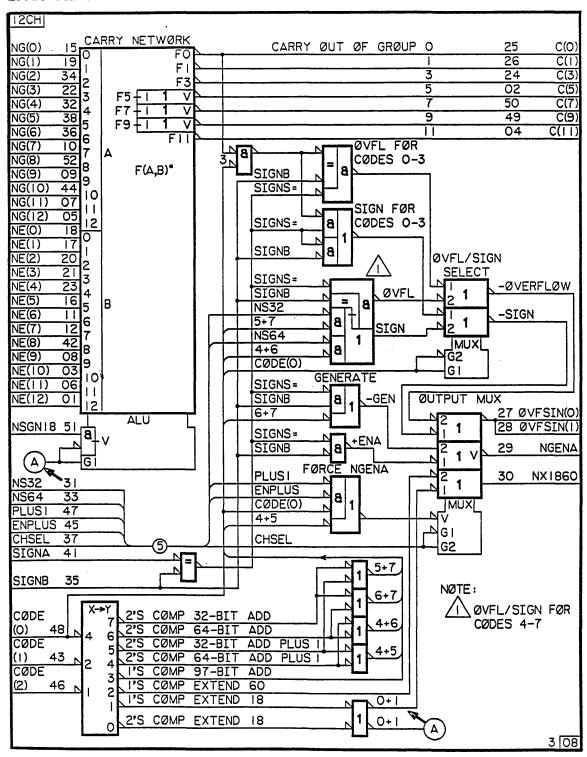
```
F0=A0
       + A1 • B0
                          F1=A1 + A2 \bullet B1
                                                   F3=A3 + A4 \bullet B3
                                + A3 • B1 • B2
       + A2 • B0 • B1
                                                          + A5 • B3 • B4
                                + A4 • B1-3
       + A3 • B0-2
                                                          + A6 • B3-5
       + A4 • B0-3
                               + A5 • B1-4
                                                         + A7 • B3-6
                               + A6 • B1-5
       + A5 • B0-4
                                                         + A8 • B3-7
       + A6 • B0-5
                              + A7 • B1-6
                                                        + A9 • B3-8
                              + A8 • B1-7
       + A7 • B0-6
                                                        + A10 • B3-9
                               + A9 • B1-8
       + A8 • B0-7
                                                        + A11 • B3-10
                               + A10 • B1-9
       + A9 • B0-8
                                                        + A12 • B3-11
       + A10 • B0-9
                              + All • Bl-10
                                                        + A0 ● B3-12
       + A11 • B0-10
                              + A12 • B1-11
                                                        + A1 • B3-12 • B0
       + A12 • B0-11
                               + A0 • B1−12
                                                        + A2 • B3-12 • B0 • B1
                          F7 = A7 + A8 \bullet B7
F5=A5
       + A6 • B5
                                                   F9=A9 + A10 \bullet B9
       + A7 • B5 • B6
                                + A9 • B7 • B8
                                                         + All • B9 • BlO
                                + A10 • B7-9
       + A8 • B5-7
                                                         + A12 • B9-11
       + A9 • B5-8
                                + A11 • B7-10
                                                         + AO • B9-12
        + A10 • B5-9
                               + A12 • B7-11
                                                         + A1 • B9-12 • B0
       + A11 • B5-10
                               + AO • B7-12
                                                         + A2 • B9-12 • B0 • B1
       + A12 • B5-11
                               + A1 • B7-12 • B0
                                                         + A3 • B9-12 • B0-2
       + A0 • B5-12
                                + A2 • B7-12 • B0 • B1
                                                         + A4 • B9-12 • B0-3
                               + A3 • B7-12 • B0-2
       + A1 • B5-12 • B0
                                                         + A5 • B9-12 • B0-4
       + A2 • B5-12 • B0 • B1 + A4 • B7-12 • B0-3
                                                        + A6 • B9-12 • B0-5
       + A3 • B5-12 • B0-2 + A5 • B7-12 • B0-4
                                                        + A7 • B9−12 • B0−6
                              + A6 • B7−12 • B0−5
       + A4 • B5-12 • B0-3
                                                        + A8 • B9−12 • B0−7
F11=A11 + A12 • B11
       + AO • B11 • B12
       + A1 • B11 • B12 • B0
       + A2 • B11 • B12 • B0 • B1
       + A3 • B11 • B12 • B0-2
       + A4 • B11 • B12 • B0-3
       + A5 • B11 • B12 • B0-4
       + A6 • B11 • B12 • B0-5
       + A7 • B11 • B12 • B0-6
       + A8 • B11 • B12 • B0-7
       + A9 • B11 • B12 • B0-8
       + A10 • B11 • B12 • B0-9
```

60458120 B

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• •			

12CH-3 Carry Network.

LOGIC SYMBOL



NOTE: ANST SYMBOLOGY FOR THE ENTIRE ARRAY.

BIAS NØNE

•

12CH-3 (Cont'd)

OPERATIONAL DESCRIPTION

The 12CH-3 symbol contains several functions: a carry network, a code translator (lower portion of symbol), AND/OR and equivalence logic which determines sign, overflow, generate, and enable, an overflow/sign select mux, and an output mux.

Carry Network

The Carry Network function is performed by an ALU whose outputs are a function of the A and B groups of inputs. The asterisk (*) following the qualifying symbol (F(A,B)*) indicates that the symbol is incomplete. Therefore, the following Carry Network information cannot be deduced from the symbol.

Active HI generates enter the array on pins NG(0-12), are weighted decimally 0-12, and designated as group A. Active HI enables enter the array on pins NE(0-12), are weighted decimally 0-12, and designated as group B.

The carry network has 7 outputs designated as F0, 1, 3, 5, 7, 9, and 11. Each output is a function of the A and B groups of inputs (refer to the Carry Network Output Equations paragraph).

Outputs F5, 7 and 9 are further controlled by gating modifier G1 and OR modifier V. G1 gates the F5, 7 and 9 outputs to output pins C(5), C(7), and C(9), respectively. G1 is active when there are code translations of 2 through 7 (not 0 or 1). V forces the F5, 7, and 9 outputs active (L0). V is active when input NSGN18 is HI AND there are code translations of 0 or 1.

Code Translator

A 3-bit code enters the array on pins CODE(0-2) and is translated. Translations of 0 and 1 are ORed together and control the Carry Network and output NX1860. A translation of 2 also controls NX1860. Translations of 3-7 control the overflow, sign, and generate functions.

Overflow For Codes 0-3

The equation for the output of the OVFL FOR CODES 0-3 network is:

((CARRY OUT OF GROUP 0 • code translation of 3)=SIGNB) • SIGNS EQUAL

Overflow/Sign for Codes 4-7

The equation for the OVFL output is:

SIGNS EQUAL • (SIGNB=(NS32 • Codes 5 or 7) + (NS64 • codes 4 or 6))

The equation for the active HI SIGN output is:

(NS32 • codes 5 or 7) + (NS64 • codes 4 or 6)

Overflow/Sign Select Mux

CODE(0) selects between the outputs of two overflow networks and two sign networks. CODE(0) is HI for codes 0-3 and LO for codes 4-7.

60458120 B 2 of 4

12CH-3 (Cont'd)

Output Mux

Input CHSEL selects between sign and overflow, generate and enable, and codes 0 or 1 and code 2.

When CHSEL is LO, gating modifier Gl is active. Gl gates the outputs from the sign, enable, and codes 0 or 1 functions to the array outputs.

When CHSEL is HI, gating modifier G2 is active. G2 gates the outputs from the overflow, generate, and code 2 functions to the array outputs.

OR modifier V forces output NGENA active (LO). V is active when the output from the Force NGENA function is ${\tt LO}$.

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Carry Network Output Equations

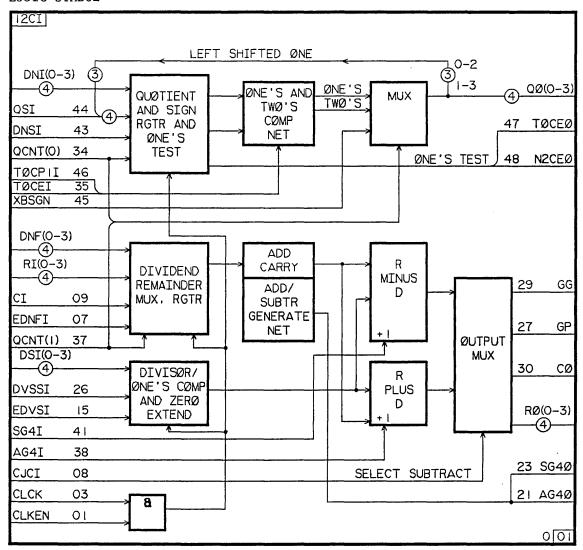
The following equations assume active HI Carry Network inputs and produce active LO results.

```
F3=A3 + A4 \bullet B3
                          F1=A1 + A2 \bullet B1
F0=A0
        + A1 • B0
        + A2 • B0 • B1
                                  + A3 • B1 • B2
                                                            + A5 • B3 • B4
        + A3 • B0-2
                                  + A4 • B1-3
                                                            + A6 • B3-5
                                 + A5 • B1-4
                                                            + A7 • B3-6
        + A4 \bullet B0-3
        + A5 \bullet B0-4
                                 + A6 • B1-5
                                                            + A8 \bullet B3-7
        + A6 • B0-5
                                 + A7 • B1-6
                                                            + A9 • B3-8
        + A7 • B0-6
                                 + A8 • B1-7
                                                            + A10 • B3-9
        + A8 • B0-7
                                 + A9 • B1-8
                                                            + A11 • B3-10
        + A9 • B0-8
                                 + A10 • B1-9
                                                            + A12 • B3-11
        + A10 • B0-9
                                 + All • Bl-10
                                                            + A0 • B3-12
                                                            + A1 • B3-12 • B0
        + All • B0-10
                                 + A12 • B1-11
        + A12 • B0-11
                                 + A0 • B1-12
                                                            + A2 • B3-12 • B0 • B1
        + A6 • B5
                           F7=A7 + A8 \bullet B7
                                                      F9=A9 + A10 \bullet B9
F5=A5
        + A7 • B5 • B6
                                  + A9 • B7 • B8
                                                            + A11 • B9 • B10
                                 + A10 • B7-9
        + A8 • B5-7
                                                            + A12 • B9-11
        + A9 • B5-8
                                  + A11 • B7-10
                                                            + A0 • B9-12
        + A10 • B5-9
                                 + A12 • B7-11
                                                            + A1 • B9-12 • B0
        + A11 • B5-10
                                 + A0 • B7-12
                                                            + A2 • B9-12 • B0 • B1
        + A12 • B5-11
                                 + A1 • B7-12 • B0
                                                            + A3 • B9-12 • B0-2
        + AO • B5-12
                                 + A2 • B7-12 • B0 • B1
                                                            + A4 • B9-12 • B0-3
        + A1 • B5-12 • B0
                                 + A3 • B7-12 • B0-2
                                                            + A5 • B9-12 • B0-4
        + A2 • B5-12 • B0 • B1 + A4 • B7-12 • B0-3
                                                            + A6 • B9-12 • B0-5
        + A3 • B5-12 • B0-2 + A5 • B7-12 • B0-4
                                                            + A7 • B9-12 • B0-6
        + A4 \bullet B5-12 \bullet B0-3
                                + A6 • B7-12 • B0-5
                                                            + A8 • B9-12 • B0-7
F11=A11 + A12 • B11
        + A0 • B11 • B12
        + A1 • B11 • B12 • B0
        + A2 • B11 • B12 • B0 • B1
        + A3 • B11 • B12 • B0-2
        + A4 • B11 • B12 • B0-3
        + A5 • B11 • B12 • B0-4
        + A6 • B11 • B12 • B0-5
        + A7 • B11 • B12 • B0-6
        + A8 • B11 • B12 • B0-7
        + A9 • B11 • B12 • B0-8
        + A10 • B11 • B12 • B0-9
```

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12CI

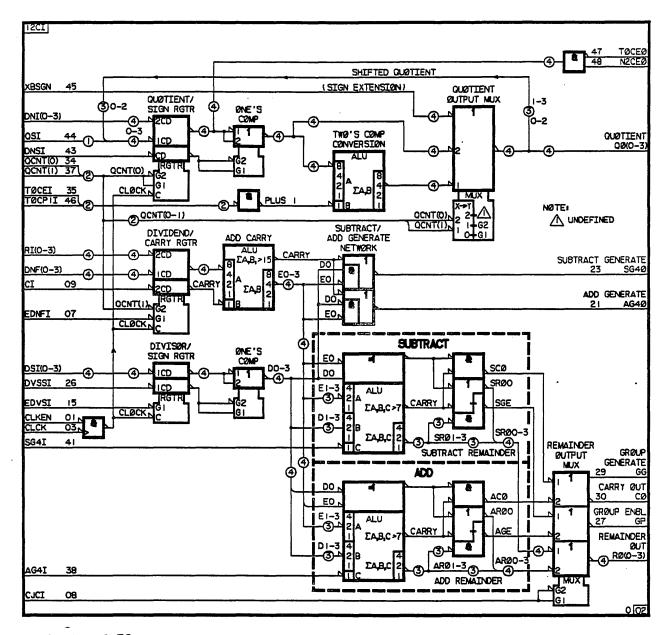
7.11	5544	
PIN NAME	REAL PIN	VIRT PIN
AG4I	38	V23
CI	09	V17
CLCK	08 03	V32 V30
CLFC	02	V33
CLKEN	01	V31
DNF(0) DNF(1)	19	V09 V11
DNF(1)	22 16	V11
DNF(2)	24	V 13
DNI(0)	33	V01
DNI(1)	32	V02
DNI(2) DNI(3)	42 36	V03 V04
DNSI	43	V08
DSI(0)	20	V24
DSI(1)	25	V25
DSI(2) DSI(3)	18 10	V26 V27
DVSSI	26	V28
EDNFI	07	V18
QCNT(0)	15 34	V29 V20
QCNT(1)		V21
OSI	44	V05
RI(0)	17	V10
RI(1) RI(2)	28 12	V12 V14
RI(3)	11	V16
SG4I	41	V22
TOCEI TOCP1I	35 46	V06 V07
XBSGN	45	V19
AG40	21	V47
CO	30	V39
GG	29	V40
GP N2CEO	27 48	V38 V45
QO(0)	51	V34
QO(1)	52	V35
QO(2) QO(3)	50 49	V36 V37
RO(0)	31	V41
RO(1)	04	V42
RO(2)	05 06	V43
RO(3) SG40	06 23	V44 V48
TOCEO	47	V46



BIAS LØ = CLFC BIAS HI = NØNE

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagrams. Refer to the ANSI symbol and its description.



BIAS LØ = CLFC BIAS HI = NØNE

OPERATIONAL DESCRIPTION

The 12CI array contains the majority of the logic required for a divide network and

12CI-0 (Cont'd)

has two somewhat independent functional areas. The two areas are the Quotient/Sign Register with its associated circuits (top one third of the symbol), and the Dividend/Carry and Divisor/Sign Registers and their associated circuits (bottom two thirds of the symbol). The only internal connections between these two areas are the QCNT (0-1), CLKEN, and CLCK control inputs which they share.

Quotient/Sign Register

The Quotient Register has two 4-bit highwayed inputs. The 4 bits in the upper highway come from input pins DNI (0-3) and are clocked into the register when control inputs QCNT (0) and CLOCK are both LO. Clock is the AND of the active LO CLKEN input and the transition to LO of the CLCK input.

The most-significant 3 bits of the lower highway (bits 0-2) connect internally to the QO (1-3) outputs. This internal feedback path performs a left end-off shift of one bit position. The least-significant bit (bit 3) enters on input pin QSI. The lower highway is clocked into the Quotient Register when QCNT (0) is HI and CLOCK is LO.

The DNSI input is clocked into the Sign Register when CLOCK is LO.

The output of the Quotient Register goes two places: the One's Complement function and an AND gate. The AND gate will be active when all 4 input bits are HI. Refer to the following paragraph for the One's Complement function.

One's Complement and Two's Complement Conversion Functions

The output of the Sign Register is the control for the One's Complement function. When the sign is LO, gating modifier G2 gates inverted data (active HI) through the function. When the sign is HI, G1 gates active LO data through the function.

The Two's Complement function converts the one's complement operation to a two's complement operation by adding one. Control inputs TOCEI and TOCPII are ANDed to form the PLUS I signal which controls the addition. The 4-bit One's Complement function enters the Two's Complement Conversion function (ALU) where it is weighted binarily I through 8 and designated as operand A. The PLUS I signal is weighted as a binary I and designated as operand B. The outputs are the summation of A and B and are weighted binarily I through 8.

Quotient Output Mux

The Quotient Output Mux is a combination of a mux and an OR function. Note that gating modifiers G2 and G1 gate in the highways from the One's Complement and Two's Complement Conversion functions respectively and the sign extension input is not gated. Thus when the sign extension is used, G1 and G2 must be inactive. Conversely, when one of the two lower highways is selected, the sign input XBSGN must be inactive (HI).

The QCNT (0-1) inputs are translated to control G1 and G2. A translation of 0 makes G1 active which gates the Two's Complement Conversion output through the mux. XBSGN must be HI.

A translation of 1 makes G2 active which gates the One's Complement output through the mux. XBSGN must be HI.

A translation of 2 produces undefined results.

A translation of 3 makes no gating modifiers active. Thus the XBSGN input is extended to the 4-bit mux output highway. This sign extension is not a part of the divide operation.

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Dividend/Carry Register

Control inputs QCNT (1), EDNFI, and CLOCK (C) control the selection and clocking of data into the Dividend/Carry Register. The combination of EDNFI LO, QCNT(1) HI, and CLOCK LO clocks the dividend (DNF (0-3) inputs) into the Dividend Register and clears the Carry Register. The combination of QCNT (1) LO, EDNFI HI, and CLOCK LO clocks the remainder and its carry (input pins RI (0-3) and CI respectively) into the Dividend and Carry Registers. External control does not allow QCNT (1) and EDNFI LO at the same time. The registers clear when both select signals are HI and CLOCK is LO.

Add Carry

The 4-bit output of the Dividend Register enters the ALU, is weighted binarily 1 through 8 and designated as operand A. The output of the Carry Register enters the ALU, is weighted a binary 1, and designated as operand B. The 4-bit ALU output (EO-3) is the summation of A and B and is weighted binarily 1 through 8. The carry output from the ALU will be LO when the summation of A and B are greater than 15.

Divisor/Sign Register and One's Complement Function

Control input EDVSI and Clock control the Divisor/Sign Register. When EDVSI and CLOCK (C) are LO, the divisor (DSI (0-3) inputs) and the divisor sign (DVSSI) enter the register. When EDVSI is HI and Clock is LO, the register clears.

The output from the Sign Register controls the One's Complement function. When the sign is LO, gating modifier G2 gates inverted data (active HI) through the function. When the sign is HI, G1 gates active LO data through the function.

Subtract/Add Generate Network

The Subtract Generate signal will be LO when the following equation is active: Carry + $(\overline{D0} \bullet E0)$

The Add Generate signal will be LO when the following equation is active: Carry + (DO • EO)

Subtract and Add Networks

The Subtract network subtracts the divisor from the dividend and produces a 4-bit remainder (SR00-3), a group generate (SCO), and a group enable (SGE).

The Add network adds the divisor to the dividend and produces a 4-bit remainder (ARO 0-3), a group generate (ACO), and a group enable (AGE).

The only difference between the two networks is that the subtract network inverts the divisor (B operand) before adding. This description will deal only with the subtract network.

The subtract network consists of an ALU which produces remainder bits 1-3 and a carry signal, and exclusive OR and AND functions which produce remainder bit 0, a group generate signal, and a group enable signal.

Dividend bits 1-3 (E1-3) and divisor bits 1-3 (D1-3) enter the ALU where they are each weighted binarily 1 through 4 and designated as operands A and B respectively. Input SG4I is a carry input to the ALU. It is weighted a binary 1 and designated as operand C. The three-bit ALU output is the summation of A, the complement of B, and C and is weighted binarily 1 through 4. The Carry output will be LO when the summation of A, the complement of B, and C is greater than 7.

Remainder bit 0 (SR00) will be LO when the following expression is active: $(E0 \oplus D0) + Carry$

60458120 B 4 of 5

12CI-0 (Cont'd)

The group generate (SCO) will be LO when the following expression is active: (EO \oplus DO) \bullet Carry

The group enable (SGE) will be LO when the following expression is active: (EO \oplus DO) + Carry) \bullet SRO 1-3

Remainder Output Mux

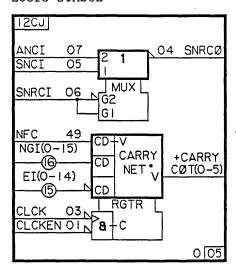
Input pin CJCI selects one of the two remainders. When CJCI is HI, gating modifier Gl selects the subtraction remainder. When CJCI is LO, G2 selects the addition remainder. The Group Generate (GG) is an inverted (active HI) copy of the Carry Output (CO).

60458120 E

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12CJ

PIN	REAL	VIRT
NAME	PIN	PIN
ANCI	07	V41
CLCK	03	V16
CLCKEN	01	V18
CLFC	51	V17
EI(0)	41	V20
EI(1)	30	V22
EI(2)	44	V24
EI(3)	48	V26
EI(4)	42	V28
EI(5)	43	V30
EI(6)	46	V32
EI(7)	45	V34
EI(8)	16	V02
EI(9)	11	V04
EI(10)	17	V06
EI(11)	09	V08
EI(12)	12	V10
EI(13)	08	V12
EI(14)	10	V14
NDIV	25	V45
NFC	49	V48
NGI(0)	50	V19
NGI(1)	35	V21
NGI(2)	32	V23
NGI (2) NGI (3) NGI (4) NGI (5) NGI (6)	36 33 38 34	V25 V27 V29 V31
NGI(7) NGI(8) NGI(9) NGI(10)	37 19 18	V33 V01 V03 V05
NGI(11)	29	V07
NGI(12)	23	V09
NGI(13)	20	V11
NGI(14)	27	V13
NGI (15)	15	V15
SNCI	05	V42
SNRCI	06	V43
AJPSS AKPSS COT(0) COT(1) COT(2)	24 21 47 02 52	V40 V39 V46 V47 V35
COT(2) COT(3) COT(4) COT(5) SNRCO	31 26 28 04	V36 V37 V38 V44



NFC IS NØT FØRCE CARRY; A HI SIGNAL INPUT FØRCES THE CARRY.

BIAS LØ = CLFC BIAS HI = NDIV

OPERATIONAL DESCRIPTION

The 12CJ-0 contains two functional elements: a carry network and a mux.

Carry Network

The data portion of the carry network symbol (top), contains three input registers clocked by the AND of CLCK and CLCKEN. Active HI generates enter on pins NGI(0-15), active LO enables enter on pins EI(0-14), and an active HI force carry signal enters on pin NFC.

The NFC register output controls OR modifier V. When V is active, it forces the carry output active (HI).

12CJ-0 (Cont'd)

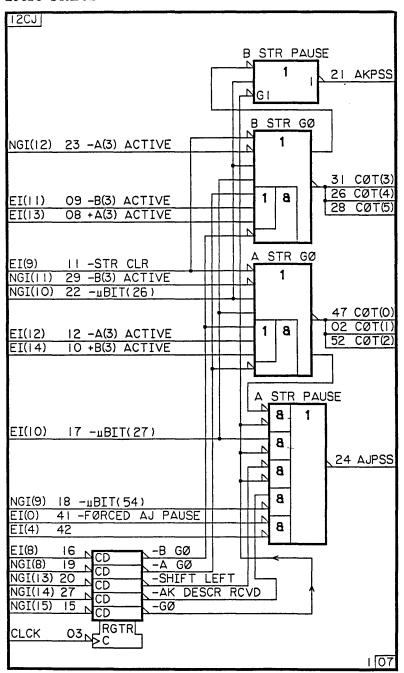
The NGI(0-15) and EI(0-14) register outputs pass through the carry network. The following carry network equation assumes active HI (+) NGI(0-15) inputs, active LO (-) EI(0-14) inputs, and produces an active HI result. Pins COT(0-5) are fanout copies of the same carry output signal.

```
COT(0-5) = NGI(0)
            + NGI(1) \bullet EI(0)
            + NGI(2) • EI(0) • EI (1)
            + NGI(3) \bullet EI(0-2)
            + NGI(4) \bullet EI(0-3)
            + NGI(5) \bullet EI(0-4)
            + NGI(6) 	€ EI(0-5)
            + NGI(7) \bullet EI(0-6)
            + NGI(8) \bullet EI(0-7)
            + NGI(9) \bullet EI(0-8)
            + NGI(10) \bullet EI(0-9)
            + NGI(11) \bullet EI(0-10)
            + NGI(12) \bullet EI(0-11)
            + NGI(13) \bullet EI(0-12)
            + NGI(14) \bullet EI(0-13)
            + NGI(15) • EI(0-14)
```

Mux

Pin SNRCI selects one of two active (HI) inputs to active (LO) output SNRCO.

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BIAS LØ = CLCKEN, CLFC, NDIV BIAS HI = NGI(O)

12CJ-1 (Cont'd)

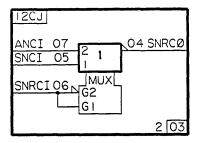
OPERATIONAL DESCRIPTION

The 12CJ-1 symbol contains the BDP Stream GO Control for the AD12-A and AD15-A computers. The following equations use signal names because of the highly specialized nature of the 12CJ-1.

- B STR PAUSE = (B STR GO + uBIT(26)) GO
- B STR GO = STR CLR + A(3) ACTIVE + $\overline{uBIT(26)}$ + $\overline{uBIT(27)}$ +((A GO + B(3) ACTIVE + A(3) ACTIVE) B GO)
- A STR GO = STR CLR + B(3) ACTIVE + $\overline{uBIT(26)}$ + $\overline{uBIT(27)}$ + ((B GO + $\overline{A(3)}$ ACTIVE + B(3) ACTIVE) A GO)

12CJ-2 Multiplexer.

LOGIC SYMBOL



NØTE:

THERE IS ONE CIRCUIT OF THIS TYPE ON EACH ARRAY. THIS CIRCUIT IS INDEPENDENT OF ANY OTHER BIAS.

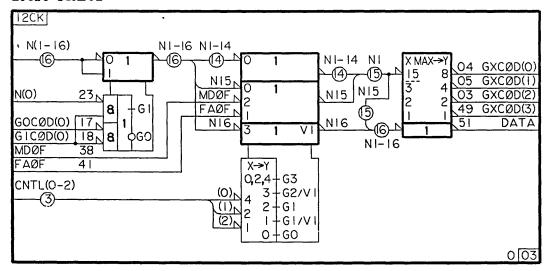
OPERATIONAL DESCRIPTION

Pin SNRCI selects one of two active (HI) inputs to active (LO) output SNRCO.

		•	
	•		
•			,

12CK

PIN NAME	REAL PIN	VIRT PIN
CNTL(0) CNTL(1) CNTL(2) FAOF	35	V17 V18 V19 V36
G0COD(G0COD(G0COD(1) 22 2) 28	V01 V05 V09 V13
G1COD(G1COD(G1COD(1) 19 2) 31	V02 V06 V10 V14
G2COD(G2COD(G2COD(0) 06 1) 08 2) 09	V03 V07 V11 V15
G3COD(G3COD(G3COD(0) 20 1) 07 2) 10	V04 V08 V12 V16
MDOF N(0) N(1) N(2)	38 23 27 15	V35 V20 V21 V22
N(3) N(4) N(5) N(6)	16 12 11 50	V23 V24 V25 V26
N(7) N(8) N(9) N(10)	01 52 45 48	V27 V28 V29 V30
N(11) N(12) N(13) N(14)	44 47 43 46	V31 V32 V33 V34
N(15) N(16) RANK2	37 36 29	V37 V38 V48
DATA	51	V47
GXCOD(GXCOD(GXCOD((1) 05 (2) 03	V46 V45 V44 V43
SCNT(0) SCNT(1) SCNT(2) SCNT(3)	26	V39 V40 V41 V42



BIAS LØ = NØNE BIAS HI = RANK 2

OPERATIONAL DESCRIPTION

The 12CK-0 receives 17 bits of data (pins N(0) - N(16)) and determines the highest-order bit which is different than bit N(0). It then produces a four-bit code which contains the weight of that bit. Sign usually enters pin N(0).

The 12CK-0 contains three functions. The function on the left can substitute input pin GOCOD(0) for pin N(0) and complement bits N(1-16). The middle function can modify the data entering the priority coder. The function on the right is the priority coder.

Sign Select and Complement Control

The function on the left selects between the two sign inputs, N(0) and GOCOD(0) and complements the data on pins N(1-16) when the selected sign is LO.

When GlCOD(0) is HI, pin N(0) controls gating modifiers GO and G1. When GlCOD(0) is LO, pin GOCOD(0) controls GO and G1.

When the selected sign is LO, Gl is active and inputs N(1-16) are complemented (gated in active HI). When the selected sign is HI, GO is active and inputs N(1-16) are gated in active LO.

Data Modify

The function in the center modifies data bits N(1-16) under the control of CNTL(0-2). Translations of CNTL(0-2) control gating modifiers GO-3 and OR modifier V1.

A translation of 0 activates GO and G3. This gates N1-16 to the priority coder.

A translation of 1 activates G1 and V1. G1 gates input FAOF into the N15 bit position and V1 forces N16 LO. Also, since G0 is not active, bits N1-14 are not gated and become zeros.

12CK-0 (Cont'd)

A translation of 2 activates G1 and G3. G1 gates input FAOF into the N15 bit position and G3 gates N16. Bits N1-14 are not gated and become zeros.

A translation of 3 activates G2 and V1. G2 gates input MDOF into the N15 bit position and V1 forces N16 LO. Bits N1-14 are not gated and become zeros.

A translation of 4 activates G3 which gates N16. N1-15 are not gated and become zeros.

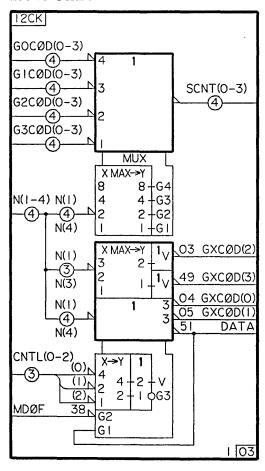
Translations of 5-7 do not activate any modifiers and therefore N1-16 become zeros.

Priority Coder

The X MAX \rightarrow Y function receives data bits N1-15 which are weighted 15-1 respectively (N1 is the most-significant bit). The priority coder produces a code which contains the weight of the highest order active (LO) bit.

The DATA output will be LO when any input (N1-16) is LO.

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BIAS LØ = RANK 2 BIAS HI = FAØF, N(O), N(5-16)

OPERATIONAL DESCRIPTION

The 12CK-1 contains two functions: a four-input mux (top function), and a priority coder (bottom function).

Mux

The highest-order active input, among input pins N(1-4), selects one of four-input highways through the mux.

N(1-4) enter a priority coder in the common control block of the mux function. They are weighted binarily 1-8 with N(1) as the most-significant bit.

The inputs and outputs of this priority coder are weighted the same so there will be only 1-bit active in the output for any input code. Gating modifier G4 is active when N(1) is active. G3 is active when N(2) is the highest-order active bit. G2 is active when N(3) is the highest-order active bit. G1 is active when N(4) is the highest-order active bit.

G1-4 select one of four input highways to output highway SCNT(0-3).

12CK-1 (Cont'd)

Priority Coder

Inputs N(1-3) enter the priority coder (X MAX -> Y in the lower function) and are weighted 3, 2, and 1 respectively. N(1) is the most-significant bit. The priority coder outputs a 2-bit code which contains the weight of the most-significant active (LO) bit. Each bit of the code (GXCOD(2-3)) can also be forced active by the OR modifier V. Refer to the Priority Coder Control paragraph for a description of V.

Inputs N(1-4) enter an OR function with three outputs, GXCOD(0-1) and DATA. When gating modifier G3 is active, all three outputs are copies of the state of the OR function. The OR function will be active if any of its inputs are active (LO). Refer to the Priority Coder Control paragraph for a description of G3.

Priority Coder Control

Pins CNTL(0-2) are translated and along with MDOF and DATA, control OR modifier V and gating modifier G3.

V is active when the following equation is satisfied:

Translation of 4 • MDOF + Translation of 2 • DATA

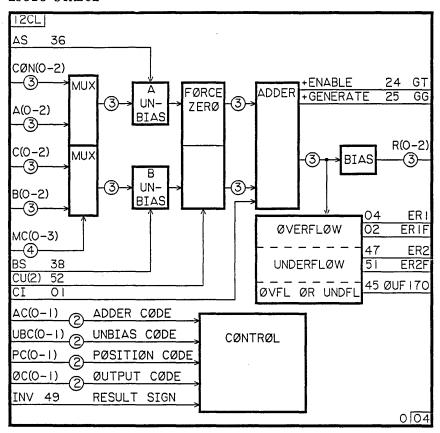
When V is active, it forces outputs GXCOD(2-3) active (LO).

G3 is active when V is not active, G3 gates outputs GXCOD(0-1).

12CL

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	23	V03
A(1) A(2)	26 15	V46 V07
AC(0)	33	V07
AC(1)	32	V23
AS D(O)	36	V08
B(0) B(1)	41 12	V10 V13
B(2)	09	V15
BS	38	V16
C(0) C(1)	16 11	V09 V12
C(2)	05	V14
CI	01	V42
CON(0) CON(1)	22	V01
CON(1)	19 20	V04 V05
CON(2)	20 03	V05
CU(0)	10	V02
CU(1)	08	V45
CU(2) EC(0)	52 48	V06 V31
EC(1)	43	V32
EXPN	46	V33
INV MC(0)	49 18	V28 V18
MC(1)	17	V19
MC(2)	07	V20
MC(3)	06	V21
OC(0) OC(1)	44 50	V29 V30
PC(0)	42	V26
PC(1)	37	V27
UBC(0) UBC(1)	35 34	V24 V25
ER1	04	V40
ER1F	02	V17
ER2	47	V41
ER2F GG	51 25	V47 V43
GT	24	V44
NR	28	V38
NRF OUF170	29 45	V39 V48
R(0)	27	V34
R(1)	21	V35
R(2) RF	30 31	V36 V37
nr	31	V3/

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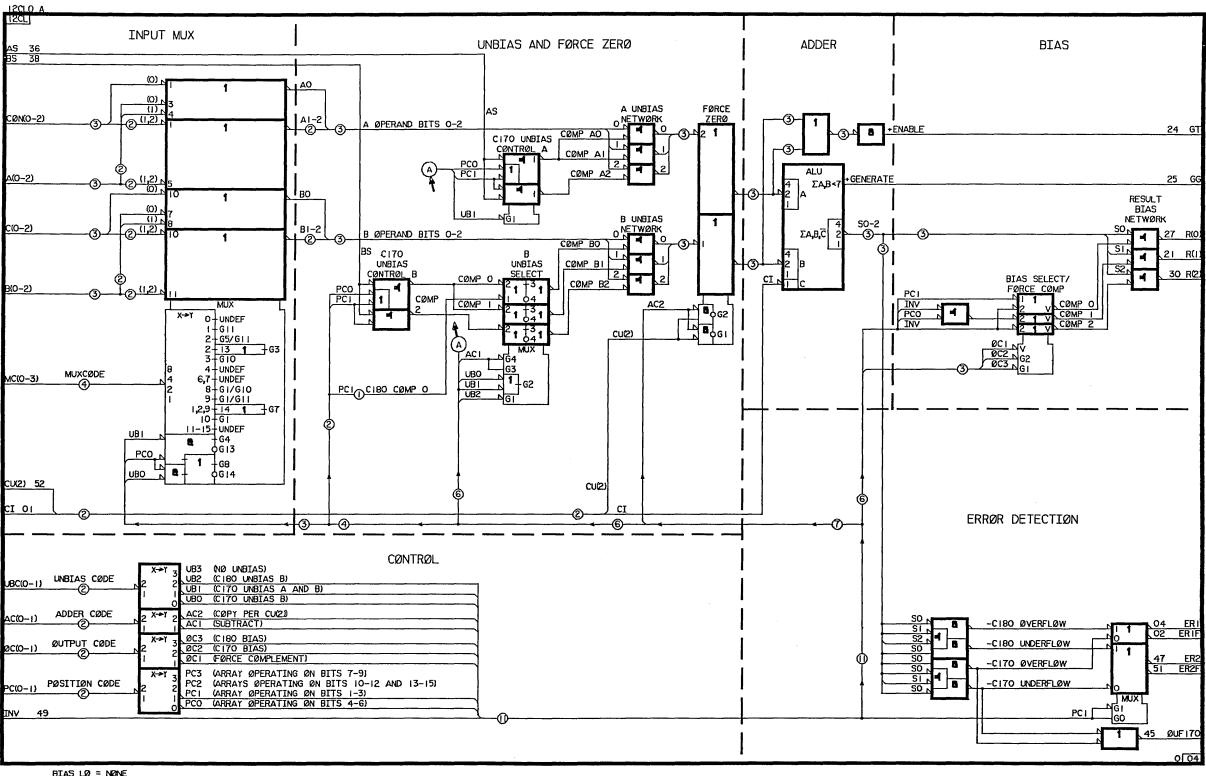


BIAS LØ = NØNE BIAS HI = EXPN, EC(O-1), CS, CU(O-1)

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagrams. Refer to the ANSI symbol and its description.

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BIAS LØ = NØNE BIAS HI = EXPN, EC(O-I), CS, CU(O-I)

12CL-0 (Cont'd)

OPERATIONAL DESCRIPTION

The 12CL-0 performs a variety of exponent arithmetic functions in the Arithmetic and Logical Network (ALN) area of the CYBER 170 Model 855 central processor.

The 12CL-0 performs the following functions:

- Adds or subtracts C170 or C180 exponents.
- Adds an integer to a C170 or C180 exponent.
- Copies one of two input operands to the output based on an external signal and removed the bias.
- Detects C170 and C180 exponent overflow and underflow.

Five 12CL-0 arrays operate on bits 1-15 of the 16-bit exponents. Exponent bit 0 is the coefficient sign and is used for control. Each 12CL-0 array operates on 3 data bits.

The Operational Description for the 12CL-0 divides into three major subjects. First there are descriptions of the inputs and outputs. Second are descriptions of C170 and C180 biased exponent format and bias removal. Third there are descriptions of the operations of each of the 6 functional areas of the 12CL-0.

Inputs

This description deals with the inputs in the context of a 15-bit network with each 12CL-0 array operating on a 3-bit slice. The most-significant array operates on bits 1-3, the next lower array operates on bits 4-7, etc. The following descriptions therefore deal with the inputs to all five 12CL-0 arrays.

AS Input

The C170 bias bit associated with the exponent on the A inputs enters pin AS on the most-significant array. The coefficient sign associated with the exponent on the A inputs enters pin AS on all other arrays.

BS Input

The C170 bias bit associated with the exponent on the B inputs enters pin BS on the most-significant array. The coefficient sign associated with the exponent on the B inputs enters pin BS on all other arrays.

CON(0-2) Inputs

A 15-bit integer representing the normalize count enters the CON(0-2) inputs (3 bits per array).

C(0-2) Inputs

A 12-bit integer representing the Address Control shift count enters the C(0-2) inputs. The most-significant 3 bits are extended with zeroes.

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12CL-0 (Cont'd)

A(0-2) and B(0-2) Inputs

Fifteen-bit exponents enter the A(0-2) and B(0-2) inputs. The exponents will both be in either C170 or C180 biased format. Refer to the C170 and C180 Exponent Format and Bias Removal paragraphs.

MC(0-3) Inputs

A 4-bit mux code enters pins MC(0-3). This mux code is translated to control the Input Mux. The same code connects to all five arrays.

CU(2) Input

A control signal which, when HI, indicates that the exponent on the B inputs is greater than the exponent on the A inputs enters pin CU(2). The 12CL-0 arrays use this signal during a copy operation to select the larger of the 2 exponents. The Force Zero function in the 12CL-0 performs the selection. The same input signal connects to all 5 arrays.

CI Input

Individual carry inputs from an external carry network enter pin CI of each array.

UBC(0-1) Inputs

A 2-bit unbias code enters pins UBC(0-1). The same code enters each array. The unbias code is translated and helps control the Input Mux and A and B Unbias Networks. Annotation on the output of each translation indicates its use.

AC(0-1) Inputs

A 2-bit adder code enters pins AC(0-1). The same code enters each array. The adder code is translated and helps control the B Unbias Network and the Force Zero function. Annotation on the output of each translation indicates its use.

OC(0-1) Inputs

A 2-bit output code enters the OC(0-1) inputs. The same code enters each array. The output code is translated and helps control the Result Bias Network. Annotation on the output of each translation indicates its use.

PC(0-1) Inputs

A 2-bit position code enters the PC(0-1) inputs. There is a unique position code biased for each array in the network with the exception of the 2 lowest-order arrays. Both low-order arrays receive the same position code. The position codes make each array in the network interpret the other controls properly for each group of bits in the network. The position code is translated and annotation on the output of each translation indicates the array position in the 15-bit network.

INV Input

The result sign enters pin INV on each array. INV helps control the Result Bias Network.

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12CL-0 (Cont'd)

Outputs

This description deals with the outputs in the context of a 15-bit network with each array operating on a 3-bit slice. The following descriptions therefore deal with the outputs from all five 12CL-0 arrays.

GT and GG Outputs

Enable (GT output) and generate (GG output) leave each array in the network and go to an external carry network.

R(0-2) Outputs

The 15-bit result leaves the network on pins R(0-2), 3 bits from each array. This 15-bit result can be in any one of three formats, C180 exponent format, C170 exponent format, or a 15-bit integer. When the result is in C170 exponent format, the highest-order 4 bits (bits 1-4) are undefined. The result coefficient sign must be inserted in these bit positions external to the 12CL-0 arrays as required.

ER1 and ER1F Outputs

The ERl and ERlF outputs are copies of the same overflow signal. The output from the most-significant array in the network (position code 1) is C180 Overflow. The output from the next lower array (position code 0) is C170 Overflow. These outputs are not used on the three least-significant arrays.

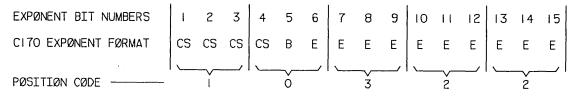
ER2 and ER2F Outputs

The ER2 and ER2F outputs are copies of the same underflow signal. The output from the most-significant array in the network (position code 1) is C180 Underflow. The outputs from the next lower array (position code 0) is C170 Underflow. These outputs are not used on the three least-significant arrays.

OUF170 Output

The OUF170 output is the OR of C170 Overflow and C170 Underflow and is used only on the second most-significant array (position code 0).

C170 Exponent Format



NØTES: 1. CS = CØEFFICIENT SIGN

- 2. B = CI70 BIAS BIT
- 3. E = DATA PØRTIØN ØF CI70 EXPØNENT
- 4. THE EXPONENT BIT NUMBERS BETWEEN THE VERTICAL LINES SHOW THE BIT DISTRIBUTION AMONG THE FIVE ARRAYS.
- 5. THE PØSITIØN CØDE SHØWN FØR EACH 3-BIT GRØUP IS THE TRANSLATIØN ØF THE 2-BIT PØSITIØN CØDE BIASED INDIVIDUALLY FØR EACH ARRAY.

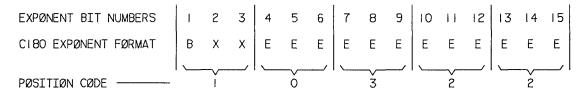
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C170 Bias Removal

The 12CL-0 array removes the C170 bias under the control of the Coefficient sign. The coefficient sign controls the C170 bias bit opposite to bits 6-15. When the coefficient sign is negative (LO) exponent bits 6-15 are complemented and bit 5 is not. When the coefficient sign is positive (HI), exponent bits 6-15 are not complemented and bit 5 is.

The 12CL-0 array extends the C170 bias bit (bit 5) to the left 1-bit position (bit 4) and then treats both bits the same when removing the bias. The 12CL-0 also makes bits 1-3 equal to the unbiased state of bits 4 and 5. This has the effect of extending unbiased bit 5 all the way to the left.

C180 Exponent Format



NØTES: 1. B = C180 BIAS BIT

- 2. X = A STATUS FIELD WHICH INDICATES AN IN-RANGE ØR ØUT-ØF-RANGE EXPØNENT. THE C180 BIAS BIT AND STATUS BITS GØ THRØUGH THE ADDER ØN THE ARRAY LIKE DATA.
- 3. E = DATA PØRTIØN ØF THE CI80 EXPØNENT
- 4. THE EXPONENT BIT NUMBERS BETWEEN THE VERTICAL LINES SHOW THE BIT DISTRIBUTION AMONG THE FIVE ARRAYS.
- 5. THE PØSITIØN CØDE SHØWN FØR EACH 3-BIT GRØUP IS THE TRANSLATIØN ØF THE 2-BIT PØSITIØN CØDE BIASED INDIVIDUALLY FØR EACH ARRAY.

PTAMAS O LOS

C180 Bias Removal

The 12CL-0 removes the C180 bias by complementing the C180 bias bit (bit 1).

Input Mux

The data portion of the Input Mux divides into two major parts, the A operand mux (top two OR functions) and the B operand mux (bottom two OR functions).

When gating modifiers select integers through these muxes, the integers pass unaltered. Note that Gl selects all 3 bits of the CON(0-2) inputs to the output of the A operand mux and GlO selects all 3 bits of the C(0-2) inputs to the output of the B operand mux.

When gating modifiers select exponents however, the most-significant bit has different gating than the 2 least-significant bits. This is because when a C170 exponent is selected, the muxes on the array in position code 0 must extend the C170 bias bit to the left 1-bit position. The C170 bias bits enter that array on input pins A(1) and B(1).

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Unbias codes of 0 and 1 and position code 0 control the C170 bias bit extension. Note in the lower part of the common control block that G4 and G8 will both be active when unbias code 1 and position code 0 are both active. Unbias code 1 indicates that both exponents are C170 and position code 0 is active for the array which operates on the C170 bias bits. G4 and G8 gate the C170 bias bits into bit 0 of the A and B operand outputs of the muxes.

G8 is active and G4 inactive when unbias code O and position code O are both active. Unbias code O indicates that only the B operand is receiving a G170 exponent.

When unbias codes of 2 or 3 are active (C180 exponent or no unbias) UBO and UB1 are both inactive making G13 and G14 active. G13 active indicates that the A operand is not a C170 exponent or this is not the array at position code 0. G14 active indicates that the B operand is not a C170 exponent or this is not the array at position code 0. G13 and G14 are used to control gating modifiers G3 and G7 (output of mux code translator).

Each mux code translation selects a pair of operands, one to the A operand mux outputs and one to the B operand mux outputs.

Mux code translations of 0, 4, 6, 7 and 11-15 produce undefined results.

A mux code translation of 1 activates gating modifier G11. G11 selects bits 1 and 2 of the exponent on input highway B. Gating modifiers G7 and G8 select bit 0. G7 is active when there is a mux code translation of 1 AND G14 is active. G7 therefore gates input bit 0 to output bit 0 (no extension). G8 is active when G14 is inactive. G8 therefore gates input bit 1 to output bit 0 extending the C170 bias bit to the left 1-bit position.

A mux code of l does not activate any gating modifiers in the A operand mux. Therefore the A operand is forced to zero.

A mux code translation of 2 activates G5 and G11 selecting exponents to both the A and B operands. A translation of 2 also selects G3 when G13 is active and G7 when G14 is active. Otherwise, G4 and/or G8 extend C170 bias bits.

A mux code translation of 3 activates G10 only. This selects an integer to the B operand and nothing (zeros) to the A operand.

A mux code translation of 5 activates no gating modifiers and therefore gates zeros to both A and B operands.

A mux code translation of 8 activates G1 and G10. This selects integers to both operands.

A mux code translation of 9 activates G1 and G11. This selects an integer to the A operand and an exponent to the B operand. G7 and G8 control the C170 bias bit extension.

A mux code translation of 10 activates G1 only. This selects an integer to the A operand and nothing (zeros) to the B operand.

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Unbias and Force Zero

The Unbias and Force Zero area divides into three major networks, the A Unbias Network with its associated control, the B Unbias Network with its associated control and the Force Zero network.

A Unbias Network

The A Unbias Network removes C170 bias and, on the array at position code 1, makes all 3 A operand bits equal to the unbiased state of the C170 bias bit. Refer to the C170 Bias Removal paragraph. The A Unbias network passes integers and C180 exponents through unaltered.

C170 Unbias Control A produces complement signals which control each A operand bit. Gating modifier G1 gates the C170 Unbias Control A output to the complement signals. Therefore when G1 is inactive, all complement signals are HI and the A operand passes through the Exclusive OR functions in the A Unbias Network unaltered. Unbias code 1 (UB1) controls G1 and is LO when a C170 unbias operation is necessary. When UB1 is LO, position codes of O and 1 and input AS control the C170 unbias operation.

The array at position codes 2 and 3 (PCO and PCl both HI) complement all 3 A operand bits when AS (coefficient sign) is LO.

The array at position code 0 (PCO LO and PCl HI) complements bit 2 when AS is LO and controls bits 0 and 1 opposite to bit 2. Bits 0 and 1 are C170 bias bits. When the C170 Unbias Control A complements bit 2, it does not complement bits 0 and 1. When the C170 Unbias Control A does not complement bit 2, it does complement bits 0 and 1.

The array at position code 1 (PCO HI and PCl LO) complements all 3 A operand bits when AS (C170 bias bit) is HI. In position code 1 the 3 A operand bits are equal to coefficient sign as they enter the A Unbias Network. Following the unbias operation they are equal to the C170 bias bit with the bias removed (i.e. equal to the unbiased state of bits 0 and 1 in the array at position code 0).

B Unbias Network

The B Unbias Network removed C170 bias, aids in the extension of C170 bias bits to all B operand bits in the array at position code 1, removes C180 bias, complements the B operand for subtract operations, and passes integers through unaltered.

The B Unbias Select network produces complement signals which control all B operand bits. Unbias codes of 0 or 1 activate gating modifier G2 which selects C170 unbias complement signals. Unbias code 2 activates G1 which selects the C180 unbias complement signal. An unbias code of 3 makes both G1 and G2 inactive blocking the C170 and C180 unbias controls. Adder code 1, (AC1) is LO for a subtract operation and therefore inverts the complement control. When AC1 is HI it does not invert the complement control.

The C170 Unbias Control B operates the same as the C170 Unbias Control A (refer to the A Unbias Network) except for the unbias codes. The unbias codes control the B Unbias Select network.

The C180 unbias operation complements the C180 bias bit which is B operand bit 0 in the array at position code $1 \cdot$

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Force Zero Network

Gating modifiers G1 and G2 are normally both active selecting both operands through the Force Zero network. An adder code of 2 and input pin CU(2) control gating modifiers G1 and G2. When AC2 is HI, both AND gates are inactive making G1 and G2 active. When AC2 is LO, CU(2) makes one of the two AND gates active making the gating modifier in its output inactive. When G1 is inactive it forces the B operand to zero. When G2 is inactive it forces the A operand to zero.

Adder

The adder is composed of 2 groups of circuits, an ALU which produces the sum (SO-2) and generate (GG) signals, and 2 circuits which produce the enable (GT) signal.

A operand bits 0-2 enter the ALU where they are weighted binarily and designated as operand A. B operand bits 0-2 enter the ALU where they are weighted binarily and designated as operand B. The carry input (input pin CI) enters the ALU where it is given a binary weight of 1 and designated as operand C.

The output of the ALU (SO-2) is weighted binarily and is the summation of A, B, and the complement of C.

The ALU also produces a generate signal which is HI when the summation of A and B is less than 7.

An OR function and an AND function produce the enable signal. The enable signal is HI when all 3-bit positions are enabled. A bit position is enabled when either or both of the operand A and B bits in that bit position are HI (zeros).

Note that no position codes enter the adder. Therefore the adder operates the same for each array in the 15-bit network.

Bias

The Result Bias Network can pass operands unaltered, add C170 or C180 bias, or force-complement the result.

The Bias Select/Force Complement network produces complement signals which control each result bit. Output codes 1, 2, and 3 control the type of operation, Force Complement, C170 Bias, or C180 Bias respectively.

When OCl is LO, OR modifier V is active and forces all three complement signals LO. This complements all 3 result bits in the Result Bias Network. When OCl is HI, V is inactive and has no effect on the complement signal.

When OC2 is LO, gating modifier G2 is active and selects C170 bias. The INV input (result sign) and position code 0 control the C170 bias operation. When the result sign is LO, all result bits are complemented except for the C170 bias bit. The C170 bias bit is bit 1 on the array at position code 0. When the result sign is HI, only the C170 bias bit is complemented.

Where OC3 is LO, gating modifier Gl is active and selects C180 bias. A C180 exponent is biased by complementing the bias bit. The C180 bias bit is bit 0 on the array at position code l.

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Error Detection

Position code 1 selects between C170 and C180 error detection. The array of position code 1 (most-significant array) detects C180 overflow and underflow. The next lower array detects C170 overflow and underflow. The error detection outputs from the 3 least-significant arrays are not connected. Therefore PCl selects between the top 2 arrays.

C180 Error Detection

The C180 error detection is relevant only when a biased C180 exponent goes through the adder. This can happen when the Input Mux selects a C180 exponent for the A operand. (Note that the A Unbias Network does not remove C180 bias.) Or the Input Mux selects a C180 exponent for the B operand and does not unbias it (Unbias code of 3).

When a biased C180 exponent is added to an unbiased quantity, the result is a biased C180 exponent. Adder outputs S0-2 on the array at position code 1 are the C180 bias bit (S0) and the 2 status field bits (S1, S2). These 3 bits indicate an in-range or out-of-range condition.

When the 2 status bits are different and the C180 bias bit is LO, there is a C180 overflow.

When the 2 status bits are different and the C180 bias bit is HI, there is a C180 underflow.

C170 Error Detection

The C170 error detection is relevant only when the adder output is an unbiased C170 exponent. At this point (exponent not biased) bits S0-2 on the array at position code 0 are the 2 bits immediately above (more significant than) the data portion of the C170 exponent. When the unbiased C170 exponent is in-range, both these bits are the same. When the arithmetic operation causes a carry out of the data portion of the exponent into S1, an out-of-range condition exists.

When SO is HI and SO and S1 are different, there is a C170 overflow.

When SO is LO and SO and SI are different, there is a C170 underflow.

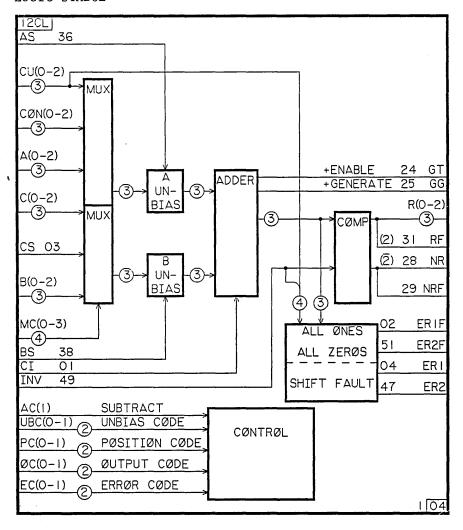
Control

The outputs from the control translation functions are all annotated for the reader's benefit even when the 12CL-0 does not need a signal from that translation. For example, an unbias code translation of 3 causes no unbias operation. The 12CL-0 does not need that signal because when the unbias code translates a 3, the inactive (HI) states of the 0-2 translations block the unbias operation.

Refer to the Input paragraphs for descriptions of the control inputs.

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LOGIC SYMBOL

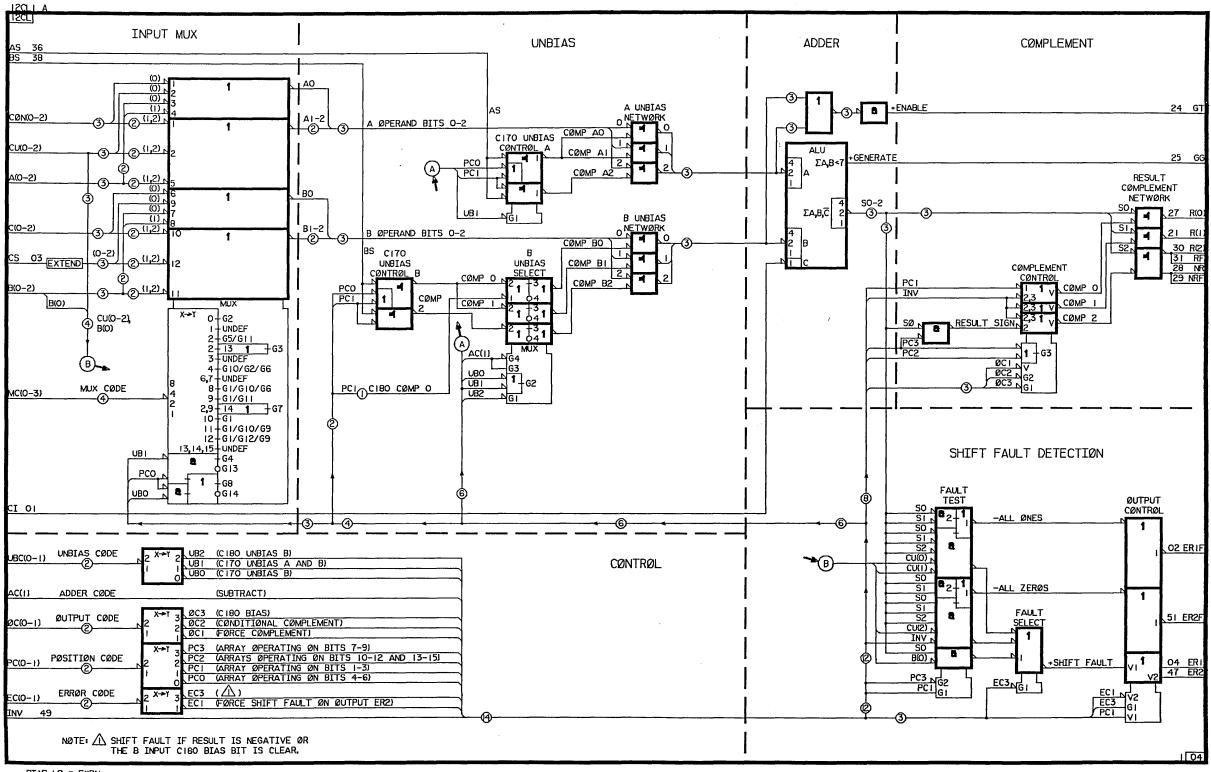


BIAS LØ = EXPN BIAS HI = AC(0)

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagrams. Refer to the ANSI symbol and its description.

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BIAS LØ = EXPN BIAS HI = AC(O)

OPERATIONAL DESCRIPTION

The 12CL-1 performs a variety of arithmetic functions on integers and exponents to determine the shift count used for operand alignment in the Arithmetic and Logical Network (ALN) area of the CYBER 170 Model 855 central processor.

The 12CL-1 performs the following functions:

- Adds an integer to C170 or C180 exponents.
- Calculates the absolute value of the difference between two C170 or C180 exponents.
- Adds or subtracts pairs of integers. The 12CL-1 array can also modify the amount of sign extension on one of the two integers.
- Force complements the result.

Five 12CL-1 arrays operate on bits 1-15 of the 16-bit exponents. Exponent bit 0 is the coefficient sign and is used for control. Each 12CL-1 array operates on 3-data bits.

The Operational Description for the 12CL-1 divides into three major subjects. First there are descriptions of the inputs and outputs. Second is a description of C170 and C180 biased exponent format and bias removal. Third, there are descriptions of the operations of each of the 6 functional areas of the 12CL-1.

Inputs

These descriptions deal with the inputs in the context of a 15-bit network with each 12CL-1 array operating on a 3-bit slice. The most-significant array operates on bits 1-3, the next lower array operates on bits 4-7, and so forth. The following descriptions therefore deal with the inputs to all 5 12CL-1 arrays.

AS Input

The C170 bias bit associated with the exponent on the A inputs enters pin AS on the most-significant array. The coefficient sign associated with the exponent on the A inputs enters pin AS on all other arrays.

BS Input

The C170 bias bit associated with the exponent on the B inputs enters pin BS on the most-significant array. The coefficient sign associated with the exponent on the B inputs enters pin BS on all other arrays.

CON(0-2) Inputs

A 7-bit integer representing a literal shift count enters the CON(0-2) inputs. These 7 bits are right-justified and extended with HIs to make a 15-bit integer. Each 12CL-1 array receives a 3-bit slice of the 15-bit integer.

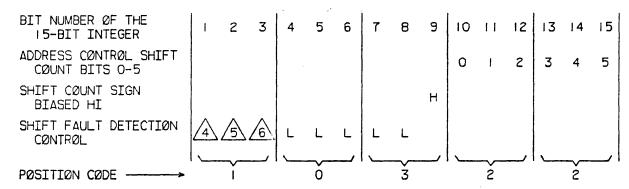
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CU(0-2) Inputs

A 6-bit integer representing the most-significant 6-bits of the Address Control Shift Count enters the CU(0-2) inputs. The 6 bits occupy bits 10-15 of a 15-bit integer. Bit 9 of the 15-bit integer is the sign of the shift count and is biased HI.

The remaining bits (1-8) of the 15-bit integer are not used for arithmetic operations in the 12CL-1 arrays. They control the Shift Fault Detection functions in the lower right portion of the symbol. Each 12CL-1 array receives a 3-bit slice of the 15-bit integer. The following figure shows the format of the 15-bit integer.

CU INPUT FORMAT



- NØTES: I. L = BIASED LØ, H = BIASED HI.
 - 2. THE 15-BIT INTEGER BIT NUMBERS BETWEEN THE VERTICAL LINES SHOW THE BIT DISTRIBUTION AMONG THE FIVE 12CL-1 ARRAYS.
 - 3. THE PØSITIØN CØDE SHØWN FØR EACH 3-BIT GRØUP IS THE TRANSLATIØN ØF THE 2-BIT PØSITIØN CØDE BIASED INDIVIDUALLY FØR EACH ARRAY.
 - 4

THE SIGNAL ENTERING BIT I INDICATES, WHEN LØ. THAT BITS 4-6 ØF THE 15-BIT ADDER ØUTPUTS ARE ALL LØ (ONES). THE 15-BIT ADDER ØUTPUT REFERS TØ THE ADDER ØUTPUTS FRØM ALL 5 12CL-1 ARRAYS. REFER TØ THE ERIF ØUTPUT PARAGRAPH.



THE SIGNAL ENTERING BIT 2 INDICATES, WHEN LØ. THAT BITS 7 AND 8 OF THE 15-BIT ADDER ØUTPUTS ARE BØTH LØ (ØNES). REFER TØ THE ERIF ØUTPUT PARAGRAPH.



THE SIGNAL ENTERING BIT 3 INDICATES, WHEN LØ, THAT BITS 4-6 ØF THE 15-BIT ADDER ØUTPUTS ARE ALL HI (ZERØS). REFER TØ THE ER2F ØUTPUT PARAGRAPH.

C(0-2) Inputs

A 6-bit integer representing the least-significant 6 bits of the Address Control Shift Count enters the C(0-2) inputs. These 6-bits are right-justified and sign-extended to make a 15-bit integer. Each 12CL array receives a 3-bit slice of the 15-bit integer.

A(0-2) and B(0-2) Inputs

Fifteen-bit exponents enter the A(0-2) and B(0-2) inputs. The exponents will both be in either C170 or C180 biased format. Refer to the C170 and C180 Exponent Format and Bias Removal.

CS Input

The sign of the Address Control Shift Count enters pin CS on the most-significant four arrays. Pin CS on the least-significant array is biased HI.

MC(0-3) Inputs

A 4-bit mux code enters pins MC(0-3). This mux code is translated to control the Input Mux. Three sets of mux codes feed the 5 12CL-1 arrays. One set of mux code bits controls the most-significant 3 arrays (bits 1-9). A second set of mux code bits controls the next-lower array (bits 10-12), and a third set of mux code bits controls the least-significant array (bits 13-15).

CI Input

Individual carry inputs from an external carry network enter pin CI of each array.

UBC(0-1) Inputs

A 2-bit unbias code enters pins UBC(0-1). The same code enters each array. The unbias code is translated and helps control the Input Mux and A and B Unbias Networks. Annotation on the output of each translation indicates its use.

AC(1) Input

The signal which enters pin AC(1) is HI for add operations and LO for subtract operations. The AC(1) input helps control the B Unbias Network.

OC(0-1) Inputs

A 2-bit output code enters the OC(0-1) inputs. The same code enters each array. The output code is translated and helps control the Complement network. Annotation on the output of each translation indicates its use.

PC(0-1) Inputs

A 2-bit position code enters the PC(0-1) inputs. There is a unique position code biased for each array in the network with the exception of the two lowest-order arrays. Both low-order arrays receive the same position code. The position codes make each array in the network interpret the other controls properly for each group of bits in the network. The position code is translated and annotation on the output of each translation indicates the array position in the 15-bit network.

EC(0-1) Inputs

A 2-bit error code enters the EC(0-1) inputs. The error code is translated and helps control the Shift Fault Detection function. Annotation on the output of each translation indicates its use.

INV Input

Input pin INV serves two purposes. On the most-significant array INV helps control the Shift Fault Detection functions. On the four least-significant arrays INV helps control the complementing of the result when that result is the absolute value of the difference between 2 exponents.

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Pin INV on the most-significant array connects to a signal which, when LO, indicates that bits 7 and 8 of the result output from the adder are both 0's. Shift Fault Detection functions on the most-significant array use this signal along with similar information on pins CU(0-2) and the adder output, to determine if the shift count is greater than 127. The Shift Fault Detection paragraphs describe the use of this control.

Pin INV has the following connections on the four least-significant arrays (in descending order of significance): Bias LO, Bias HI, Result Sign, Result Sign. The Result Bias Network paragraphs describe the use of this control.

Outputs

These descriptions deal with the outputs in the context of a 15-bit network with each array operating on a 3-bit slice. The following descriptions therefore deal with the outputs from all five 12CL-1 arrays.

GT and GG Outputs

Enable (GT output) and generate (GG output) signals leave each array in the network and go to a carry network which is external to the 12CL-1 arrays.

R(0-2), RF, NR, and NRF Outputs

The 15-bit result leaves the network on pins R(0-2), 3 bits from each array. Since the result is a shift count with a maximum value of 127, the lowest-order 7 result bits (9-15) contain the shift count. Bits 1-8 are all result sign.

Output pin RF is a copy of the R(2) output.

Output pins NR and NRF are both copies of the complement (active HI) of the R(2) output.

ER1F Output

The ERIF output is used only on the arrays operating on bits 4-6 (position code 0) and 7-9 (position code 3).

The ERIF output on the array at position code 0 is LO when the adder result bits 4-6 are all ones. This signal connects to input pin CU(0) on the most-significant array (position code 1).

The ERIF output on the array at position code 3 is LO when the adder result bits 7 and 8 are both LO (ones). This signal connects to input pin CU(1) on the most-significant array.

ER2F Output

The ER2F output is used only on the arrays operating on bits 4-6 (position code 0) and 7-9 (position code 3).

The ER2F output on the array at position code 0 is LO when the adder result bits 4-6 are all HI (zeros). This signal connects to input pin CU(2) on the most-significant array (position code 1).

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The ER2F output on the array at position code 3 is LO when the adder result bits 7 and 8 are both HI (zeros). This signal connects to input pin INV on the most-significant array.

ER1 and ER2 Outputs

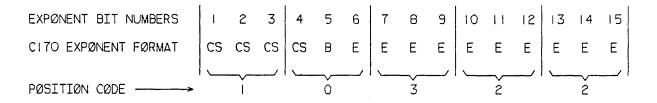
The ER1 and ER2 outputs are used only on the most-significant array (position code 1).

The ERl output is HI when there is a shift fault. A shift fault exists when the adder result is greater than 127 (bits 1-8 are not all alike). The 8 most-significant bits should all be sign and therefore all alike.

The ERl output is also HI when the sign of the result is negative or the C180 exponent on the B inputs is negative. These are also shift faults.

The ER2 output is the same as the ER1 output except that it can be forced HI with an error code translation of $l_{\:\raisebox{1pt}{\text{\circle*{1.5}}}}$

C170 Exponent Format



NØTES: I. CS = CØEFFICENT SIGN

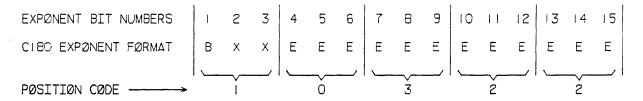
- 2. B = CI70 BIAS BIT
- 3. E = DATA PØRTIØN ØF C170 EXPØNENT
- 4. THE EXPONENT BIT NUMBERS BETWEEN THE VERTICAL LINES SHOW THE BIT DISTRIBUTION AMONG THE FIVE ARRAYS.
- 5. THE PØSITIØN CØDE SHØWN FØR EACH 3-BIT GRØUP IS THE TRANSLATIØN ØF THE 2-BIT PØSITIØN CØDE BIASED INDIVIDUALLY FØR EACH ARRAY.

C170 Bias Removal

The 12CL-1 array removes the C170 bias under the control of the coefficient sign. The coefficient sign controls the C170 bias bit opposite to bits 6-15. When the coefficient sign is negative (LO) exponent bits 6-15 are complemented and bit 5 is not. When the coefficient sign is positive (HI), exponent bits 6-15 are not complemented and bit 5 is.

The 12CL-1 array extends the C170 bias bit (bit 5) to the left 1-bit position (bit 4) and then treats both bits the same when removing the bias. The 12CL-1 also makes bits 1-3 equal to the unbiased state of bits 4 and 5. This has the effect of extending unbiased bit 5 all the way to the left.

C180 Exponent Format



NØTES: 1. B = C180 BIAS BIT

- 2. X = A STATUS FIELD WHICH INDICATES AN IN-RANGE ØR ØUT-ØF-RANGE EXPØNENT. THE C180 BIAS BIT AND STATUS BITS GØ THRØUGH THE ADDER ØN THE ARRAY LIKE DATA.
- 3. E = DATA PØRTIØN ØF THE CI80 EXPØNENT
- 4. THE EXPONENT BIT NUMBERS BETWEEN THE VERTICAL LINES SHOW THE BIT DISTRIBUTION AMONG THE FIVE ARRAYS.
- 5. THE PØSITIØN CØDE SHØWN FØR EACH 3-BIT GRØUP IS THE TRANSLATIØN ØF THE 2-BIT PØSITIØN CØDE BIASED INDIVIDUALLY FØR EACH ARRAY.

C180 Bias Removal

The 12CL-1 removes the C180 bias by complementing the C180 bias bit (bit 1).

Input Mux

The data portion of the Input Mux divides into two major parts, the A operand mux (top two OR functions) and the B operand mux (bottom two OR functions).

When gating modifiers select integers through these muxes, the integers pass unaltered. Note that GI selects all 3 bits of the CON(0-2) inputs to the output of the A operand mux.

When gating modifiers select exponents however, the most-significant bit has different gating than the 2 least-significant bits. This is because when a C170 exponent is selected, the muxes on the array in position code 0 must extend the C170 bias bit to the left one bit position. The C170 bias bits enter that array on input pins A(1) and B(1).

Unbias codes of 0 and 1 and position code 0 control the C170 bias bit extension. Note in the lower part of the common control block that G4 and G8 will both be active when unbias code 1 and position code 0 are both active. Unbias code 1 indicates that both exponents are C170 and position code 0 is active for the array which operates on the C170 bias bits. C4 and C8 gate the C170 bias bits into bit 0 of the A and B operand outputs of the muxes.

G8 is active and G4 inactive when unbias code 0 and position code 0 are both active. Unbias code 0 indicates that only the B operand is receiving a C170 exponent.

When unbias codes of 2 or 3 are active (C180 exponent or no unbias) UBO and UB1 are both inactive making G13 and G14 active. G13 active indicates that the A operand is not a C170 exponent or this is not the array at position code 0. G14 active indicates that the B operand is not a C170 exponent or this is not the array at position code 0. G13 and G14 are used to control gating modifiers G3 and G7 (output of mux code translator).

Each mux code translation selects a pair of operands, one to the A operand mux outputs and one to the B operand mux outputs.

Mux code translations of 1, 3, 6, 7 and 13-15 produce undefined results.

A mux code translation of 0 activates gating modifier G2. G2 selects all three CU inputs. A mux code translation of 0 does not activate any gating modifiers used in the B operand mux. Therefore the B operand is forced to zero.

A mux code translation of 2 activates G5 and G1l selecting exponents (A and B inputs) to both the A and B operands. A translation of 2 also selects G3 when G13 is active and G7 when G14 is active. Otherwise, G4 and/or G8 extend C170 bias bits.

A mux code translation of 4 activates G10, G2, and G6. G10 and G6 select all three C inputs to the B operand output of the mux. G2 selects all three CU inputs to the A operand output of the mux.

A mux code translation of 5 activates no gating modififiers and therefore gates zeros to both A and B operands.

A mux code translation of 8 activates G1, G10, and G6. This selects integers (CON and C inputs) to both operands.

A mux code translation of 9 activates G1 and G11. This selects an integer to the A operand and an exponent to the B operand. G7 and G8 control the G170 bias bit extension.

A mux code translation of 10 activates G1 only. This selects an integer to the A operand and nothing (zeros) to the B operand.

A mux code translation of 11 activates G1, G10, and G9. G1 selects all 3 bits of the CON inputs to the A operand output of the mux. G10 and G9 select C(1, 2) and CS to the B operand output of the mux. Input pin CS is the sign of the Address Control Shift Count and therefore sign-extends the most-significant of the 3 bits selected to the B operand outputs of the mux.

A mux code translation of 12 activates G1, G12, and G9. G1 selects all 3 bits of the CON inputs to the A operand output of the mux. G12 and G9 select the CS input to all 3 bits of the B operand output of the mux. This sign-extends all 3 bits of the B operand.

Unbias

The Unbias area divides into two major networks, the A Unbias Network with its associated control and the B Unbias Network with its associated control.

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A Unbias Network

The A Unbias Network removes C170 bias and, on the array at position code 1, makes all 3 A operand bits equal to the unbiased state of the C170 bias bit. Refer to the C170 Bias Removal paragraph. The A Unbias Network passes integers and C180 exponents through unaltered.

C170 Unbias Control A produces complement signals which control each A operand bit. Gating modifier G1 gates the C170 Unbias Control A output to the complement signals. Therefore when G1 is inactive, all complement signals are HI and the A operand passes through the Exclusive OR functions in the A Unbias Network unaltered. Unbias code 1 (UB1) controls G1 and is LO when a C170 unbias operation is necessary. When UB1 is LO, position codes of 0 and 1 and input AS control the C170 unbias operation.

The arrays at position codes 2 and 3 (PCO and PCl both HI) complement all 3 A operand bits when AS (coefficient sign) is LO.

The array at position code 0 (PCO LO and PCl HI) complements bit 2 when AS is LO and controls bits 0 and 1 opposite to bit 2. Bits 0 and 1 are C170 bias bits. When the C170 Unbias Control A complements bit 2, it does not complement bits 0 and 1. When the C170 Unbias Control A does not complement bit 2, it does complement bits 0 and 1.

The array at position code l (PCO HI and PC1 LO) complements all 3 A operand bits when AS (C170 bias bit) is HI. In position code l the three A operand bits are equal to coefficient sign as they enter the A Unbias Network. Following the unbias operation they will be equal to the C170 bias bit with the bias removed (i.e. equal to the unbiased state of bits 0 and l in the array at position code 0).

B Unbias Network

The B Unbias Network removes C170 bias, aids in the extension of C170 bias bits to all B operand bits in the array at position code 1, removes C180 bias, complements the B operand for subtract operations, and passes integers through unaltered.

The B Unbias Select network produces complement signals which control all B operand bits. Unbias codes of 0 or 1 activate gating modifier G2 which selects C170 unbias complement signals. Unbias code 2 activates G1 which selects the C180 unbias complement signal. An unbias code of 3 makes both G1 and G2 inactive blocking the C170 and C180 unbias controls. Adder code AC1 is LO for a subtract operation and therefore inverts the complement control. When AC1 is HI it does not invert the complement control.

The C170 Unbias Control B operates the same as the C170 Unbias Control A (refer to the A Unbias Network) except for the unbias codes. The unbias codes control the B Unbias Select network.

The C180 unbias operation complements the C180 bias bit which is B operand bit 0 in the array at position code 1.

Adder

The adder is composed of two groups of circuits, an ACU which produces the sum (SO-2) and generate (GG) signals, and two circuits which produce the enable (GT) signal.

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A operand bits 0-2 enter the ALU where they are weighted binarily and designated as operand A. B operand bits 0-2 enter the ALU where they are weighted binarily and designated as operand B. The carry input (input pin CI) enters the ALU where it is given a binary weight of 1 and designated as operand C.

The output of the ALU (SO-2) is weighted binarily and is the summation of A, B, and the complement of C.

The ALU also produces a generate signal which is HI when the summation of A and B is less than 7.

An OR function and an AND function produce the enable signal. The enable signal is HI when all 3-bit positions are enabled. A bit position is enabled when either or both of the operand A and B bits in that bit position are $0^{\circ}s$.

Note that no position codes enter the adder. Therefore the adder operates the same for each array in the 15-bit network.

Complement

The Result Complement Network consists of Exclusive ORs which can complement each result bit.

The Complement Control function produces complement signals which control each result bit. Output code translations of 0-3 control the type of operation.

Output Code 0

An output code translation of 0 makes gating modifiers G1, G2, and OR modifier V all inactive. This makes all three complement signals (COMPO-2) inactive and the result passes through the Result Complement Network unaltered.

Output Code 1

An output code translation of 1 makes OR modifier V active. V forces all three complement signals active (LO) which complements all 3 result bits.

Output Code 2

An output code translation of 2 makes gating modifier G2 active. G2 is used in the upper part of the Complement Control to enable a conditional complement operation. Position codes 0-3, input pin INV, and Result Sign signal also control the conditional complement operation.

On the array at position code 1 (PC2, PC3 HI) gating modifier G3 and the Result Sign signal are both inactive (HI). Therefore all three complement signals are inactive and bits 1-3 of the 15-bit result pass unaltered through the Result Complement Network.

On the array at position code 0 (PC2, PC3 HI), gating modifier G3 and the Result Sign signal are both inactive. Therefore all three complement signals are inactive and bits 4-6 of the 15-bit result are unaltered.

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On the array at position code 3 (PC3 LO) gating modifier G3 is active and the Result Sign signal is enabled (i.e. the Result Sign signal can follow the SO output from the adder which on this array is the result sign). Gating modifiers G2 and G3 are both active enabling the INV input to control the function. The INV input however, is biased HI on this array. Thus the Comp O and Comp I signals are inactive and the Result Sign signal controls the Comp 2 signal. Bits 7 and 8 of the 15-bit result pass unaltered and bit 9 (controlled by Comp 2) is complemented when Result Sign is LO.

On the arrays at position code 2 (PC2 LO), gating modifier G3 is active. G2 and G3 active enable INV to control the complement signals. The INV input on these two least-significant arrays connects to the result sign. Thus bits 10-15 of the 15-bit result are complemented when the result sign is LO.

Output Code 3

An output code translation of 3 makes Gl active. This output code is never used but if it was, it would complement the most-significant bit in the 15-bit result. Gl active and PCl active make Comp 0 active for the most-significant bit.

Shift Fault Detection

The Shift Fault Detection area determines if the shift count is greater than 127, if the B operand C180 exponent is negative, or if the result sign is negative. The most-significant three arrays (position codes 1, 0, and 3) perform all the tests.

Error codes control the type of test. The following is a list of the four error code translations and the tests they control.

- Error Code 0 Shift fault when result is greater than 127.
- Error Code 1 Same as error code 0 except force the ER2 output HI.
- Error Code 2 Same as error code 0.
- Error Code 3 Shift Fault if result is negative or if the C180 exponent on the B inputs is negative (bias bit clear).

Since error codes 0-2 all test for the same thing, this description will first describe the three most-significant arrays operating with EC3 HI and then it will describe them with EC3 LO.

Error Codes 0-2 And Position Code 3 (Array Operating on Bits 7-9)

Two AND gates in the Fault Test function control the All Ones signal. Two more AND gates control the All Zeros signal. The top AND gate in each pair tests the SO and Sl outputs of the adder. In this array they are bits 7 and 8 of the 15-bit result. The lower AND gate in each pair tests all 3 adder result bits and 2 input pins each. These lower AND gates are not relevant on this array.

Gating modifier Gl in the Fault Test function is active because position code l is HI. G2 is active because position code 3 is LO. G1 and G2 gate the test of bits 7 and 8 to the A11 Ones and A11 Zeros signals.

Gating modifier Gl in the Output Control function is active because EC3 is HI. Therefore the All Ones and All Zeros signals leave the array on pins ER1F and ER2F respectively. Pins ER1F and ER2F connect to pins CU(1) and INV respectively on the most-significant array.

The Fault Select function and output pins ER1 and ER2 are not used on this array.

Error Codes 0-2 And Position Code 0 (array operating on bits 4-6)

In the Fault Test function, the lower AND gates in each pair control the All Ones and All Zeros tests. Input pins CU(0-2) and INV are biased LO on this array. Gl is active because PCl is HI. G2 is inactive because PC3 is HI. G2 inactive blocks the upper (two input) AND gates in each pair. The lower AND gate in each pair tests all 3 adder result bits (4-6) for all LOs (ones) or all HIs (zeros).

Gating modifier Gl in the Output Control function is active because EC3 is HI. Therefore the All Ones and All Zeros signals leave the array on pins ER1F and ER2F respectively. Pins ER1F and ER2F connect to pins CU(0) and CU(2) respectively on the most-significant array.

The Fault Select function and output pins ER1 and ER2 are not used on this array.

Error Codes 0-2 And Position Code 1 (array operating on bits 1-3)

In the Fault Test function, the lower AND gate in each pair controls the All Ones and All Zeros tests. Input pins CU(0-1) bring in All Ones signals from bits 4-6 and 7, 8 respectively. Pins CU(2) and INV bring in All Zeros signals from bits 4-6 and 7, 8 respectively. Gl is inactive however (PCl LO) and the All Ones and All Zeros signals do not leave the array. Instead the results of the All Ones and All Zeros tests enter the Fault Select function.

Gating modifier Gl in the Fault Select function is inactive because EC3 is HI. This blocks the lower input which comes from an AND gate which tests the result sign and B exponent bias bit. When result bits 1-8 are all ones or all zeros, no fault exists and the Shift Fault signal is LO. When bits 1-8 are not alike (shift count greater than 127), both the All Ones and All Zeros tests will result in HIs making the Shift Fault signal HI.

OR modifier V1 in the Output Control function is inactive because PC1 is LO. When V1 is active (all four lower arrays) it forces the ER1 and ER2 outputs HI.

OR modifier V2 in the Output Control function is active for error code 1 and forces the ER2 output active (HI). When V2 is inactive (error codes 0 and 2) both the ER1 and ER2 outputs carry the Shift Fault signal.

Error Code 3 And Position Codes 0 and 3 (array operating on bits 4-9)

Gating modifier Gl in the Output Control is inactive because EC3 is LO. Gl blocks the ER1F and ER2F outputs (makes them HI). This sends HIs to the CU(0-2) and INV inputs on the most-significant array.

The Fault Test and Fault Select functions and outputs ER1 and ER2 are not used on these arrays.

Error Code And Position Code 1 (array operating on bits 1-3)

In the Fault Test function, the lower AND gates which test for all ones and all zeros are both made inactive by the HIs on the CU(0-2) and INV inputs. Therefore the top two inputs to the Fault Select function are HI.

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Gating modifier Gl in the Fault Select function is active selecting the output from the bottom AND gate in the Fault Test function. This AND gate tests the most-significant adder result bit which is sign, and the B(0) input which is the B operand Cl80 exponent bias bit. When SO is LO or B(0) is HI, the AND gate is inactive and the Shift Fault signal is HI.

OR modifiers Vl and V2 in the Output Control function are inactive and the Shift Fault signal leaves the array on pins ERl and ER2.

Pins ER1F and ER2F are not used.

Control

Refer to the Input paragraphs for descriptions of the control inputs.

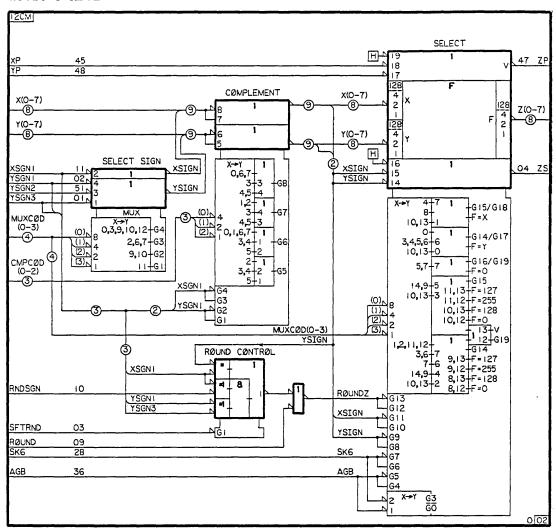
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12CM

		
NAME	REAL PIN	VIR1 PIN
AGB	36	V34
AGI1 AGI2	08 07	V45 V46
CMPCOE		V23
CMPCOD		V21
CMPCOE		V22 V24
MUXCO		V25
михсо		V26
MUXCO		V27 V28
ROUND	09	V30
SFTRND		V29
SK6 X(0)	28 46	V33 V03
X(1)	20	V04
X(2) X(3)	17 19	V05 V06
X(4)	16	V06
X(5)	38	V08
X(6) X(7)	42 44	V09 V10
XP	45	V31
XSGN1	11	V02
Y(0) Y(1)	49 18	V13 V14
Y(2)	12	V15
Y(3)	22	V16
Y(4) Y(5)	15 37	V17 V18
Y(6)	41	V19
Y(7)	43	V20
YP YSGN1	48 02	V32 V12
YSGN2	51	V11
YSGN3	01	V01
AGO	05	V47
NAGO Z(0)	06 52	V48 V36
Z(1)	21	V30
Z(2)	24	V38
Z(3) Z(4)	23 29	V39 V40
Z(5)	30	V41
Z(6)	31 50	V42
Z(7) ZP	50 47	V43 V44
ZS	04	V35

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LOGIC SYMBOL



BIAS NONE

OPERATIONAL DESCRIPTION

The 12CM-0 performs a variety of complement and mux functions on two 8-bit data paths (X(0-7)) and Y(0-7), their parity bits (XP), and their sign bits (XSIGN).

The 12CM-0 contains four major functions: Sign Select, Complement, Round Control, and Select.

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Sign Select

The MUXCOD(0-3) inputs enter the common control block of the Sign Select function where they are translated to control gating modifiers which make the sign selection.

A translation of 11 makes G1 active. G1 gates the YSGN3 input to the YSIGN output.

Translations of 9 or 10 make G2 active. G2 gates the XSGN1 input to the XSIGN output.

Translations of 2, 6, or 7 make G3 active. G3 gates the YSGN2 input to the YSIGN output.

Translations of 0, 3, 9, 10, or 12 make G4 active. G4 gates the YSGNl input to the YSIGN output.

Translations of 1, 4, 5, 8, 13, 14, or 15 activate no gating modifiers and therefore force X and Y signs to zero.

Complement

The CMPCOD(0-2) inputs are translated to control four OR functions. A single translation may feed more than one OR function. Note that a translation of 3 feeds all four OR functions. Gating modifiers G1-G4 modify the OR functions which control G5-8. G6 and G8 gate the X and Y data straight through without inversion. G5 and G7 gate active HI (inverted) data.

The four OR functions all operate in a similar manner. This description will describe the operation of only the lowest of the four OR functions.

A CMPCOD translation of 2 activates the lower OR function which makes G5 active. G5 gates Y(0-7) and YSIGN in active HI which complements this data.

Translations of 3 or 4 require that G2 also be active in order to make the OR function active. A translation of 5 requires G1.

Round Control

The equation for the output of the Round Control function follows.

(YSIGN=XSGN1) + ((XSGN1 + RNDSGN)(YSGN1 + YSGN3)) ● SFTRND

The ROUND input is ORed with the output of the Round Control and produces ROUNDZ. ROUNDZ is used in the Select function as part of the control for the Z(0-7) and ZP outputs. Refer to the Select paragraph.

Select

The data portion of the Select function (top) divides into three functions. The top function (OR Qualifying Symbol) is a mux which gates parity to output ZP. Gating modifiers G18 and G17 select between the X operand parity (input XP) or the Y operand parity (YP), respectively. The combination of G19 and OR modifier V can force the ZP output either HI or LO. These control modifiers originate in the common control block. The Select Control paragraph describes the control.

60458120 B

The middle function has an F qualifying symbol. This indicates that the symbol is incomplete and the function information is expressed by equations in the common control block. This function receives two 8-bit highwayed inputs, X and Y which are weighted binarily and designated as operand X and Y, respectively. The 8-bit output highway (outputs Z(0-7)) is also weighted binarily and designated as output operand F. Equations in the common control block (bottom of the Select function) describe the contents of F for the various control combinations. When the equation F=X is active, the function places the X operand on the output highway. When the equation F=Y is active, the function places the Y operand on the output highway. F=O means that all 8 bits are forced HI. F=127 means the lowest-order 7 bits are LO and the most-significant bit is HI (value of 127). F=255 means they are all LO. F=128 means the most-significant bit is LO and the rest are HI. The Select Control paragraph describes the control.

The lower function (OR qualifying symbol) is a mux which selects the proper sign to output ZS. Gating modifiers G14, G15 and G16 select YSIGN, XSIGN, or HI. The Select Control paragraph describes the control.

Select Control

The MUXCOD(0-3) inputs enter the common control block of the Select function where they are translated to control six OR functions. Five of the six OR functions are in a vertical row on the output side of the MUXCOD translator. The sixth OR function is on the output of the fourth and fifth OR functions. A single MUXCOD translation may feed more than one OR function. Note that a translation of 10 feeds four of the OR functions.

These OR functions are modified by gating modifiers GO-G13 which are controlled by ROUNDZ, XSIGN, YSIGN, and inputs SK6 and AGB. The OR functions produce gating modifiers G14-G19, OR modifier V, and the function control equations for F. These controls are used in the data portion of the Select function (top).

The top OR function produces gating modifiers and a function control equation which select the X operand and its sign and parity bit.

The second OR function selects the Y operand and its sign and parity bit.

The third OR functions makes all outputs HI.

The fourth OR function selects X sign, forces the F operand to binary values of 127, 255, 128, or O under the control of XSIGN, and ROUNDZ, and causes the parity output ZP to follow ROUNDZ. Note that the fourth OR function also feeds the sixth OR function.

The fifth OR function selects Y sign, forces the F operand to values of 127, 255, 128, or O under the control of YSIGN and ROUNDZ, and causes the parity output ZP to follow ROUNDZ. Note that the fifth OR function feeds the sixth OR function.

The sixth OR function is activated when either the fourth or fifth OR functions are active. G12 and G13 (controlled by ROUNDZ) control OR modifier V and G19. When the sixth OR function is active and G13 is active (ROUNDZ LO), V is active. V forces output ZP LO. When the sixth OR function is active and G12 is active (ROUNDZ HI), G19 is active. G19 gates a HI to output ZP. Thus output ZP follows ROUNDZ when the sixth OR function is active.

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The first five OR functions all operate in a similar manner. This description will describe the operation of only the fifth one (bottom).

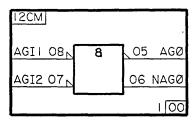
MUXCOD translations of 1, 2, 11, or 12 will activate the fifth OR function without any further modification. MUXCOD translations of 3 or 6 require that G7 also be active in order to activate the OR function. MUXCOD translations of 14 or 9 require G4 and translations of 10 or 13 require G2.

When the fifth OR function is active, the sixth OR function becomes active allowing ROUNDZ to control output ZP. Also G14 will be active without the need for any gating modifiers. F=127 is active when G9 AND G13 AND the fifth OR function are all active. G9 and G13 are active when YSIGN and ROUNDZ are LO. The remaining outputs from the fifth OR function operate in a similar manner.

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12CM-1 AND Gate.

LOGIC SYMBOL



BIAS NØNE

OPERATIONAL DESCRIPTION

(None required.)

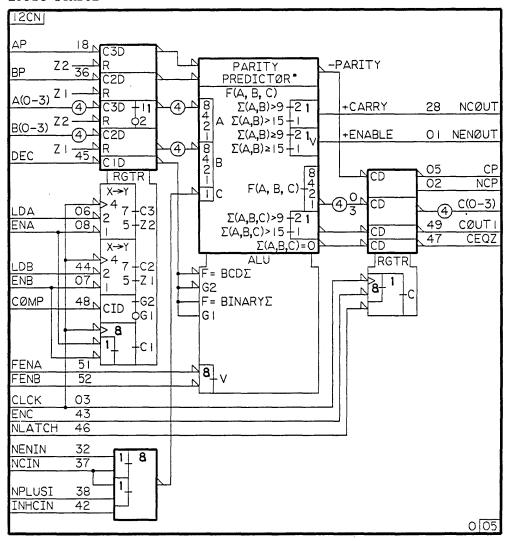
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12CN

PIN	REAL	VIRT
NAME	PIN	PIN
A(0) A(1)	15 41	V02 V03
A(2)	10	V04
A(3)	12	V05
AP	18	V01
B(0) B(1)	35 16	V07 V08
B(2)	11	V09
B(3)	09	V10
BP	36	V06
CLCK	03 48	V17 V12
DEC	45	V11
ENA	08	V14
ENB	07	V16
ENC	43	V34
FENA FENB	51 52	V18 V19
FI(0)	22	V24
FI(1)	20	V25
F1(2)	17	V26
FI(3)	24 33	V27 V28
FI(5)	34	V29
FI(6)	29	V30
FI(7) FI(8)	23	V31
INHCIN	27 42	V32 V23
LDA	06	V13
LDB	44	V15
NCIN NENIN	37 32	V21 V20
NLATCH		V41
NPLUS1	38	V22
C(0)	04	V44
C(1)	30	V45
C(2) C(3)	31 50	V46 V47
CEQZ	47	V48
COUT1	49	V40
CP CP	05 10	V42
FO(0) FO(1)	19 21	V37 V38
FO(2)	26	V39
FO(3)	25	V33
NCOUT NCP	28 02	V35 V43
NENOUT		V43

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LOGIC SYMBOL



BIAS NONE

OPERATIONAL DESCRIPTION

The 12CN-0 is an Arithmetic and Logical Unit (ALU) with input and output registers, a parity predictor, and a carry network.

Input Register

The data portion of the input register function (top left) contains registers for the A operand A(0-3) and its parity bit AP, the B operand B(0-3) and its parity bit BP, and the decimal control signal DEC.

Clock modifier C3, originating in the common control block, clocks in the A operand and its parity bit. Z2 will reset these two registers.

Gating modifiers Gl and G2 select either the true data (Gl active), or the complement data (G2 active) from the output of the A operand register.

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C2 clocks in B operand data and its parity bit. Z1 resets these two registers.

Cl clocks in the decimal control signal. This register cannot be reset.

Input Register Control

Input LDA (load A) and ENA (enable A) enter a translator along with CLCK (clock). A translation of 7 clocks in the A operand and its parity bit. A translation of 5 resets these two registers. The contents of the registers will not change for translations of 0-4, and 6.

Input LDB (load B) and ENB (enable B) enter a translator along with CLCK. A translation of 7 clocks in the B operand and its parity bit. A translation of 5 resets these two registers. The contents of the registers will not change for translations of 0-4, and 6.

The complement control signal COMP enters a register in the common control block. Cl clocks in this control signal. When the register is set, G2 is active and gates the complement of the A operand register to the ALU. When the register is reset, G1 is active and gates the true state of the A operand register to the ALU.

Cl is controlled by an OR of the two enables ANDed with clock. Cl clocks in the complement control signal and the decimal control signal.

Carry Network

The Carry Network produces a LO output when the following inputs are HI: (NENIN+NCIN)(NCIN+PLUS1)INHCIN.

Parity Predictor

The asterisk (*) in the Parity Predictor symbol indicates that the symbol is incomplete. Therefore, the following Parity Predictor information cannot be deduced from the symbol.

The Parity Predictor receives the parity bits from the two input operands and internal inputs from the ALU to determine what the parity of the result will be. The Parity Predictor does not generate parity; it only adjusts it. Bad parity (odd) on one of the two input operands will result in odd parity on the output of the Parity Predictor.

Arithmetic and Logical Unit (ALU)

The qualifying symbol in the ALU function is F(A, B, C). The F in the qualifying symbol indicates that the symbol is incomplete and the function information is expressed by equations in the common control block.

ALU Inputs

The ALU receives the 4-bit A and B operands from the input registers. It also receives a carry input from the carry network. The two 4-bit operand highways enter the ALU, are weighted binarily, and designated as operands A and B. The carry input enters the ALU, receives a binary weight of 1 and is designated as operand C.

The decimal input (DEC from the input register) controls the function of the ALU. When DEC is LO, the ALU produces a BCD summation of A, B, and C. When DEC is HI, the ALU produces a binary summation of A, B, and C. Gating modifiers Gl and G2 gate the appropriate equations for the carry and enable outputs. The ALU Output paragraph describes these outputs.

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Input pins FENA and FENB are ANDed together to control OR modifier V. When V is active, it forces the enable output NENOUT HI.

ALU Outputs

Output pin NCOUT will be HI when the summation of A and B is greater than 9 and G2 is active. G2 is active when the ALU produces a BCD summation. NCOUT will also be HI when the summation of A and B is greater than 15 and G1 is active. G1 indicates a binary summation.

Output pin NENOUT will be HI when the summation of A and B is greater than or equal to 9 and 62 is active, or the summation of A and B is greater than or equal to 15 and 61 is active, or V is active.

The 4-bit highwayed output is the BCD or binary summation of the A, B, and C operands. The result is weighted binarily and sent to the output register.

The ALU output below the result highway will be LO when the summation of A, B, and C is greater than 9 and G2 is active, or the summation of A, B, and C is greater than 15 and G1 is active.

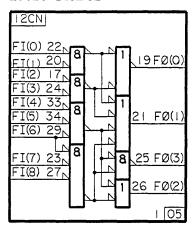
The bottom ALU output will be LO when the summation of A, B, and C is equal to zero.

Output Register

Clock modifier C clocks ALU results into the output register. Input pin NLATCH is HI for normal clocked register operation allowing the AND of inputs ENC (enable C) and CLCK to control the C modifier. When NLATCH is LO, the ENC and CLCK inputs have no effect on C. C will remain active for as long as NLATCH is active. Thus while NLATCH is active the output register cannot latch and the outputs follow the inputs.

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LOGIC SYMBOL



BIAS NONE

OPERATIONAL DESCRIPTION

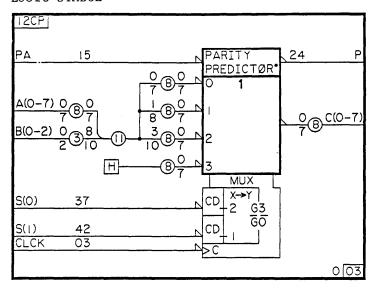
(None required.)

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12CP

PIN NAME	REAL PIN	VIRT PIN
A(0)	17	V01
A(1) A(2)	18 25	V02 V03
A(3)	08	V04
A(4)	09	V05
A(5) A(6)	19 20	V06 V07
A(7)	51	V07
AC	31	V26
B(0) B(1)	21 10	V10 V11
B(1)	11	V11
CLCK	03	V28
D	12	V29
H(0) H(1)	46 48	V33 V34
H(2)	44	V35
H(3)	45	V36
J(0) J(1)	28 36	V39 V40
J(2)	32	V41
J(3)	35	V42
L M(0)	02 41	V38 V44
M(1)	38	V45
M(2)	34	V46
MDA MDB	16 22	V25 V22
N	33	V47
PA	15	V09
S(0) S(1)	37 42	V23 V24
ZERO	43	V27
C(0)	26	V14
C(1)	27	V15 V16
C(2) C(3)	29 30	V 16 V17
C(4)	04	V17
C(5)	49	V19
C(6)	52 01	V20
C(7) E	01 06	V21 V30
F	05	V31
G	07	V32
I K	47 23	V37 V43
0	50	V48
Р	24	V13

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PA IS THE PARITY BIT FØR A(0-7). IF ANY ØPERATIØN TØGGLES AN ØDD NUMBER ØF DATA BITS, THE PARITY PREDICTØR TØGGLES THE ØUTPUT PARITY BIT P.

BIAS LØ = MDB, L BIAS HI = ZERØ, AC, MDA

OPERATIONAL DESCRIPTION

The 12CP-0 receives 11 data-bits and performs left end-off shifts of 0, 1; $\cos 3$ -bit positions or extends zeros to the 8-bit output highway. It does this by connecting (internal to the array) the required bit patterns to inputs of a mux where select signals S(0,1) select the desired shift or zero fill.

Inputs and Mux

A byte of data enters the array on pins A(0-7) and occupies bit positions 0-7 in the input highway. Input pins B(0-2) bring in the next 3 higher order-bits. B(0) is in bit position 8, B(1) in 9, and B(2) in 10. Input pin PA is the parity bit for the data byte on A(0-7). Refer to the Parity Predictor paragraph.

Clock entering the array on pin CLCK clocks the S(0,1) select signals into a register. The output of the register is translated to form G (gating) modifiers for selecting one of four input highways to the mux.

A translation of 0 selects the upper highway where input bits 0-7 are connected straight (no shift) to mux bits 0-7.

12CP-0 (Cont'd)

A translation of 1 selects input bits 1-8 which are connected with a left shift of 1 to mux bits 0-7.

A translation of 2 selects input bits 3-10 which are connected with a left shift of 3 to mux bits 0-7.

A translation of 3 selects HIs to mux bits 0-7 performing a zero fill.

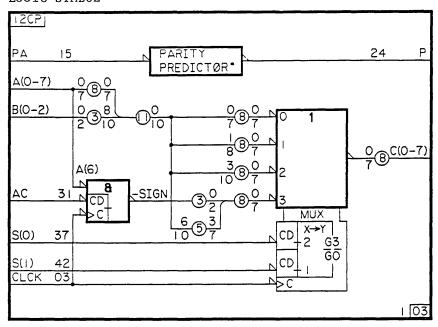
Parity Predictor

The asterisk in the Parity Predictor symbol indicates that the symbol is incomplete. Therefore, the following Parity Predictor information cannot be deduced from the symbol.

The even parity bit for A(0-7) data highway enters on pin PA. The Parity Predictor receives this parity bit and internal inputs (not shown) to perform its function.

The Parity Predictor does not generate parity. It adjusts even parity based on the input data and the operation performed. Bad parity in will result in bad parity out.

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PA IS THE PARITY BIT FØR A(0-7). IF ANY ØPERATIØN TØGGLES AN ØDD NUMBER ØF DATA BITS, THE PARITY PREDICTØR TØGGLES THE ØUTPUT PARITY BIT P.

BIAS LØ = L BIAS HI = ZERØ, MDA, MDB

OPERATIONAL DESCRIPTION

The 12CP-1 receives 11 data-bits and performs left end-off shifts of 0, 1, or 3-bit positions to the 8-bit output highway. Also while performing a left shift of 3, it can extend sign to the three least-significant bits of the output. The 12CP-1 does this by connecting (internal to the array) the required bit patterns to inputs of a mux where select signals S(0,1) select the desired shift or shift with sign extension.

Inputs and Mux

A byte of data enters the array on pins A(0-7) and occupies bit positions 0-7 in the input highway. Input pins B(0-2) bring in the next three higher order bits. B(0) is in bit position 8, B(1) in 9, and B(2) in 10. Input pin PA is the parity bit for the data byte on A(0-7). Refer to the Parity Predictor paragraph.

Clock entering the array on pin CLCK clocks the S(0,1) select signals into a register. The output of the register is translated to form G (gating) modifiers for selecting one of four input highways to the mux.

12CP-1 (Cont'd)

A translation of 0 selects the upper highway where input bits 0-7 are connected straight (no shift) to mux bits 0-7.

A translation of 1 selects input bits 1-8 which are connected with a left shift of 1 to mux bits 0-7.

A translation of 2 selects input bits 3-10 which are connected with a left shift of 3 to mux bits 0-7.

A translation of 3 selects input bits 6-10 which are connected with a left shift of 3 to mux bits 3-7. This same translation also selects the output of the Sign Control circuit and extends it to mux bits 0-3. Refer to the Sign Control paragraph.

Sign Control

Clock entering the array on pin CLCK clocks the sign control signal (input pin AC) into a register. Sign enters the array on pin A(6) and the output of the register gates it to bit positions 0-2 in the lower highway to the mux.

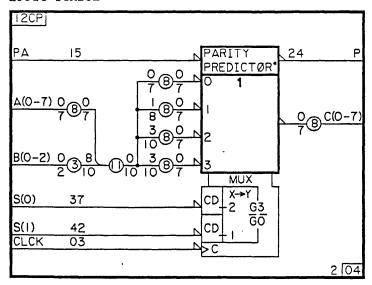
Parity Predictor

The asterisk in the Parity Predictor symbol indicates that the symbol is incomplete. Therefore, the following Parity Predictor information cannot be deduced from the symbol.

The even parity bit for A(0-7) data highway enters on pin PA. The Parity Predictor receives this parity bit and internal inputs (not shown) to perform its function.

The Parity Predictor does not generate parity. It adjusts even parity based on the input data and the operation performed. Bad parity in will result in bad parity out.

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PA IS THE PARITY BIT FØR A(0-7), IF ANY ØPERATIØN TØGGLES AN ØDD NUMBER ØF DATA BITS, THE PARITY PREDICTØR TØGGLES THE ØUTPUT PARITY BIT P.

BIAS LØ = MDA, L BIAS HI = ZERØ, AC, MDB

OPERATIONAL DESCRIPTION

The 12CP-2 receives 11 data-bits and performs left end-off shifts of 0, 1, or 3-bit positions to the 8-bit output highway. It does this by connecting (internal to the array) the required bit patterns to inputs of a mux where select signals S(0,1) select the desired shift.

Inputs and Mux

A byte of data enters the array on pins A(0-7) and occupies bit positions 0-7 in the input highway. Input pins B(0-2) bring in the next three higher order bits. B(0) is in bit position 8, B(1) in 9, and B(2) in 10. Input pin PA is the parity bit for the data byte on A(0-7). Refer to the Parity Predictor paragraph.

Clock entering the array on pin CLCK clocks the S(0,1) select signals into a register. The output of the register is translated to form G (gating) modifiers for selecting one of four input highways to the mux.

A translation of 0 selects the upper highway where input bits 0-7 are connected straight (no shift) to mux bits 0-7.

12CP-2 (Cont'd)

A translation of l selects input bits l-8 which are connected with a left shift of l to mux bits 0-7.

Translations of 2 or 3 select input bits 3-10 which are connected with a left shift of 3 to mux bits 0-7.

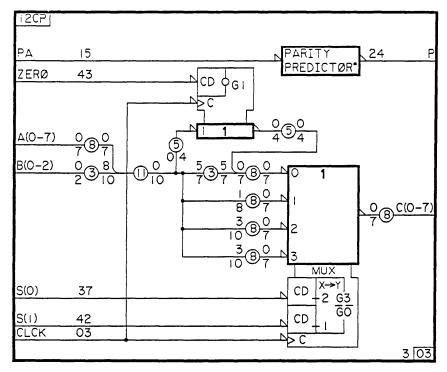
Parity Predictor

The asterisk in the Parity Predictor symbol indicates that the symbol is incomplete. Therefore, the following Parity Predictor information cannot be deduced from the symbol.

The even parity bit for A(0-7) data highway enters on pin PA. The Parity Predictor receives this parity bit and internal inputs (not shown) to perform its function.

The Parity Predictor does not generate parity. It adjusts even parity based on the input data and the operation performed. Bad parity in will result in bad parity out.

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PA IS THE PARITY BIT FØR A(0-7), IF ANY ØPERATIØN TØGGLES AN ØDD NUMBER ØF DATA BITS, THE PARITY PREDICTØR TØGGLES THE ØUTPUT PARITY BIT P.

BIAS LØ = MDA, L BIAS HI = AC, MDB

OPERATIONAL DESCRIPTION

The 12CP-3 receives 11 data-bits and performs left end-off shifts of 0, 1, or 3-bit positions to the 8-bit output highway. Also while performing a left shift of 0, bits 0-4 may be forced to zero under the control of the ZERO input. The 12CP-3 performs the shifts by connecting (internal to the array) the required bit patterns to inputs of a mux where select signals S(0,1) select the desired shift.

Inputs and Mux

A byte of data enters the array on pins A(0-7) and occupies bit positions 0-7 in the input highway. Input pins B(0-2) bring in the next three higher order bits. B(0) is in bit position 8, B(1) in 9, and B(2) in 10. Input pin PA is the parity bit for the data byte on A(0-7). Refer to the Parity Predictor paragraph.

12CP-3 (Cont'd)

Clock entering the array on pin CLCK clocks the S(0,1) select signals into a register. The output of the register is translated to form G (gating) modifiers for selecting one of four input highways to the mux.

A translation of 0 selects the upper highway where input bits 0-7 are connected straight (no shift) to mux bits 0-7. Input bits 0-4 pass through a gate controlled by the output of a register feed by input pin ZERO. Clock entering the array on pin CLCK clocks pin ZERO into a register. When the register is active (input ZERO LO when clocked), gating modifier Gl is inactive and bits 0-4 are forced to zero. When the register is inactive, Gl is active and bits 0-4 pass through to the upper mux highway.

A translation of 1 selects input bits 1-8 which are connected with a left shift of 1 to mux bits 0-7.

Translations of 2 or 3 selects input bits 3-10 which are connected with a left shift of 3 to mux bits 0-7.

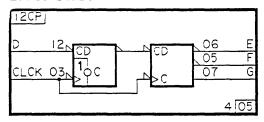
Parity Predictor

The asterisk in the Parity Predictor symbol indicates that the symbol is incomplete. Therefore, the following Parity Predictor information cannot be deduced from the symbol.

The even parity bit for A(0-7) data highway enters on pin PA. The Parity Predictor receives this parity bit and internal inputs (not shown) to perform its function.

The Parity Predictor does not generate parity. It adjusts even parity based on the input data and the operation performed. Bad parity in will result in bad parity out.

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- 1. THE BIAS USED FØR 12CP TYPE 0-3 DØES NØT AFFECT TYPE 4.
- 2 NØT CØMPATIBLE WITH TYPE 5.

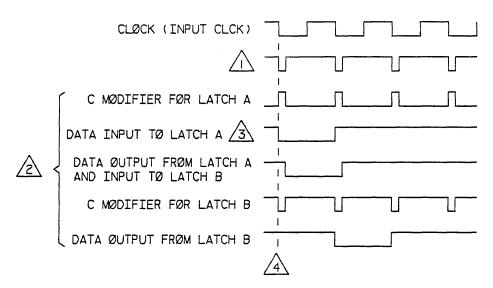
BIAS LØ = L BIAS HI = NØNE

OPERATIONAL DESCRIPTION

The above symbol consists of two latches connected in series. The latch on the left is called Latch A in this description. It has a C (clock) modifier which is inactive only during the first 2.5 ns following a LO transition of clock. The remainder of the time the C modifier for Latch A is active. Refer to the timing diagram. Since the C modifier in Latch A is active most of the time, any signal change on input D will pass to the output except during those 2.5 ns when the C modifier is inactive and Latch A holds its contents.

The latch on the right is called Latch B in this description. It has a C modifier which is active only during the first 2.5 ns following a LO transition of clock. The remainder of the time the C modifier for Latch A is inactive. Refer to the timing diagram. Latch B operates in a normal manner, clocking in data during the 2.5 ns the C modifier is active and holding its contents while the C modifier is inactive.

The use of these two latches becomes apparent when two of these arrays are connected together in series. Outputs E or F on the first array connect to input D of the next array and both arrays are clocked with the same clock signal. Without the Latch A between the two Latch Bs, a signal could pass from Latch B in the first array, all the way into Latch B in the second array during the same 2.5 ns that their C modifiers are active. The A latches are holding (latched) during that period of time and a race (short path) condition is avoided.



NØTES:



ØUTPUT ØF THE ØN-CHIP CLØCK SHAPER. THE CLØCK SHAPER FØRMS A 2.5 NS PULSE ØN THE LEADING EDGE ØF THE ACTIVE LØ CLØCK INPUT (CLCK). THE ANSI SYMBØL USES THE DYNAMIC INDICATØR (>) TØ SHØW THIS CLØCK SHAPER.



/2\ THE LØ LEVEL ØF THE WAVEFØRM INDICATES THE ACTIVE STATE.



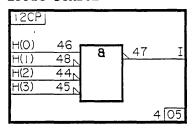
SHØWN AS IT WØULD LØØK IF CØMING FRØM LATCH B IN A PREVIØUS 12CP-4 CIRCUIT.



 4 nøte that the c mødifier før latch a is inactive when ITS DATA INPUT BECOMES ACTIVE. THE C MODIFIER FOR LATCH A BECOMES ACTIVE 2.5 NS LATER THUS DELAYING THE DATA OUTPUT FRØM LATCH A UNTIL THE C MØDIFIER FØR LATCH B BECØMES INACTIVE. LATCH B MUST THEN WAIT FOR THE NEXT CLOCK BEFØRE IT CAN SET.

12CP-4 AND Gate (Sheet 2).

LOGIC SYMBOL



- 1. THE BIAS USED FØR 12CP TYPE O-3 DØES NØT AFFECT TYPE 4.
- 2 NØT CØMPATIBLE WITH TYPE 5.

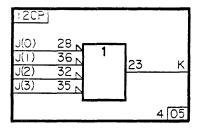
BIAS LØ = L BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

12CP-4 OR Gate (Sheet 3).

LOGIC SYMBOL



- 1. THE BIAS USED FØR 12CP TYPE O-3 DØES NØT AFFECT TYPE 4.
- 2 NØT CØMPATIBLE WITH TYPE 5.

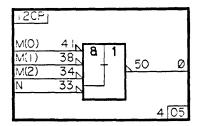
BIAS LØ = L BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

12CP-4 AND/OR Gate (Sheet 4).

LOGIC SYMBOL



I. THE BIAS USED FØR 12CP TYPE O-3 DØES NØT AFFECT TYPE 4.

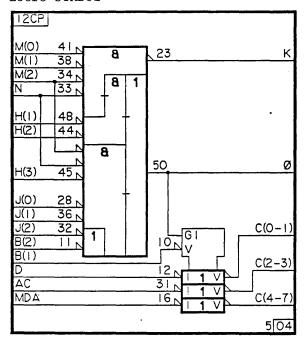
2 NØT CØMPATIBLE WITH TYPE 5.

BIAS LØ = L BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

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BIAS LØ = A(O-7), PA, CLCK, J(3), H(0), MDB BIAS HI = S(O-1), L, ZERØ

OPERATIONAL DESCRIPTION

Parentheses were removed from the input pin names in order to make the equations easier to read.

Output K (LO) = MO • M2 • N

Output O (HI) = $(MO \bullet MI \bullet M2 \bullet N \bullet H1 \bullet H2)+(M2 \bullet N \bullet H3 \bullet J0 \bullet J1) \bullet (J2+B2)$

Gating modifier Gl in the symbol in the lower right corner will be active when output O is H. OR modifier V is active when input pin B(1) is LO.

Outputs C(0-1) are two copies of the same signal and will be LO when the following equation is active: $(D \bullet G1)+V$.

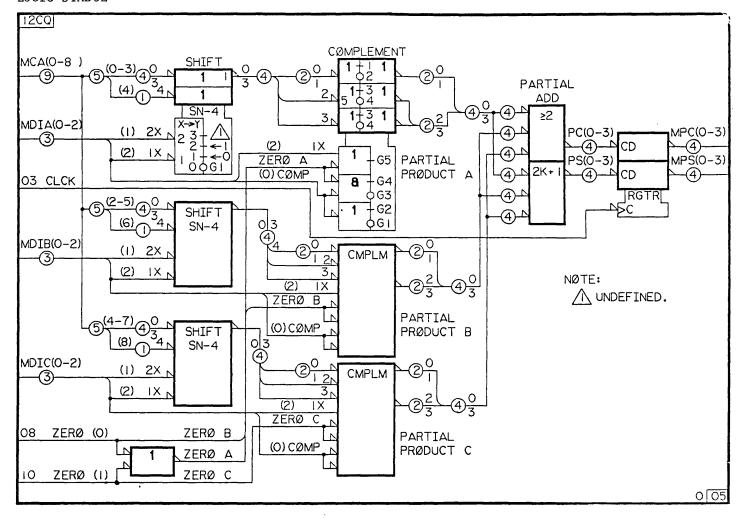
Outputs C(2-3) are two copies of the same signal and will be LO when the following equation is active: (AC \bullet G1)+V.

Outputs C(4-7) are two copies of the same signal and will be LO wher the following equation is active: (MDA \bullet G1)+V.

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12CQ

C SINI C	2541) 41 D.T.
PIN NAME	REAL PIN	VIRT PIN
CLCK	03	V25
CLFC	04 47	V26 V48
FNO	30	V47
MCA(0)	49	V16
MCA(1) MCA(2)	18 07	V17 V18
MCA(3)	16	V19
MCA(4)	52	V20
MCA(5) MCA(6)	44 09	V21 V22
MCA(7)	06	V23
MCA(8)	05	V24
MDIA(0) MDIA(1)	38 17	V07 V08
MDIA(2)	34	V09
MDIB(0)	43	V10
MDIB(1) MDIB(2)	36 42	V11 V12
MDIC(0)	12	V13
MDIC(1)	11	V14
MDIC(2) MPL(0)	15 41	V15 V04
MPL(1)	48	V05
MPL(2)	45	V06
ONECMP	46 37	V01 V02
SNMPL	35	V03
ZERO(0) ZERO(1)	08 10	V27 V28
DO0(0)	32	V28 V31
DO0(0)	27	V34
DO0(2)	19	V37
DO1(0)	33 29	V32 V35
DO1(1)	23	V38
MPC(0)	22	V39
MPC(1) MPC(2)	21 01	V41 V43
MPC(3)	51	V45
MPS(0)	20	V40
MPS(1) MPS(2)	26 02	V42 V44
MPS(3)	50	V46
NDO(0)	31	V30
NDO(1) NDO(2)	25 24	V33 V36
TWOCOR	28	V29



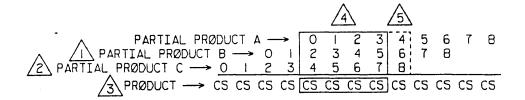
TYPE O MAY BE USED WITH ANY OF THE OTHER 12CQ USES BECAUSE THEIR BIAS DOES NOT AFFECT THIS USE.

BIAS LØ = CLFC

BIAS HI = NONE

OPERATIONAL DESCRIPTION

Each 12CQ-0 begins the formation of three partial products by first performing wired shifts of the multiplicand to adjust each partial product according to the significance of the multiplier codes. The 12CQ-0 then completes the formation of each partial product by performing a shift and complement under the control of the multiplier codes. This process is the multiply. The 12CQ-0 then forms the product by performing a partial add of the three partial products and clocking the resulting partial sums and partial carries into an output register. The following figure shows a small portion of the three partial products, the product, and the portion of the operation handled by one 12CQ-0 array.



νØΤES: Λ

ALIGNED VIA AN ØN-CHIP WIRED LEFT SHIFT ØF TWØ.



ALIGNED VIA AN ØN-CHIP WIRED LEFT SHIFT ØF FØUR.



THE I2CO-O ADDS THE THREE PARTIAL PRODUCTS TOGETHER AND PRODUCES A PARTIAL CARRY AND PARTIAL SUM BIT FOR EACH COLUMN.



SØLID ØUTLINE SHØWS THE PØRTIØN ØF THE THREE PARTIAL PRØDUCTS AND PRØDUCT HANDLED BY ØNE 12CQ-O ARRAY.



DASHED ØUTLINE SHØWS BITS WHICH ALSØ MUST ENTER EACH PARTIAL PRØDUCT BECAUSE ØF THE PØSSIBILITY ØF A MULTIPY ØF 2X (LEFT SHIFT ØF ØNE) WHICH TAKES PLACE IN THE SHIFT FUNCTIØN FØR EACH PARTIAL PRØDUCT.

Inputs

The multiplicand enters on pins MCA(0-8). Bits 0-4 go straight to the shift function for Partial Product A. Bits 2-6 are left-shifted by two and enter the shift function for Partial Product B. Bits 4-7 are left-shifted by four and enter the shift function for Partial Product C.

The multiplier codes for Partial Products A, B, and C enter MDIA(0-2), MDIB(0-2), and MDIC(0-2), respectively. The Shift and Complement paragraphs describe their use.

The ZERO (0-1) inputs enable the complement control for the two least-significant bits in each partial product, and gate partial product bit 2 into the complement function for each partial product. The Complement paragraph describes this control.

Outputs

MPC(0-3) outputs are product partial carries.

MPS(0-3) outputs are product partial sums.

Shift Function

There are three shift functions, one for each partial product. Separate multiply codes control each shift function. The multiply code which enters MDIB(0-2) is two bits more significant than the code which enters MDIA(0-2). The multiply code which enters MDIC(0-2) is four bits more significant than MDIA(0-2).

12CQ-0 (Cont'd)

The top shift function, for Partial Product A, is the only one with detailed symbology because the lower two operate in the same manner. This description will deal only with Partial Product A for the same reason.

Multiplier code bits 1 and 2 enter the shift function common control block where they are translated.

A translation of 0 makes gating modifier Gl inactive which blocks the shift function output. Gl is active for all other translations.

A translation of 1 causes a shift of 0. Shift function input bits 0-3 go straight to output bits 0-3. Input bit 4 is discarded.

A translation of 2 causes an end-off left (up) shift of 1-bit position. Shift function input bits 1-4 shift up to output bits 0-3. Input bit 0 is discarded.

A translation of 3 causes undefined results.

Complement Function

There are three complement functions, one for each partial product. Separate multiply codes and zero controls feed each complement function.

The top complement function, for Partial Product A, is the only one with detailed symbology because the lower two operate in the same manner. This description will deal only with Partial Product A for the same reason.

Data bits 0 and 1 enter the complement function in highwayed form. Gating modifier Gl selects true data and G2 selects complemented data. Data bits 2 and 3 enter the complement function separately. G5 gates in bit 2 and G3 and G4 select true or complement data.

Complement Control

- G5 is active when 1X is HI OR ZERO A is LO.
- G4 is active when ZERO A AND COMP are both LO.
- G3 is active when either ZERO A OR COMP is HI.
- G2 is active when COMP is LO.
- Gl is active when COMP is HI.

Partial Add

The partial add consists of two functions, one for partial carries (top) and one for partial sums (bottom).

A partial carry bit will be active (LO) when two or more corresponding inputs are active (LO). For example, PC(O) will be LO when two or more partial product bit zeros are LO.

12CQ-0 (Cont'd)

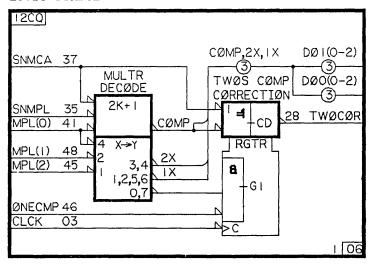
A partial sum bit will be active (LO) when an odd number of corresponding inputs are active (LO). For example, PS(0) will be LO when an odd number of partial product bits zeros are LO.

Output Register

Clock enters the 12CQ-O on pin CLCK and clocks the partial carries and partial sums into the output register.

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THIS BIAS HAS NØ AFFECT ØN THE TYPE O USE (MULTIPLY).

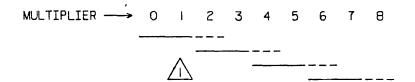
BIAS LØ = FNØ, FANEN, CLFC

BIAS HI = NØNE

TERMINATE = NDO(0-2)

OPERATIONAL DESCRIPTION

Each 12CQ-1 array receives three bits of multiplier and produces a multiplier code which represents the two most-significant bits of the 3-bit group. The figure below shows a small portion of the multiplier and the bits handled by each 12CQ-1 array.



NØTE: THE SØLID UNDERLINES INDICATE THE TWØ MØST SIGNIFICANT BITS HANDLED BY EACH 12CQ-1 AND THE DASHED UNDERLINES SHØW THE ØNE-BIT ØVERLAP.

12CQ-1 (Cont'd)

The multiplier code consists of three signals: COMP, 2X, and 1X. Two copies of the 3-bit code leave the array, one copy on pins D01(0-2) and the other on pins D00(0-2). The Multiplier Decode paragraph describes the Decode function.

The 12CQ-1 also produces a two's complement correction signal and clocks it into a register. The Two's Complement Correction paragraph describes this signal.

Multiplier Decode

Three bits of the multiplier enter the array on pins MPL(0-2). The multiplicand sign enters on pin SNMCA and the multiplier sign enters on pin SNMPL.

COMP=SNMCA+SNMPL+MPL(0)

The 2X and 1X signals are the result of a translation of the 3 multiplier bits. Translations of 3 or 4 will make the 2X signal active (LO). Translations of 1, 2, 5, or 6 will make the 1X signal active (LO). Translations of 0 or 7 will make an output LO which will disable an AND gate in the common control block of the Two's Complement Correction function.

Two's Complement Correction

The equation for the two's complement correction signal is:

COMP (+) (ONECMP • Multiplier Decodes of 0 or 7 • SNMCA)

Clock enters the array on pin CLCK and clocks this signal into a register. The two's complement correction signal leaves the array on pin TWOCOR.

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1200					
FNØ	30 N			32	DØ0(0)
		1	-	33	DØ1(0)
Ì	1		-¦[31	NDØ(O)
Ī	- 1		' [27	DØ0(1)
j	1			29	DØ1(1)
				25	NDØ(I)
	i		2	19	DØ0(2)
MPL(0)	41 NGI		2	23	DØ1(2)
MPL(2)	45 G2		2	24	NDØ(2)
	-02				
					2 05

THIS BIAS HAS NØ AFFECT ØN THE TYPE O USE (MULTIPLY).

BIAS LØ = ØNECMP

BIAS HI = MPL(I), SNMPL, SNMCA, FANEN

ALSØ, IF REMAINDER ØF ARRAY IS NØT USED AS TYPE O

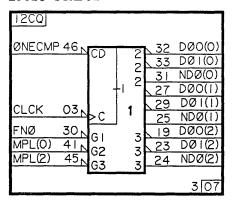
(MULTIPLY), BIAS CLFC = HI AND CLCK = LØ

TERMINATE = TWØCØR. ALSØ, TERMINATE NDØ(O-2) IF NØT USED.

OPERATIONAL DESCRIPTION

Input pin FNO controls an OR function which has six active LO outputs and three active HI outputs. Input pin MPL(0) controls gating modifier Gl which gates the top three outputs. Input pin MPL(2) controls G2 which gates the lower three outputs. The three outputs in the center are not gated.

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THIS BIAS HAS NO AFFECT ON THE TYPE O USE (MULTIPLY).

BIAS LØ = CLFC

BIAS HI = MPL(I), SNMPL, SNMCA, FANEN

TERMINATE = TWØCØR. ALSØ, TERMINATE NDØ(O-2) IF NØT USED.

OPERATIONAL DESCRIPTION

Clock entering the 12CQ-3 on pin CLCK, clocks data (pin ONECMP) into a latch. Pin FNO controls gating modifier Gl which gates the output of the latch into the OR function.

The OR function has six active LO outputs and three active HI outputs. Input pin MPL(0) controls G2 which gates the top three outputs. Input pin MPL(2) controls G3 which gates the lower three outputs. The three outputs in the center are not gated.

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12CQ-4 Exclusive OR.

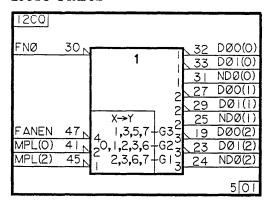
LOGIC SYMBOL

12CQ				
SNMCA	37 _N		32	DØ0(0)
		=1	33	DØ1(0)
SNMPL	35 _N		31	NDØ(O)
MPL(I)	48		19	DØ0(2)
		=1	23	DØ I(2)
MPL(2)	45 _N		24	NDØ(2)
			1	
				4 04

THIS BIAS HAS NØ EFFECT ØN
THE TYPE O USE (MULTIPLY),
BIAS LØ = FANEN, FNØ
BIAS HI = ØNECMP, MPL(O)
ALSØ, IF REMAINDER ØF ARRAY IS NØT USED AS TYPE O
(MULTIPLY), BIAS CLFC = HI AND CLCK = LØ

OPERATIONAL DESCRIPTION

(None required.)



BIAS LØ = ØNECMP BIAS HI = MPL(I), SNMPL, SNMCA ALSØ, IF REMAINDER ØF ARRAY IS NØT USED AS TYPE O (MULTIPLY), BIAS CLFC = HI AND CLCK = LØ TERMINATE = TWØCØR. ALSØ, TERMINATE NDØ(O-2) IF NØT USED.

OPERATIONAL DESCRIPTION

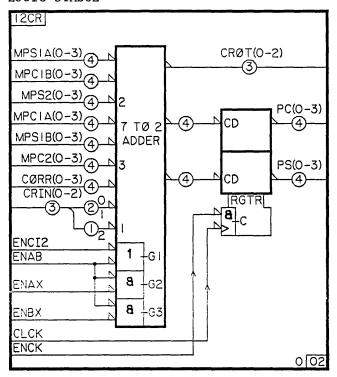
Input FNO controls an OR function which has six active LO outputs and three active HI outputs. Gating modifiers G1, G2 and G3 gate these outputs to the output pins. Translations of input pins FANEN, MPL(0), and MPL(2) control the gating modifiers.

Translations of 1, 3, 5, or 7 activate G3. Translation of 0, 1, 2, 3, or 6 activate G2. Translations of 2, 3, 6, or 7 activate G1. A translation of 4 does not activate any gating modifier and therefore all outputs are inactive.

12CR

PIÑ NAME	REAL PIN	VIRT PIN
CLCK CORR(0) CORR(1) CORR(2)	08	V33 V07 V14 V21
CORR(3) CRIN(0) CRIN(1) CRIN(2)	11 45	V29 V22 V30 V31
ENAB ENAX ENBX ENCI2	41 35 38 46	V32 V46 V47 V48
ENCK MPC1A(0) MPC1A(1) MPC1A(2)	26	V34 V04 V11 V18
MPC1A(3) MPC1B(0) MPC1B(1) MPC1B(2)	18 22	V26 V02 V09 V16
MPC1B(3) MPC2(0) MPC2(1) MPC2(2)	09	V24 V06 V13 V20
MPC2(3) MPS1A(0) MPS1A(1) MPS1A(2)	42 17 24	V28 V01 V08 V15
MPS1A(3) MPS1B(0) MPS1B(1) MPS1B(2)	19	V23 V05 V12 V19
MPS1B(3) MPS2(0) MPS2(1) MPS2(2)	36 16 12 15	V27 V03 V10 V17
MPS2(3)	37	V25
CROT(0) CROT(1) CROT(2)	21 05 04	V35 V36 V39
PC(0) PC(1) PC(2) PC(3)	02 51 49 47	V37 V40 V42 V44
PS(0) PS(1) PS(2) PS(3)	01 29 50 31	V38 V41 V43 V45

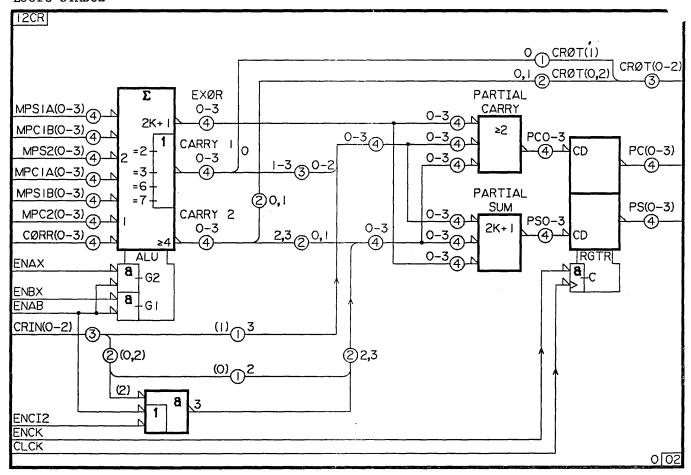
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BIAS NØNE

OPERATIONAL DESCRIPTION

The block diagram is used to save space on the logic diagrams. Refer to the ANSI symbol and its description.



BIAS NONE

OPERATIONAL DESCRIPTION

The 12CR-0 adds seven four-bit operands and produces a partial carry and partial sum bit for each bit position. It then clocks these results into an output register.

Add

The 12CR-0 performs the add with three functions: ALU, Partial Carry and Partial Sum.

ALU Function

The ALU function receives seven four-bit operands and produces three four-bit output highways, EXOR, Carry 1 and Carry 2.

Gating modifier Gl gates in the MPC2(0-3) operand, G2 gates in the MPS2(0-3) operand. Gl is active when both ENBX and ENAB are active. G2 is active when both ENAX and ENAB are active.

Bit N of the EXOR highway will be active (LO) when there are an odd number of active (LO) bit N inputs among the seven operands. The EXOR highway connects to both the Partial Carry and Partial Sum functions.

Bit N of the Carry 1 highway will be active (LO) when there are 2, 3, 6, or 7 active (LO) bit Ns among the seven operands. The Carry 1 highway connects to the Partial Carry and Partial Sum functions with an on-chip wired left shift of 1-bit position. Carry 1 bit 0 leaves the array on output pin CROT(1). Bit 0 from the ALU connects to the next higher-order array where it will become Carry 1 bit 3. Bits 1-3 from the ALU are left-shifted to bit positions 0-2 and a new bit 3 enters on input pin CRIN(1). This is Carry 1 bit 0 from the ALU on the next lower-order array.

Bit N of the Carry 2 highway will be active (LO) when there are 4 or more active (LO) bit Ns among the seven operands. The Carry 2 highway connects to the Partial Carry and Partial Sum functions with an on-chip wired left shift of 2-bit positions. Carry 2 bits 0 and 1 leave the array on output pins CROT(0,2), respectively. Bits 0 and 1 connect to the next higher-order array where they will become Carry 2 bits 2 and 3. Bits 2 and 3 are left-shifted to bit positions 0 and 1 and new bits 2 and 3 enter on pins CRIN(0-2), respectively. These are Carry 2 bits 0 and 1 from the next lower-order array. CRIN(2) is gated in by either ENAB LO or ENCI2 LO.

Partial Carry

The Partial Carry function receives the three four-bit input highways described in the ALU Function paragraph and produces Partial Carry bits 0-3.

Partial Carry bit N is active (LO) when there are two or more active (LO) bit N inputs among the three highways entering the Partial Carry function.

Partial Sum

The Partial Sum function receives the three four-bit input highways described in the ALU Function paragraph and produces Partial Sum bits 0-3.

Partial Sum bit N will be active (LO) when there are an odd number of active (LO) bit N inputs among the three highways entering the Partial Sum function.

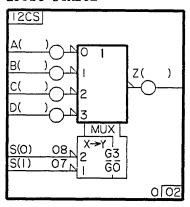
Output Register

Pins ENCK and CLCK are ANDed to latch the partial carry and partial sum bits into the output register. Outputs PC(0-3) are the partial carry bits and PS(0-3) are the partial sum bits.

60458120 B 3 of 3

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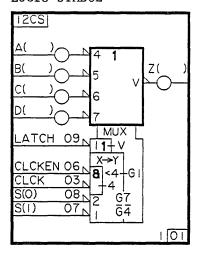
PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	34	V01
A(1)	36	V02
A(2)	37	V03
A(3)	42	V04
A(4)	20	V05
A(5)	18	V06
A(6)	21	V07
A(7)	12	V08
B(0)	35	V09
B(1)	33	V10
B(2)	38	V11
B(3)	41	V12
B(4)	17	V13
B(5)	15	V14
B(6)	24	V15
B(7)	11	V16
C(0)	32	V17
C(1)	31	V18
C(2)	44	V19
C(3)	45	V20
C(4)	27	V21
C(5)	25	V22
C(6)	19	V23
C(7) CLCK CLCKEN D(0)	10 03 06 48 47	V24 V38 V36 V25 V26
D(1) D(2) D(3) D(4) D(5)	46 43 23 16	V27 V28 V29 V30
D(6) D(7) LATCH S(0)	22 02 09 08	V30 V31 V32 V37 V33
S(1)	07	V34
S(2)	52	V35
P	51	V48
Z(0)	30	V39
Z(1)	49	V40
Z(2)	29	V41
Z(3)	50	V42
Z(4)	28	V43
Z(5)	04	V44
Z(6)	26	V45
Z(7)	05	V46
Z(8)	01	V47



BIAS LØ = CLCKEN, CLCK BIAS HI = S(2), LATCH

OPERATIONAL DESCRIPTION

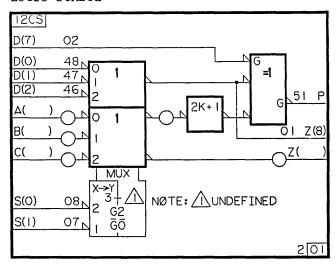
Pins S(0) and S(1) select one of four input highways to output highway Z.



BIAS LØ = NØNEBIAS HI = S(2)

OPERATIONAL DESCRIPTION

Pins S(0) and S(1) select one of four input highways. Pins CLCK and CLCKEN are ANDed to enable the selected data in the mux. The inputs to the mux will not be enabled if the control translation is less than 4. If the translation is less than 4, Gl is active. Gl gates the LATCH input allowing it to enter V. If V is active the output of Z is forced LO. If V is inactive it has no effect on the Z outputs.



TØ USE AS A PARITY CHECK NETWØRK PINS D(O-2) ARE THE PARITY BITS FØR THE A, B, AND C TRUNKS RESPECTIVELY, TØ USE AS A PARITY GENERATØR CØNNECT PINS D(O-2) TØ BIAS HI.

BIAS LØ = CLCKEN, CLCK BIAS HI = S(2), LATCH

OPERATIONAL DESCRIPTION

Input Select Control

Pins S(0) and S(1) select one of three input highways and one of three individual input pins through a pair of muxes when the select code equals 0, 1, or 2. The outputs of the muxes are undefined when the select code equals 3.

Parity Check

When the 12CS-2 is used for parity checking, input pins D(0), D(1), and D(2) receive the parity bits for input highways A, B, and C respectively. The =1 and 2K+1 functions work together to perform an odd parity check. The 2K+1 performs an odd parity check on the selected data and the result is exclusive ORed with the selected parity bit. Pin D(7) gates the result to output pin P. Output pin P will be LO when pin D(7) is LO and there is odd parity.

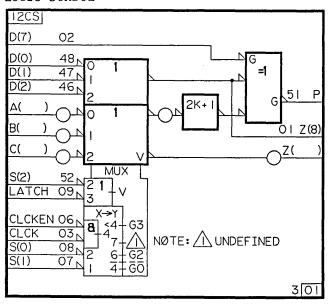
Parity Generate

When the 12CS-2 is used for parity generation, input pins D(0), D(1), and D(2) are all biased HI. The =1 and 2K+1 functions work together to generate the parity bit for an even parity. The 2K+1 performs an odd parity check on the selected data and the result is exclusive ORed with the HI from the upper mux. Pin D(7) gates the result to output pin P. Output pin P is the new parity bit for the selected data.

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12CS-3 Three-Input Multiplexer with Parity Checking or Parity Generation on the Output of the Registers.

LOGIC SYMBOL



TØ USE AS A PARITY CHECK NETWØRK PINES D(O-2) ARE THE PARITY BITS FØR THE A, B, AND C TRUNKS RESPECTIVELY. TØ USE AS A PARITY GENERATØR CØNNECT PINS D(O-2) TØ BIAS HI.

BIAS NØNE

OPERATIONAL DESCRIPTION

Input Register Control

Pins S(0) and S(1) select one of three input highways and one of three individual input pins to a pair of muxes. Pins CLCK and CLCKEN are ANDed to enable the selected data in the mux. Note that a translation of 4-6 produce gating modifiers G0-2 which control the muxes and a translation of 7 produces undefined outputs. Translations of less than 4 will make G3 active (refer to Sign Extension).

Sign Extension

When the control translation is less than 4, G3 is active and G0-2 are inactive. G3 gates LATCH to control the OR modifier V, and the absence of G0-2 block all inputs to the muxes. When LATCH is LO, V is active and forces the Z outputs LO. When LATCH is HI, V is inactive and the Z outputs contain zeros (caused by the blocked mux inputs).

When the control translation is 6, G2 is active and gates the C highway and D(2) into the muxes and also gates pin S(2) in to control V. When S(2) is LO, V is active and the Z outputs are forced LO. When S(2) is HI, V is inactive and the contents of the C highway pass unaltered to the Z outputs.

12CS-3 (Cont'd)

Parity Check

When the 12CS-3 is used for parity checking, input pins D(0), D(1), and D(2) receive the parity bits for input highways A, B, and C respectively. The =1 and 2K+1 functions work together to perform an odd parity check. The 2K+1 perform an odd parity check on the selected data and the result is exclusive ORed with the selected parity bit. Pin D(7) gates the result to output P. Output P will be LO when pin D(7) is LO and there is odd parity.

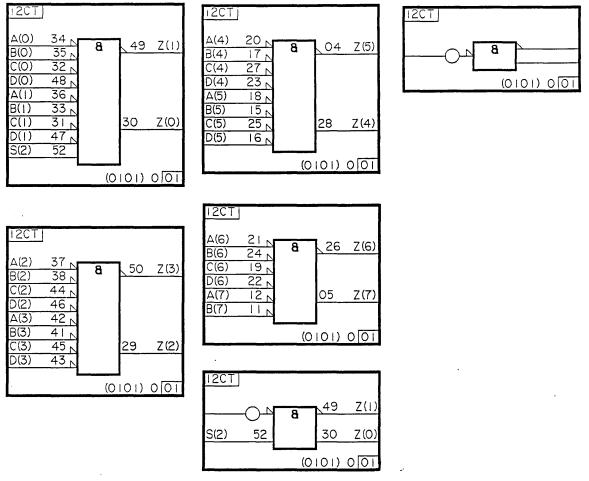
Parity Generate

When the 12CS-3 is used for parity generation, input pins D(0), D(1), and D(2) are all biased HI. The =1 and 2K+1 functions work together to generate the parity bit for an even parity. The 2K+1 performs an odd parity check on the contents of the lower register and the result is exclusive ORed with the HI from the upper register. Pin D(7) gates the result to output pin P. Output pin P is the new parity bit for the selected data.

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12CT

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	34	V01
A(1)	36	V02
A(2)	37	V03
A(3)	42	V04
A(4)	20	V05
A(5)	18	V06
A(6)	21	V07
A(7)	12	V08
B(0)	35	V09
B(1)	33	V10
B(2)	38	V11
B(3)	41	V12
B(4)	17	V13
B(5)	15	V14
B(6)	24	V15
B(7)	11	V16
C(0)	32	V17
C(1)	31	V18
C(2)	44	V19
C(3)	45	V20
C(4)	27	V21
C(5)	25	V22
C(6)	19	V23
C(7)	10	V24
CLCKEN	06	V36
D(0)	48	V25
D(1)	47	V26
D(2)	46	V27
D(3)	43	V28
D(4)	23	V29
D(5)	16	V30
D(6)	22	V31
D(7)	02	V32
LATCH	09	V37
S(0)	08	V33
S(1)	07	V34
S(2)	52	V35
CLCK	03	V38
P	51	V48
Z(0)	30	V39
Z(1)	49	V40
Z(2)	29	V41
Z(3)	50	V42
Z(4)	28	V43
Z(5)	04	V44
Z(6)	26	V45
Z(7)	05	V46
Z(8)	01	V47

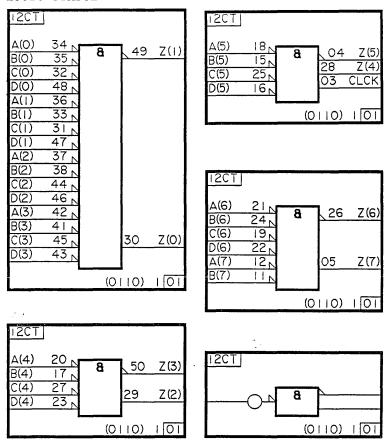


BIAS LØ = S(1), D(7)BIAS HI = S(0), C(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (0101) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

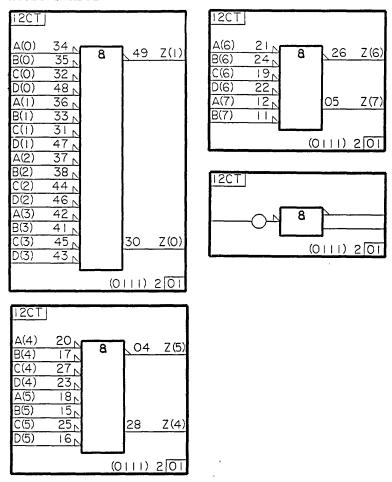


BIAS $L\emptyset = S(1)$, C(7)BIAS HI = S(0), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The 0110 in the bottom of each box is for designer reference. It denotes the biased states of pins S(0), S(1), C(7), and D(7) respectively.

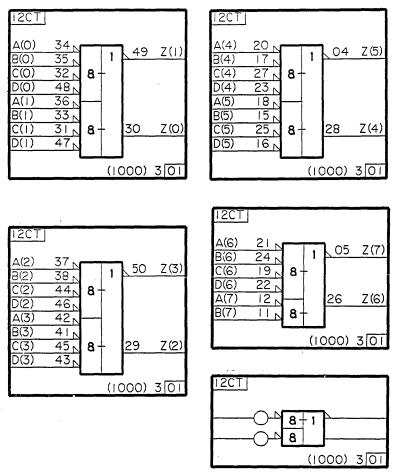


BIAS LØ = S(1), C(7), D(7)BIAS HI = S(0)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (0111) In the bottom of each box is for designer reference. It denotes the biased states of pins S(0), S(1), C(7) and D(7) respectively.

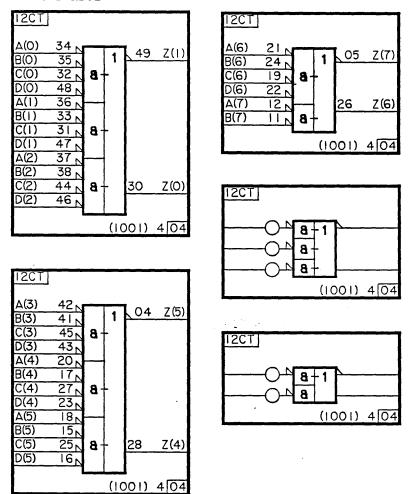


BIAS $L\emptyset = S(0)$ BIAS HI = S(1), C(7), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1000) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

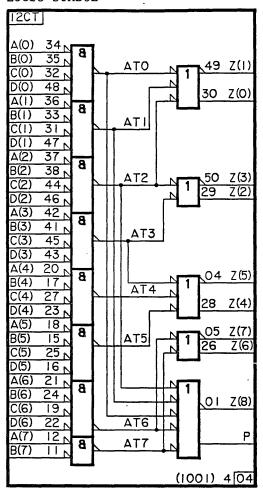


BIAS LØ = S(O), D(7) BIAS HI = S(I), C(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1001) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

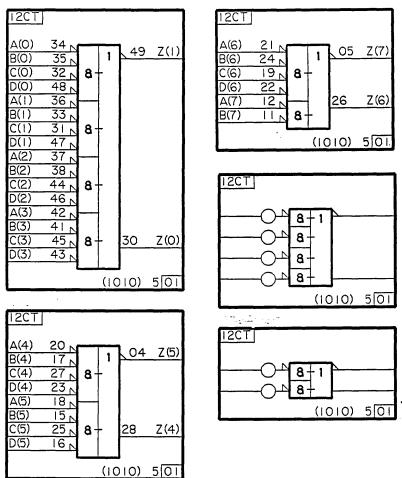


BIAS LØ = S(O), D(7) BIAS HI = S(I), C(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1001) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

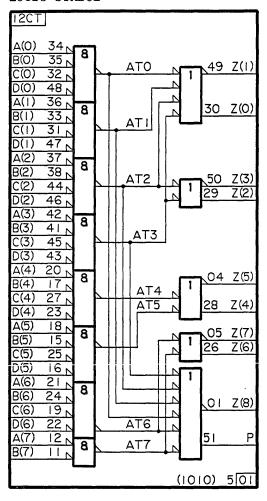


BIAS LØ = S(O), C(7)BIAS HI = S(I), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1010) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

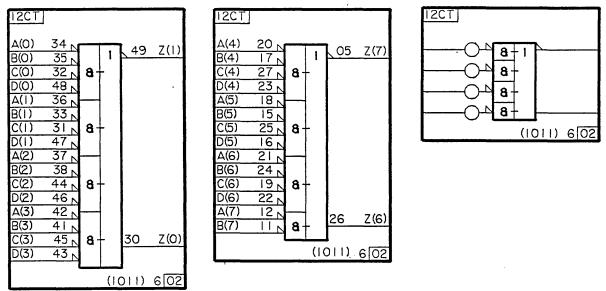


BIAS LØ = S(O), C(7) BIAS HI = S(I), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1010) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

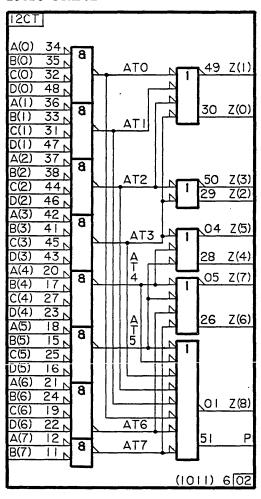


BIAS LØ = S(O), C(7), D(7) BIAS HI = S(I)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1011) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

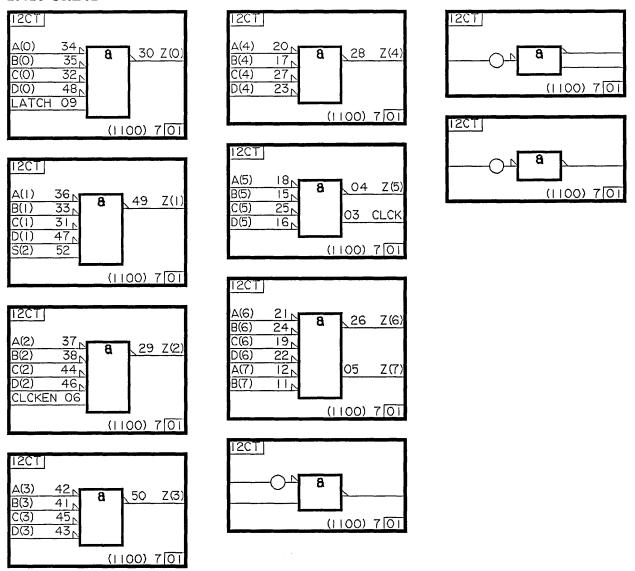


BIAS LØ = S (O), C(7), D(7) BIAS HI = S(1)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1011) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

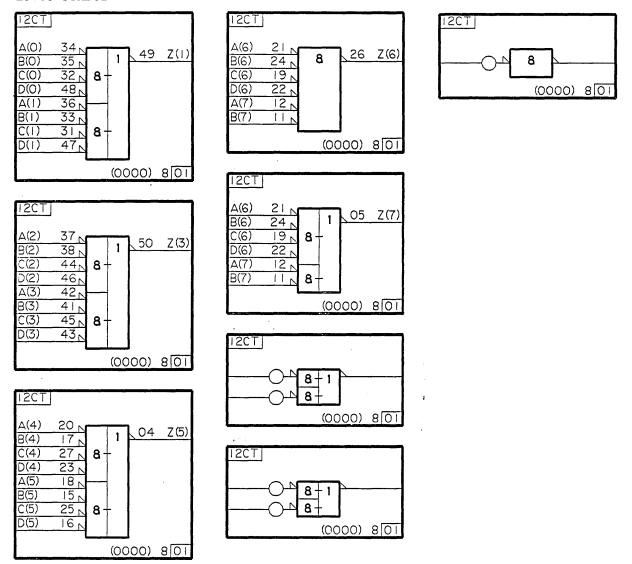


BIAS LØ = S(0.1)BIAS HI = C(7), D(7)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1100) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.

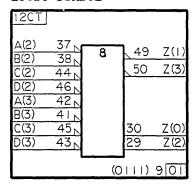


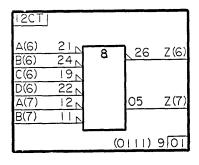
BIAS LØ = NØNE BIAS HI = S(O, I), C(7), D(7)

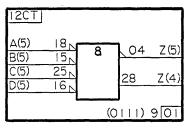
OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (1100) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.







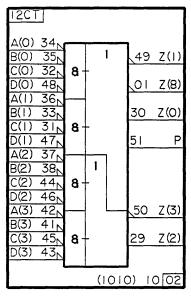
BIAS HI = S(O)

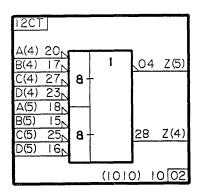
BIAS LØ = S(1), C(7), D(7), A(0), B(0), C(0), D(0), A(1), B(1), C(1), D(1), A(4), B(4), C(4), D(4)

OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

The (0111) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7) respectively.



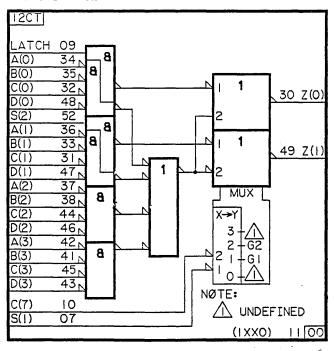


BIAS $L\emptyset = S(0)$, C(7)BIAS HI = A(6-7), S(1), D(7)

OPERATIONAL DESCRIPTION

Output pin Z(1) is the OR of all four AND gates. Output pin Z(3) is the OR of the lower 2 AND gates.

The (1010) in the bottom of each box is for designer reference. It denotes the biased state of pins S(0), S(1), C(7), and D(7).



BIAS LØ = S(O) BIAS HI = D(7)

OPERATIONAL DESCRIPTION

Input pins C(7) and S(1) are translated to select AND gates or AND/OR gates.

Translations of 0 and 3 produce undefined results.

A translation of 1 gates an AND of A(0), B(0), C(0), D(0), and LATCH to output pin Z(0). This translation also gates an AND of A(1), B(1), C(1), D(1), and S(2) to output pin Z(1).

A translation of 2 gates the OR of four four-input AND gates to output pin Z(1) and the complement of that same logic to output pin Z(0).

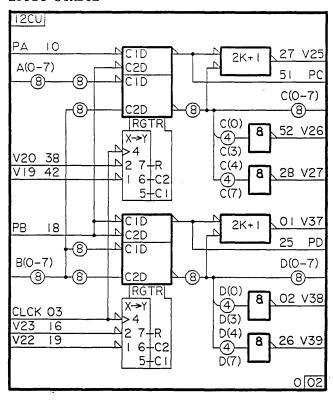
The (1XX0) in the bottom of the box is for designer reference. It denotes the biased states of pins S(0), S(1), C(7), and D(7) respectively. Note in this case however, that pins S(1) and C(7) are not biased and are shown as Xs.

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12CU

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	45	V03
A(1)	46	V05
A(2) A(3)	44	V07 V09
A(3)	43 34	V09 V11
A(5)	33	V13
A(6)	35	V15
A(7)	36	V17
B(0)	12	V04
B(1)	08	V06
B(2)	41	V08
B(3)	09	V10
B(4)	17	V12
B(5)	15	V14
B(6)	20	V16
B(7)	37	V18
CLCK	03	V 16
PA	10	V01
PB	18	V02
V19	42 38	V19
V20 V21	11	V20 V21
V22	19	V22
V23	16	V23
C(0)	49	V29
C(1)	50	V30
C(2)	47	V31
C(3)	48	V32
C(4)	29	V33
C(5)	30	V34
C(6)	31	V35
C(7)	32	V36
D(0)	07	V41
D(1)	06 05	V41 V42 V43
D(2) D(3)	04	V43 V44
D(4)	22	V45
D(5)	21	V46
D(6)	24	V47
D(7)	23	V48
PC	51	V28
PD	25	V40
V25 V26	27	V25 V26
V26 V27	52 28	V27
V37	01	V37
V38	02	V38
V39	26	V39

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BIAS LØ = V21 BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Upper Register

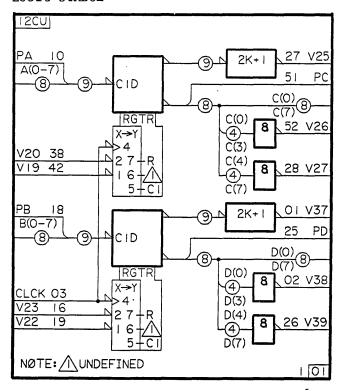
Input pins V19, V20, and CLCK control the upper register. A control translation of 5 clocks inputs A(0-7) and PA, 6 clocks inputs B(0-7) (active HI) and PB (active L0), and 7 clears the register.

Output pin V25 is active (LO) when an odd number of parity checker inputs are active. Output pins V26 and V27 are active (LO) when input pins C(0-3) and C(4-7) are active (HI), respectively.

Lower Register

Input pins V22, V23, and CLCK control the lower register. A control translation of 5 clocks inputs B(0-7) and PB, 6 clocks input B(0-7) (active HI) and PB(active LO), and 7 clears the register.

Output pin V37 is active (LO) when an odd number of parity checker inputs are active. Output pins V38 and V39 are active (LO) when input pins D(0-3) and D(4-7) are active (HI), respectively.



BIAS LØ = V21 BIAS HI = NØNE

OPERATIONAL DESCRIPTION

Upper Register

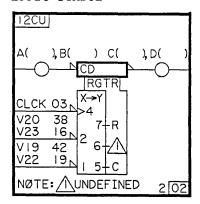
Input pins V19, V20, and CLCK control the upper register. A control translation of 5 clocks inputs A(0-7) and PA, 6 is undefined, and 7 clears the register.

Output pin V25 is active (LO) when an odd number of parity checker inputs are active. Output pins V26 and V27 are active (LO) when input pins C(0-3) and C(4-7) are active (HI), respectively.

Lower Register

Input pins V22, V23 and CLCK control the lower register. A control translation of 5 clocks inputs B(0-7) and PB, 6 is undefined and 7 clears the register.

Output pin V37 is active (LO) when an odd number of parity checker inputs are active. Output pins V38 and V39 are active (LO) when input pins D(0-3) and D(4-7) are active (HI), respectively.



INPUT PINS ARE: A(0-7), B(0-7) ØUTPUT PINS ARE: C(0-7), D(0-7)

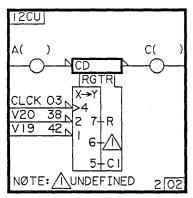
BIAS LØ = V21, PA, PB BIAS HI = NØNE TERMINATE = V26, V27, V38, V39

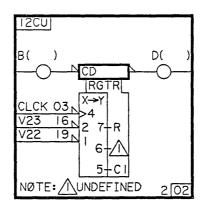
OPERATIONAL DESCRIPTION

Input pins V19 and V22 (tied together), V20 and V23 (tied together), and CLCK control the register. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.

12CU-2 8-Bit Registers.

LOGIC SYMBOL

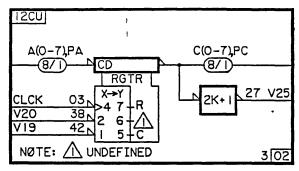


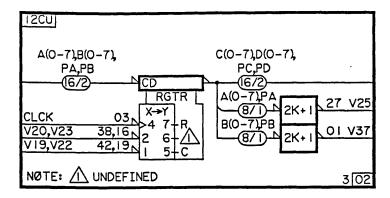


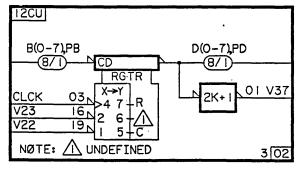
BIAS LØ = V21, PA, PB BIAS HI = NØNE TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Input pins V19, V20, and CLCK or V22, V23 and CLCK control their respective registers. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.







BIAS LØ = V21 BIAS HI = NØNE

TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Two 8-Bit Registers with Parity

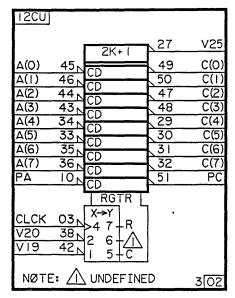
Input pins V19, V20, and CLCK or V22, V23 and CLCK control their respective registers. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.

Output pins V25 and V37 are active (LO) when an odd number of parity checker inputs are active.

16-Bit Register with Parity

Input pins V19 and V22 (tied together), V20 and V23 (tied together), and CLCK control the register. A control translation of 5 clocks inputs A(0-7), B(0-7), PA, and PB, 6 is undefined, and 7 clears the register.

Output pins V25 and V37 are active (LO) when an odd number of parity checker inputs A(0-7) and PA, or B(0-7) and PB are active, respectively.



12CU				
Ì		2K+ I	01	V37
B(O)	12 _N	CD	07	D(O)
B(1)	087	CD	06	D(1)
B(2)	41	CD	05	D(2)
B(3)	09	CD	04	D(3)
B(4)	17 _N	CD	22	D(4)
B(5)	15	CD	21	D(5)
B(6)	20 _N	CD	24	D(6)
B(7)	37 _N	CD	23	D(7)
PB	18 N	CD	25	PD
CLCK V23 V22	03 _N 16 _N	RGTR X-Y >4 7 - R 2 6 - 1 5 - C		
NØTE	: 🛆	UNDEFINE	.D	302

BIAS LØ = V21 BIAS HI = NØNE

TERMINATE = V26, V27, V38, V39

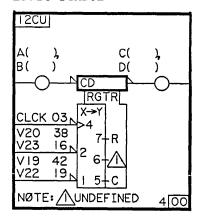
OPERATIONAL DESCRIPTION

Input pins V19, V20, and CLCK or V22, V23, and CLCK control their respective registers. A control translation of 5 clocks input data A(0-7), PA, and B(0-7), PB, 6 is undefined, and 7 clears the register.

The 12CU-3 divides into two areas; the common control block and the common output block.

The common control block (above the double line) contains the odd parity checker. The common output block monitors the outputs of the register.

Output pins V25 and V37 are active (LO) when an odd number of parity checker inputs are active.

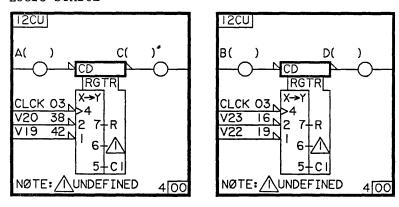


- I. INPUT PINS ARE: A(0-7, PA, B(0-7), PB ØUTPUT PINS ARE: C(0-7), PC, D(0-7), PD
- 2. USE ØF PA AND PB FØR DATA MAY VIØLATE LØAD BALANCING RULE.

BIAS LØ = V2| BIAS HI = NØNE TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Input pins V19 and V22 (tied together), V20 and V23 (tied together), and CLCK control the register. A control translation of 5 clocks the input data, 6 is undefined and 7 clears the register.

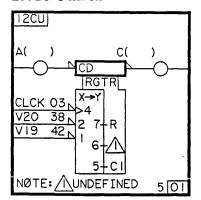


- I. INPUT PINS ARE: A(0-7), PA, B(0-7), PB OUTPUT PINS ARE: C(0-7), PC, D(0-7), PD
- 2. USE ØF PA AND PB FØR DATA MAY VIØLATE LØAD BALANCING RULE.

BIAS LØ = V21 BIAS HI = NØNE TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Input pins V19, V20, and CLCK or V22, V23, and CLCK control their respective registers. A control translation of 5 clocks the input data, 6 is undefined, and 7 clears the register.



Note:

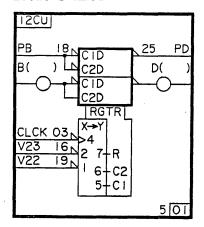
1. INPUT PINS ARE: A(0-7), PA OUTPUT PINS ARE: C(0-7), PC

BIAS LØ = V21 BIAS HI = NØNE TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Input pins V19, V20, and CLCK control the register. A control translation of 5 clocks the A input data, 6 is undefined, and 7 clears the register.

60458120 B

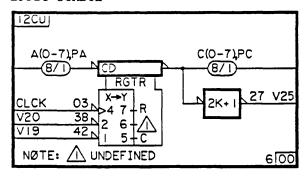


Note:

1. INPUT PINS ARE: B(0-7), PB
OUTPUT PINS ARE: D(0-7), PD

OPERATIONAL DESCRIPTION

Inputs pins V22, V23, and CLCK control the register. A control translation of 5 clocks the B and PB inputs (all active LO), 6 clocks the B inputs (active HI) and PB (active LO), and 7 clears the register.



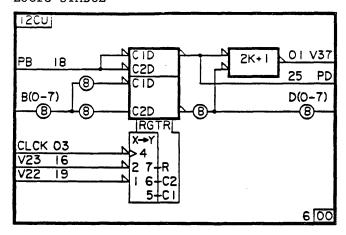
BIAS LØ = V21 BIAS HI = NØNE

TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Input pins V19, V20, and CLCK control the register. A control translation of 5 clocks inputs A(0-7) and PA, 6 is undefined, and 7 clears the register.

Output pin V25 is active (LO) when an odd number of parity checker inputs are active.



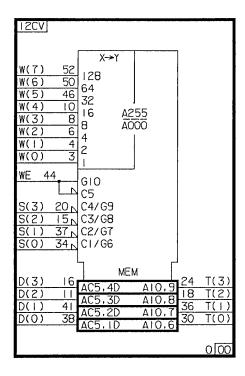
BIAS LØ = V21 BIAS HI = NØNE TERMINATE = V26, V27, V38, V39

OPERATIONAL DESCRIPTION

Input pins V22, V23, and CLCK control the register. A control translation of 5 clocks input PB active (LO) into the upper register and inputs B(0-7) active (LO) into the lower register. A control translation of 6 clocks input PB active (LO) into the upper register and inputs B(0-7) active (HI) into the lower register. A control translation of 7 clears the register.

Output pin V37 is active (LO) when an odd number of parity checker inputs are active.

12CV-0 256 by 4-Bit RAM.



BIAS NONE

OPERATIONAL DESCRIPTION

The 12CV can write to or read from any one of 256 locations.

Inputs

W7 through WO are the address bits that are translated into write and read addresses.

WE controls the Write (WE = L0) and rad (WE = HI) operations.

S3 through S0 (active state = L0) select the data inputs and outputs.

D3 through D0 are the data inputs.

Outputs

T3 through T0 are the data outputs.

Write Operation

When WE is LO, clock modifier C5 clocks the write data into a memory location.

Read Operation

When WE is HI, gate modifier G10 gates the read data from a memory location.

CUT ALONG LIN

COMMENT SHEET

CDC key to level 4 Logic Diagrams Symbol Descriptions 12AA through 12AS, 12CA through 12CV Volume 1 Logic Diagram Symbols Manual

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CDC® KEY TO LEVEL 4 LOGIC DIAGRAMS

SYMBOL DESCRIPTIONS

12DA THROUGH 12DD, 12SA THROUGH 12SX, 12101 THROUGH 12422, 121HA THROUGH 121HH

VOLUME 2

LOGIC DIAGRAM SYMBOLS MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A (12-01-82)	Manual released.
B (04-16-84)	Engineering Change Order 45780. Manual revised to accommodate technical and editorial corrections. Because of extensive changes to this manual, chart tape and dots have not been used, and all pages reflect the latest revision level. This revision obsoletes all previous editions.
C (12-04-84)	Manual revised; includes Engineering Change Order 46650. Front Cover through 4 and 12CI-0 (2 of 5) in Volume 1 are revised.
D (04-15-85)	Manual revised; adds CYBERPLUS Arrays. In Volume 1, changed Front Cover, Title Page, Revision Record, 3 and 4. Added 5 and 6; changed old 5/6 to 7/8; changed 2-1, 12CB-5 (1 of 1), and Comment Sheet. In Volume 2, changed Front Cover, Title Page, Revision Record, 3 and 4. Added 5 and 6; changed old 5/6 to 7/8; changed 12SD-0 (1 of 1), and Comment Sheet. Inserted new index tab 12DA and pages 12DA (1 of 1), 12DB-0 (1 of 1), 12DB (1 of 1), 12DB-0 (1 of 1), 12DB-1 (1 of 1), 12DB-2 (1 of 1), 12DB-3 (1 of 1), 12DB-4 (1 of 1), 12DC (1 of 1), 12DC-0 (1 of 1), 12DD (1 of 1), 12DD-0 (1 of 1), 12SB (1 of 1), 12SB-0 (1 of 2), 12SB-0 (2 of 2), 12SB-1 (1 of 2), 12SB-1 (2 of 2), 12ST (1 of 1), 12ST-0 (1 of 2), 12ST-0 (2 of 2), 12SU (1 of 1), 12SU-1 (1 of 1), 12SX (1 of 1), 12SX-1 (1 of 2), 12SX-1 (2 of 2), 12122-1 (1 of 1), 12122-2 (1 of 1), 12141-1 (1 of 1), 12165-1 (1 of 1), 12180-1 (1 of 1), 12470-1 (1 of 1), 12474-1 (1 of 1).
E (06-13-86)	Manual revised; includes Engineering Change Order 47939. In Volume 1, Front Cover through 3, 5 through 8, 1-7/1-8, 1-9/1-10, and 12CI-0 (2 of 5) are revised. In Volume 2, Front Cover through 3, 5 through 8, and 12422 (1 of 1) are revised. Page 9 is added to both volumes.
F (03-06-87)	Manual revised; includes Engineering Change Order 48291. In Volume 1, Front Cover through 8, 1-11, 1-26, 12AF-6 (1 of 1), 12AG-6 (1 of 1), 12AM-2 (1 of 2), 12CL-0 (5 of 10), and 12CL-0 (7 of 10) are revised. In Volume 2, Front Cover through 8, 12DC-0 (1 of 1), 12SH-5 (2 of 2), 12SP-9 (1 of 1), and 12171 (1 of 1) are revised. In Volume 1, pages 12AK (1 of 1), 12AK-0 (1 of 2/2 of 2), 12AK-1 (1 of 2/2 of 2), 12AL (1 of 1), 12AL-0 (1 of 2/2 of 2), 12AL-1 (1 of 2/2 of 2), and 12CV are added.
Publication No. 60458120	

REVISION LETTERS I, O, Q, S, X AND Z ARE NOT USED.

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or use Comment Sheet in the back of this manual.

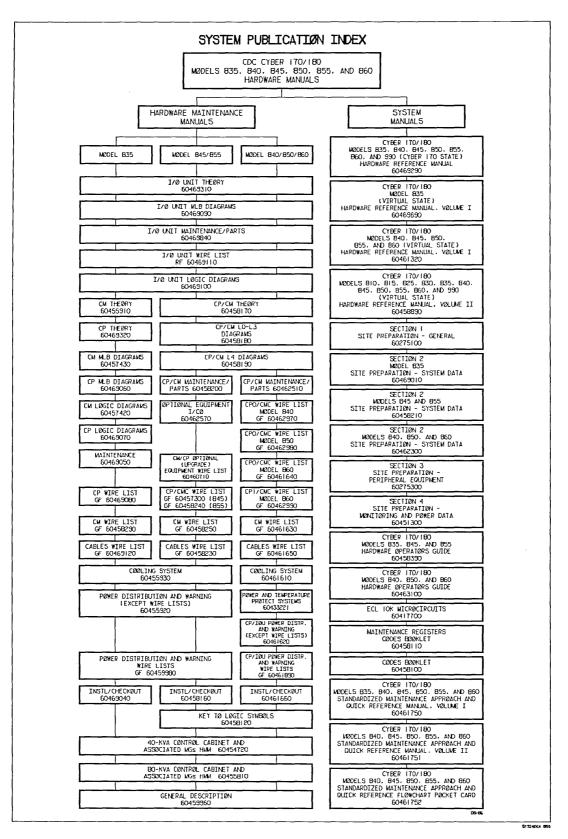
PREFACE

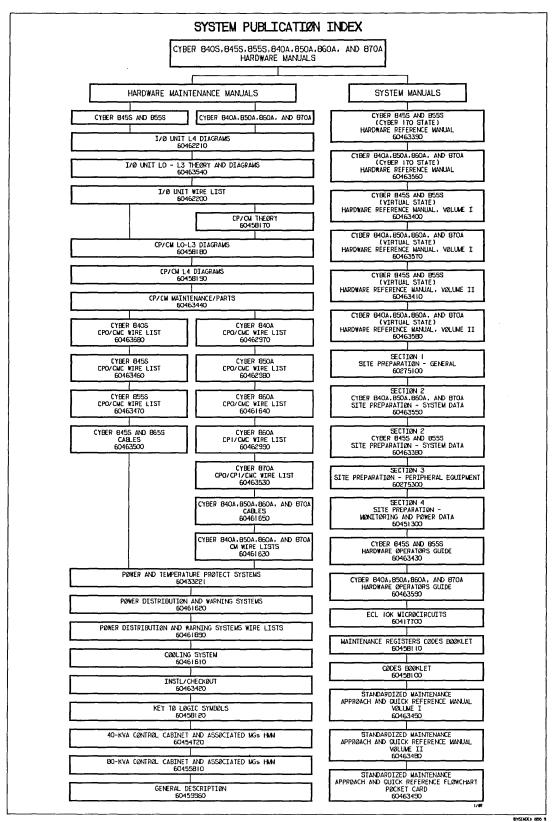
This manual is one of a set of manuals for the $CDC^{\textcircled{1}}$ CYBER 170 Models 845 and 855 Computer Systems, CYBER 180 Models 840, 845, 850, 855, 860, and 990 Computer Systems, CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 990E, and 995E Computer Systems, and the CYBERPLUS Parallel Processor. The System Publication Indexes on the following pages list other manuals that are applicable to the computer equipment.

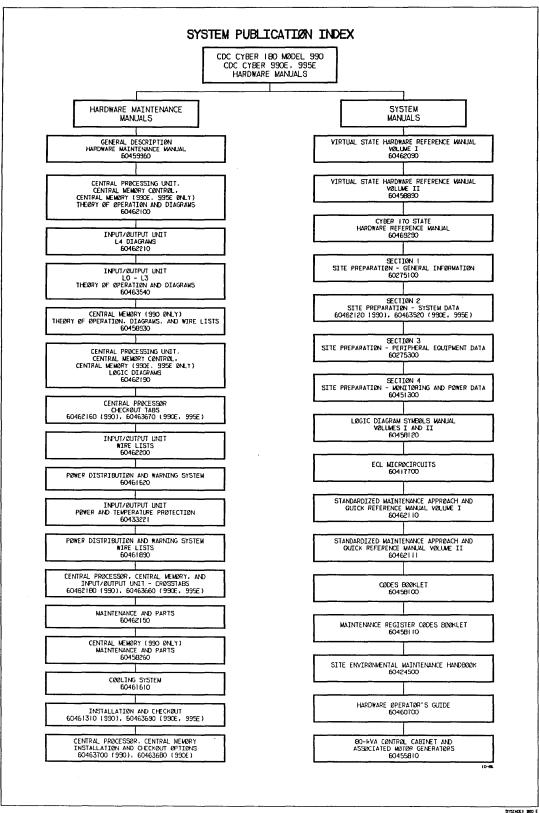
This manual contains two volumes. Volume 1 contains the key to level 4 (IA) diagrams section and the Symbol Descriptions section for the 12AA through 12CV LSI arrays. Volume 2 contains the Symbol Descriptions section for the 12DA through 12DD LST arrays, the 12SA through 12SX LSI arrays, the 12101 through 12474 Emitter Coupled Logic (ECL) 100,000 series microcircuits, and the 12HA through 12HH half-arrays.

The key to L4 diagrams section describes the L4 diagrams and supplementary charts such as backup charts and connector charts. The Symbol Descriptions section provides an operational description, pin number and bias information for every logic circuit used in the central processor.

This manual is intended primarily for customer engineers and does not contain design ground rules. Logic designers should refer to applicable Control Data specifications and vendor literature for complete electrical characteristics and application guidelines.







RELATED PUBLICATIONS (CYBERPLUS)

Following is a list of other manuals applicable to the CYBERPLUS Multiparallel Processor System. The manuals are available from:

Control Data Corporation Literature and Distribution Services 308 North Dale Street St. Paul, Minnesota 55103

<u>Title</u>	Publication Number
Medium and Large Scale Computer Systems, Site Preparation Manual, Section 1, General Information	60275100
CYBERPLUS Parallel Processor Site Preparation Manual, Section 2, Site Data	60461720
Medium and Large Scale Computer Systems, Site Preparation Manual, Section 3, Peripheral Equipment Data	60275300
Medium and Large Scale Computer Systems, Site Preparation Manual, Section 4, Monitoring and Power Data	60451300
Site Environmental Maintenance Handbook	60424500
CYBERPLUS Parallel Processor Hardware Maintenance Manual, Volume l Installation and Checkout	60461740
CYBERPLUS Parallel Processor Hardware Maintenance Manual, Volume 2 Maintenance and Parts Data	60461850
CYBERPLUS Parallel Processor Hardware Maintenance Manual, Volume 3 Diagrams	60461830
CYBERPLUS Parallel Processor Hardware Maintenance Manual, Volume 4 Troubleshooting	60462390
CYBERPLUS Parallel Processor Hardware Reference Manual	77960981
CYBERPLUS Parallel Processor Wire Lists	60461870

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RELATED PUBLICATIONS (CYBERPLUS), Cont'd

<u>Title</u>	Publication Number
CYBERPLUS Parallel Processor CYBER 180 Models 840, 850, 860, 990 CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 990E, 995E Cooling System Hardware Maintenance Manual	60461610
CYBERPLUS Parallel Processor CYBER 180 Models 840, 850, 860, 990 CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 990E, 995E Power Distribution and Warning System Hardware Maintenance Manual	60461620
25-kVA Frequency Converter Hardware Maintenance Manual	60456520
40-kVA Control Cabinet and Associated Motor-Generators Hardware Maintenance Manual	60454720
80-kVA Control Cabinet and Associated Motor-Generators Hardware Maintenance Manual	60455810
CYBERPLUS Parallel Processor Maintenance Software Manual	60461730
Concurrent Maintenance Library (CML) Reference Manual	60455980

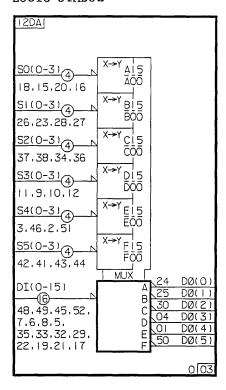
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12AH		12102	
12AI		12107	
12AJ		12112	
12AK		12114	
12AL		12117	

12DA

PIN	REAL	VIRT
NAME	PIN	PIN
DI(0)	48	V01
DI(1)	49	V02
DI(2)	45	V03
DI(3)	52	V04
DI(4)	07	V05
DI(5)	06	V06
DI(6)	08	V07
DI(7)	05	V08
DI(8)	35	V09
DI(9)	33	V10
DI(10)	32	V11
DI(11)	29	V12
DI(12)	22	V13
DI(13)	19	V14
DI(14)	21	V15
DI(15)	17	V16
S0(0)	18	V19
S0(1)	15	V20
S0(2)	20	V17
S0(3)	16	V18
S1(0)	26	V23
S1(1)	23	V24
S1(2)	28	V21
S1(3)	27	V22
S2(0)	37	V27
S2(1)	38	V28
S2(2)	34	V25
S2(3)	36	V26
S3(0)	11	V31
S3(1)	09	V32
S3(2)	10	V29
S3(3)	12	V30
S4(0)	03	V35
S4(1)	46	V36
S4(2)	02	V33
S4(3)	51	V34
S5(0)	42	V39
S5(1)	41	V40
S5(2)	43	V37
S5(3)	44	V38
D0(0)	24	V41
D0(1)	25	V42
D0(2)	30	V45
D0(3)	04	V43
D0(4)	01	V44
D0(5)	50	V46

<i>,</i>		•	



OPERATIONAL DESCRIPTION

The 12DA-0 array decodes incoming select bits and routes the incoming data bits accordingly. The select bits are four-bit groups coming from six different select registers. They specify which bit of the 16 incoming data bits is to be sent to any or all of the six possible output locations. However, the four-bit select groups are output-line specific (i.e. the group SO(0-3) controls only the output line DO(0) and therefore can only direct the selected bit of data to one location).

The incoming data is 16 single bits, each from the identical bit position of a maximum of 16 different data words.

The mux can select from one to six of up to 16 different data bits, and can individually route the selected bits to different locations simultaneously.

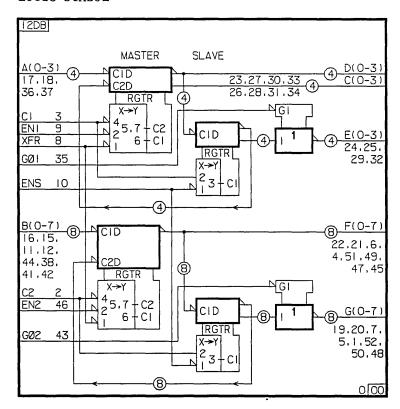
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12DB

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	17	V01
A(1)	18	V02
A(2)	36	V03
A(3)	37	V04
B(0)	16	V05
B(1)	15	V06
B(2)	11	V07
B(3)	12	V08
B(4)	44	V09
B(5)	38	V10
B(6)	41	V11
B(7)	42	V12
CLK1	03	V13
CLK2	02	V20
EN1	09	V17
EN2	46	V19
ENS	10	V14
XFR	08	V18
G01	35	V15
G02	43	V16
C(0)	26	V21
C(1)	28	V24
C(2)	31	V27
C(3)	34	V30
D(0)	23	V22
D(1)	27	V25
D(2)	30	V28
D(3)	33	V31
E(0)	24	V23
E(1)	25	V26
E(2)	29	V29
E(3)	32	V32
F(0)	22	V33
F(1)	21	V35
F(2)	06	V37
F(3)	04	V39
F(4)	51	V41
F(5)	49	V43
F(6)	47	V45
F(7)	45	V47
G(0)	19	V34
G(1)	20	V36
G(2)	07	V38
G(3)	05	V40
G(4)	01	V42
G(5)	52	V44
G(6)	50	V46
G(7)	48	V48

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OPERATIONAL DESCRIPTION

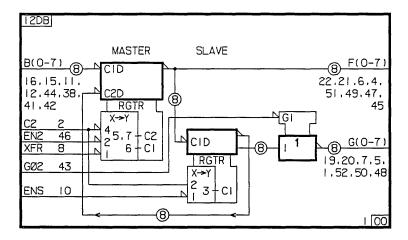
Data presented to the 12DB-0 array is available from the output lines of the master and slave registers during normal operation. The output from the slave registers is available to be gated to output lines for shadow selection and back into the master registers for restoration.

When an interrupt occurs the data is captured by the slave registers. Then, upon restoration of normal operation, the data is reestablished at the master registers by the slaves (note polarity of clock 1, above) and the operation resumes from the conditions that existed at the moment the interrupt occurred.

The 12DB-0 array consists of master registers of four and eight bits and equivalent slave registers. The input control for the master registers is the translation of a clock, enable one, and a transfer signal which selects the data to be captured. Separate clock signals control the A-rank (four-bit) and the B-bank (eight-bit) registers. The input control for the slave registers consists of two signals. The same clock signals (but opposite polarity) that is presented to the master registers, and enable slave.

The outputs available are from the master registers and the gated outputs from the slave registers. The true signal from the slaves is also routed back into the master registers.

60458120 D



OPERATIONAL DESCRIPTION

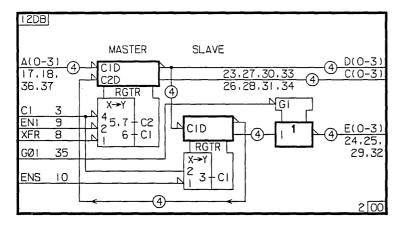
This symbol is the lower section of a 12DB-0. The data input, B(0-7), to this array is output from the array on the master and slave register output lines. Slave output is available for gating on the output lines for shadow selection and back into the master register for restoration.

When an interrupt occurs, data is captured by the slave register. On restoration of normal operation, data is reestablished by gating slave register output to master register input. Operation then can resume, picking up conditions that existed at the moment the interrupt occurred.

The array has master and slave registers, each eight bits, and for the master register, an input control which is the translation of clock C2, enable EN2, and transfer signal XFR. Input control for the slave register consists of clock C2 (inverted from C2 at the master), and enable ENS.

Gated outputs are available from master and slave, and the true signals from the slave are also routed back to the master register input.

60458120 D l of 1



OPERATIONAL DESCRIPTION

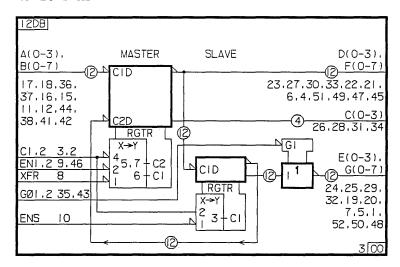
This symbol is the upper section of a 12DB-0. The data input, A(0-3), to this array is output from the array on the master and slave register output lines. Slave output is available for gating on the output lines for shadow selection and back into the master register for restoration.

When an interrupt occurs, data is captured by the slave register. On restoration of normal operation, data is re-established by gating slave register output to master register input. Operation then can resume, picking up conditions that existed at the moment the interrupt occurred.

The array has master and slave registers, each four bits, and for the master register, an input control which is the translation of clock Cl, enable ENl, and transfer signal XFR. Input control for the slave register consists of clock Cl (inverted from Cl at the master), and enable ENS.

Gated outputs are available from master and slave, and the true signals from the slave are also routed back to the master register input.

60458120 D



OPERATIONAL DESCRIPTION

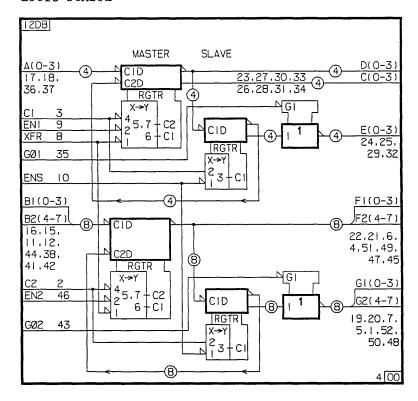
This symbol is the full 12DB-0 depicted as a single symbol. Data input, A(0-3), B(0-7), to this array is output from the array on the master and slave register output lines. Slave output is available for gating on the output lines for shadow selection and back into the master register for restoration.

When an interrupt occurs, data is captured by the slave register. On restoration of normal operation, data is reestablished by gating slave register output to master register input. Operation then can resume, picking up conditions that existed at the moment the interrupt occurred.

The array has master and slave registers, each 12 bits, and for the master register, an input control that is the translation of clocks C1 and C2 (tied together externally), enables EN1 and EN2 (tied together), and transfer signal XFR. Input control for the slave register consists of clocks C1 and C2 (tied together and inverted from C1 and C2 at the master), and enables EN1 and EN2 (tied together).

Gated outputs are available from master and slave, and the true signals from the slave are also routed back to the master register input.

60458120 D l of 1



OPERATIONAL DESCRIPTION

This symbol is a special 12DB-0 case (B-inputs and F-outputs are split). The data input, A(0-3), B1(0-3), B2(4-7), to this array is output from the array on the master and slave register output lines. Slave output is available for gating on the output lines for shadow selection and back into the master register for restoration.

When an interrupt occurs, data is captured by the slave register. On restoration of normal operation, data is reestablished by gating slave register output to master register input. Operation then can resume, picking up conditions that existed at the moment the interrupt occurred.

The array has four and eight-bit master and slave registers. For the four-bit master register, input control is the translation of clock Cl, enable ENl, and transfer signal XFR. Input control for the four-bit slave register consists of clock Cl (inverted from Cl at the master), and enable ENS.

For the eight-bit master register, input control is the translation of clock C2, enable EN2, and transfer signal XFR. Input control for the eight-bit slave register consists of clock C2 (inverted from C2 at the master), and enable ENS.

Input to the eight-bit master is shown, by split input, B1(0-3), B2(4-7), as originating on two different auxilliary boards. Gated outputs are available from master and slave, and the true signals from the slave also are routed back to the master register input.

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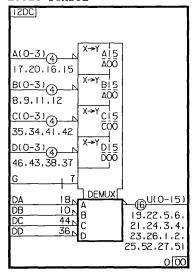
12DC

PIN	REAL	VIRT
NAME	PIN	PIN
DA	18	V41
DB	10	V31
DC	44	V36
DD	36	V26
AD0	17	V12
A01	20	V11
A02	16	V04
A03	15	V03
B00	08	V14
B01	09	V13
B02	11	V06
B03	12	V05
C00	35	V16
C01	34	V15
C02	41	V08
C03	42	V07
D00	46	V18
D01	43	V17
D02	36	V10
D03	37	V09
G	07	V19
H	28	V46
J	29	V47
K	49	V48
L	48	V49
F	45	V50
U(00)	19	V45
U(01)	22	V35
U(02)	05	V40
U(03)	06	V30
U(04)	21	V44
U(05)	24	V34
U(06)	03	V39
U(07)	04	V29
U(08)	23	V43
U(09)	26	V33
U(10)	01	V38
U(11)	02	V28
U(12)	25	V42
U(13)	52	V32
U(14)	27	V37
U(15)	51	V27
M	30	V51
N	31	V52
P	33	V53
R	32	V54
T	50	V55
V	47	V56

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12DC-0 Control Fanout.

LOGIC SYMBOL



OPERATIONAL DESCRIPTION

The mux portion of the 12DC-0 array consists of circuits that decode incoming designation bits and route incoming data bits accordingly. Incoming data is four single bits, each from identical bit positions of up to four different elements. The four sets of designation bits, which are presented to the decoder, specify which line or lines of the 16 output lines will receive which bit or bits of the incoming data. Each four-bit designation group controls selection of a specific data bit.

The AND portion of the 12DC-0 array is a four section AND gate with common gating. The four sections have the true signals available as outputs. Two of the sections also have the false signals available.

The outgoing data is up to four single bits, each from the identical bit position of a maximum of four different data words, and are transmitted on one to four of a maximum of 16 output data lines. The output lines are going to 16 different locations.

The 12DC-0 array can select from one to four bits of data, each to be routed to one of 16 possible destinations simultaneously.

The common gate signal is used to enable or disable four clock signals as required.

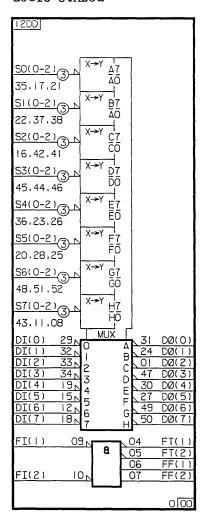
60458120 F

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12DD

PIN	REAL	VIRT
NAME	PIN	PIN
CLK	03	V33
DI(0)	29	V01
DI(1)	32	V02
DI(2)	33	V03
DI(3)	34	V04
DI(4)	19	V05
DI(5)	15	V06
DI(6)	12	V07
DI(7)	18	V08
FI(1)	09	V35
FI(2)	10	V40
FSE	02	V34
S0(0)	35	V09
S0(1)	17	V10
S0(2)	21	V11
S1(0)	22	V12
S1(1)	37	V12
S1(2)	38	V13
S2(0)	16	V15
S2(1)	42	V16
S2(2)	41	V17
S3(0)	45	V18
S3(1)	44	V19
S3(2)	46	V20
S4(0)	36	V21
S4(1)	23	V22
S4(2)	26	V23
S5(0)	20	V24
S5(1)	28	V25
S5(2)	25	V26
S6(0)	48	V27
S6(1)	51	V28
S6(2)	52	V29
S7(0)	43	V30
S7(1)	11	V31
S7(2)	08	V32
D0(0)	31	V41
D0(1)	24	V42
D0(2)	01	V43
D0(3)	47	V44
D0(4)	30	V45
D0(5)	27	V46
D0(6)	49	V47
D0(7)	50	V48
FF(1)	06	V36
FF(2)	07	V39
FT(1)	04	V37
FT(2)	05	V38

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OPERATIONAL DESCRIPTION

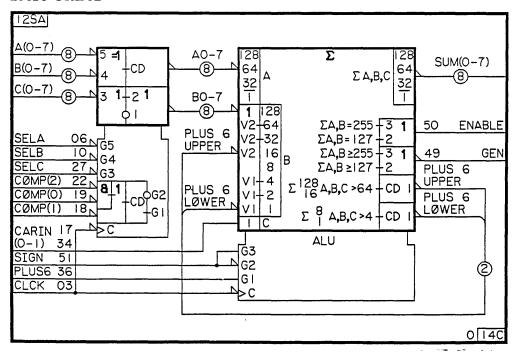
This array has eight data inputs, DI(0-7), and eight data outputs, DO(0-7). Each of the eight outputs is controlled by a three-bit decoder (typically SO(0-2) which controls the DO(0) output line) and any single output line can have any of the single inputs gated to it. For instance, decoder SO(0-2), with binary OIO inputs would gate input line DI(2) onto output DO(0). Data clocked into the array is captured in latches where it resides while being gated by the decoders.

The lower part of the symbol performs an AND function on inputs FI(1) and FI(2) and fans out the result to four outputs, two true, and two false.

60458120 D

12SA

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	05	V01
A(1)	08	V02
A(2)	15	V03
A(3)	12	V04
A(4)	38	V05
A(5)	42	V06
A(6)	45	V07
B(0) B(1) B(2)	48 09 04 16	V08 V09 V10 V11
B(3)	11	V12
B(4)	35	V13
B(5)	41	V14
B(6)	43	V15
B(7)	47	V16
C(0)	07	V17
C(1)	02	V18
C(2)	20	V17
C(3)	33	V20
C(4)	37	V21
C(5)	44	V22
C(6)	46	V23
C(7)	52	V24
CARIN(0) 17	V34
CARIN(1 CLCK CLKEN COMP(0)	03 01	V44 V39 V38 V40
COMP(1) COMP(2) PLUS6 SELA	22 36	V41 V42 V43 V45
SELB SELC SIGN	06 10 27 51	V46 V47 V37
ENABLE	50	V36
GEN	49	V35
NZERO	28	V33
OVFL	21	V48
SUM(0)	26	V25
SUM(1)	25	V26
SUM(2)	23	V27
SUM(3)	24	V28
SUM(4)	30	V29
SUM(5)	29	V30
SUM(6)	31	V31
SUM(7)	32	V32



BIAS LØ = CLKEN

IF CLØCK IS NØT USED: BIAS LØ = CLCK

BIAS HI = CLKEN

OPERATIONAL DESCRIPTION

The 12SA-O consists of two major functional elements: the input network (left side of symbol) and the arithmetic and logical unit (ALU).

Input Network

The input network controls the two operands which enter the ALU. Gating modifiers select A and/or B input highways through an exclusive OR function to an 8-bit register. Gating modifiers also select the C input highway and select between its true or complement states.

The SELA, SELB, and SELC inputs control gating modifiers G5, G4, and G3 respectively.

G5 active and G4 inactive selects the A input highway to the register.

G4 active and G5 inactive selects the B input highway to the register.

G4 and G5 both active results in an exclusive OR of the A and B input highways.

12SA-0 (Cont'd)

When clock on pin CLCK goes LO, clock modifier C clocks the selected data into the register.

- G3 selects the C input highway and G1 and G2 select between true or complement data.
- G3 active and G2 active selects C input highway data to the ALU.
- G3 active and G1 active selects the complement of the C input highway data to the ALU.

When G3 is inactive, G2 active gates HIs(zeros) and G1 active gates LOs(ones) to the ALU.

A 1-bit latch in the common control block controls gating modifiers Gl and G2. When the latch is set, Gl is active. When the latch is clear, G2 is active. Clock and inputs COMP(0-2) control the latch. The latch will set when clock goes L0 and the following equation is active:

COMP(1) OR (COMP(0) AND COMP(2)).

ALU

The ALU produces the summation of the A, B, and C operands and also produces the enable and generate signals which connect to a carry network external to the 12SA-0 array. The ALU also has the ability to force the B operand bits weighted 2, 4, 32, and 64 active. This ORs a value of 6 with the lower 4 bits of the B operand and a value of 96 with the upper 4 bits of the B operand. The ALU produces the PLUS 6 LOWER and PLUS 6 UPPER signals which control this operation.

A Operand Inputs

The A inputs to the ALU are weighted binarily and designated as operand A.

B Operand Inputs

The B inputs to the ALU enter through an OR function where the plus 6 modification takes place. When the PLUS 6 LOWER signal is LO, OR modifier VI is active. VI forces the bits weighted 2 and 4 active. When the PLUS 6 UPPER signal is LO, OR modifier V2 is active. V2 forces the bits weighted 32 and 64 active. When the OR modifiers are inactive, they have no effect on the B operand. The result of the OR function is weighted binarily and designated as operand B.

C Operand Input

The carry input enters the ALU on pins CARIN(0,1). The carry input has a binary weight of 1 and is designated as operand C. Note that the carry signal is active HI, i.e., the carry input has a value of 1 when it is HI.

SUM Outputs

The SUM(0-7) outputs are the summation of the A, B, and C operands.

12SA-0 (Cont'd)

Enable and Generate Outputs

The value of the summation of A and B and gating modifiers G2 and G3 control the ENABLE and GEN outputs. Input pin SIGN controls G2 and G3. The SIGN input is LO when the most-significant bits of the A and B operands are sign. Thus when the most-significant bit is sign, G2 is active and the 7 least-significant bits (maximum value of 127) control the enable and generate outputs. When the SIGN input is HI, all 8 bits (maximum value of 255) control the enable and generate outputs.

The ENABLE output is HI when G3 is active AND the summation of A and B is equal to 255 or G2 is active AND the summation of A and B is equal to 127.

The GEN output is LO when G3 is active AND the summation of A and B is greater then or equal to 255 or G2 is active AND the summation of A and B is greater than or equal to 127.

Plus 6 Upper and Lower Outputs

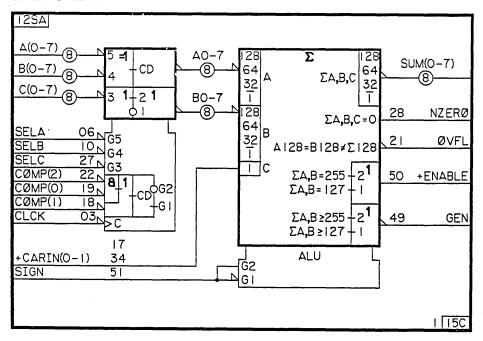
Input pin PLUS6 controls gating modifier Gl which gates the outputs of two latches to the PLUS 6 UPPER and PLUS 6 LOWER signals.

A transition to LO of the CLCK input sets the upper latch when the summation of the most-significant 4 bits of A, B, and C are greater than 64.

A transition to LO of the CLCK input sets the lower latch when the summation of the least-significant 4 bits of A, B, and C are greater than 4.

The PLUS 6 UPPER and PLUS 6 LOWER signals modify the next B operand to enter the ALU.

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BIAS LØ = CLKEN, PLUS6

IF CLØCK IS NØT USED: BIAS LØ = CLCK, PLUS6

BIAS HI = CLKEN

OPERATIONAL DESCRIPTION

The 12SA-1 consists of two major functional elements: the input network (left side of symbol) and the arithmetic and logical unit (ALU).

Input Network

The Input network controls the two operands which enter the ALU. Gating modifiers select A and/or B input highways through an exclusive OR function to an 8-bit register. Gating modifiers also select the C input highway and select between its true or complement states.

The SELA, SELB, and SELC inputs control gating modifiers G5, G4, and G3 respectively.

- G5 active and G4 inactive selects the A input highway to the register.
- ${\sf G4}$ active and ${\sf G5}$ inactive selects the B input highway to the register.
- G4 and G5 both active results in an exclusive OR of the A and B input highways.

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12SA-1 (Cont'd)

When clock on pin CLCK goes LO, clock modifier C clocks the selected data into the register.

- G3 selects the C input highway and G1 and G2 select between true or complement data.
- G3 active and G2 active selects C input highway data to the ALU.
- G3 active and G1 active selects the complement of the C input highway data to the ALU.

When G3 is inactive, G2 active gates HIs(zeros) and G1 active gates LOs(ones) to the ALU.

A 1-bit latch in the common control block controls gating modifiers Gl and G2. When the latch is set, Gl is active. When the latch is clear, G2 is active. Clock and inputs COMP(0-2) control the latch. The latch will set when clock goes L0 and the following equation is active:

COMP(1) OR [COMP(0) AND COMP(2)].

ALU

The ALU produces the summation of the A, B, and C operands and also produces the enable and generate signal which connect to a carry network external to the 12SA-1 array.

A and B Operand Inputs

The A and B operands enter the ALU where they are each weighted binarily and designated as operands A and B respectively.

C Operand Input

The carry input enters the ALU on pins CARIN(0,1). The carry input has a binary weight of l and is designated as operand C. Note that the carry signal is active HI, i.e., the carry input has a value of l when it is HI.

SUM Outputs

The SUM(0-7) outputs are the summation of the A, B, and C operands.

Zero Check Output

Output pin NZERO is HI when the summation of A, B, and C is equal to O.

Overflow Output

Output OVFL is LO when the most-significant bit of A is equal to the most-significant bit of B and not equal to the most-significant result bit.

Enable and Generate Outputs

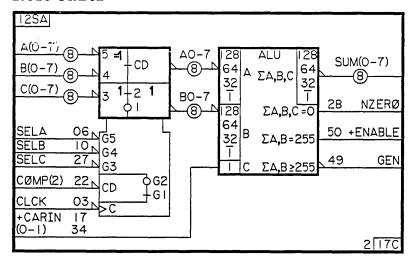
The value of the summation of A and B and gating modifiers G1 and G2 control the ENABLE and GEN outputs. Input pin SIGN controls G1 and G2. The SIGN input is LO when the most-significant bits of the A and B operands are sign. Thus when the most-significant bit is sign, G1 is active and the 7 least-significant bits (maximum value of 127) control the enable and generate outputs. When the SIGN input is HI, all 8 bits (maximum value of 255) control the enable and generate outputs.

12SA-1 (Cont'd)

The ENABLE output is HI when G2 is active AND the summation of A and B is equal to 255 or G1 is active AND the summation of A and B is equal to 127.

The GEN output is LO when G2 is active AND the summation of A and B is greater then or equal to 255 or G1 is active AND the summation of A and B is greater than or equal to 127.

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BIAS LØ = CLKEN, CØMP(O), PLUS6 BIAS HI = CØMP(I), SIGN IF CLØCK IS NØT USED: BIAS LØ = CLCK, CØMP(O), PLUS6 (SEE TYPE 3) BIAS HI = CLKEN, CØMP(I), SIGN

OPERATIONAL DESCRIPTION

The 12SA-2 consists of two major functional elements: the input network (left side of symbol) and the arithmetic and logical unit (ALU).

Input Network

The input network controls the two operands which enter the ALU. Gating modifiers select A and/or B input highways through an exclusive OR function to an 8-bit register. Gating modifiers also select the C input highway and select between its true or complement states.

The SELA, SELB, and SELC inputs control gating modifiers G5, G4, and G3 respectively.

G5 active and G4 inactive selects the A input highway to the register.

G4 active and G5 inactive selects the B input highway to the register.

G4 and G5 both active results in an Exclusive OR of the A and B input highways.

When clock on pin CLCK goes LO, clock modifier C clocks the selected data into the register.

- G3 selects the C input highway and G1 and G2 select between true or complement data.
- G3 active and G2 active selects C input highway data to the ALU.
- G3 active and G1 active selects the complement of the C input highway data to the ALU.

60458120 B

12SA-2 (Cont'd)

When G3 is inactive, G2 active gates HIs(zeros) and G1 active gates LOs(ones) to the ALU.

A 1-bit latch in the common control block controls gating modifiers G1 and G2. When the latch is set, G1 is active. When the latch is clear, G2 is active. Clock and input COMP(2) controls the latch.

ALU

The ALU produces the summation of the A, B, and C operands and also produces the enable and generate signals which connect to a carry network external to the 12SA-2 array.

A and B Operand Inputs

The A and B operands enter the ALU where they are each weighted binarily and designated as operands A and B respectively.

C Operand Input

The carry input enters the ALU on pins CARIN(0,1). The carry input has a binary weight of 1 and is designated as operand C. Note that the carry signal is active HI, i.e., the carry input has a value of 1 when it is HI.

SUM Outputs

The SUM(0-7) outputs are the summation of the A, B, and C operands.

Zero Check Output

Output pin NZERO is HI when the summation of A, B, and C is equal to zero.

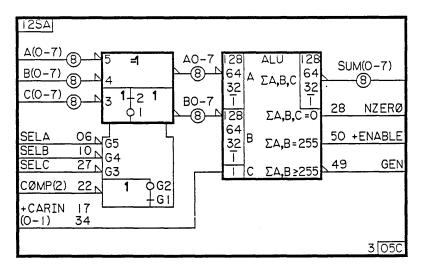
Enable Output

Output ENABLE is HI when the summation of A and B equals 255.

Generate Output

Output GEN is LO when the summation of A and B is greater than or equal to 255.

60458120 B



BIAS LØ = CLCK, CØMP(O), PLUS6 BIAS HI = CLKEN, CØMP(I), SIGN

OPERATIONAL DESCRIPTION

The 12SA-3 consists of two major functional elements: the input network (left side of symbol) and the arithmetic and logical unit (ALU).

Input Network

The Input network controls the two operands which enter the ALU. Gating modifiers select A and/or B input highways through an Exclusive OR function. Gating modifiers also select the C input highway and select between its true or complement states.

The SELA, SELB, and SELC inputs control gating modifiers G5, G4, and G3 respectively.

- G5 active and G4 inactive selects the A input highway.
- G4 active and G5 inactive selects the B input highway to the register.
- G4 and G5 both active results in an exclusive OR of the A and B input highways.
- G3 selects the C input highway and G1 and G2 select between true or complement data.
- G3 active and G2 active selects C input highway data to the ALU.
- G3 active and G1 active selects the complement of the C input highway data to the ALU.

12SA-3 (Cont'd)

When G3 is inactive, G2 active gates HIs(zeros) and G1 active gates LOs(ones) to the ALU.

The COMP(2) input controls G1 and G2. When COMP(2) is LO, G1 is active. When COMP(2) is HI, G2 is active.

ALU

The ALU produces the summation of the A, B, and C operands and also produces the enable and generate signal which connect to a carry network external to the 12SA-3 array.

A and B Operand Inputs

The A and B operands enter the ALU where they are each weighted binarily and designated as operands A and B respectively.

C Operand Input

The carry input enters the ALU on pins CARIN(0,1). The carry input has a binary weight of 1 and is designated as operand C. Note that the carry signal is active HI, i.e., the carry input has a value of 1 when it is HI.

SUM Outputs

The SUM(0-7) outputs are the summation of the A, B, and C operands.

Zero Check Output

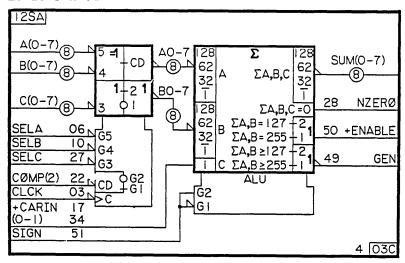
Output pin NZERO is HI when the summation of A, B, and C is equal to O.

Enable Output

Output ENABLE is HI when the summation of A and B equals 255.

Generate Output

Output GEN is LO when the summation of A and B is greater than or equal to 255.



BIAS LØ = CLKEN, CØMP(O), PLUS6 BIAS HI = CØMP(I) IF CLØCK IS NØT USED: BIAS LØ = CLCK, CØMP(O), PLUS6 (SEE TYPE 5) BIAS HI = CLKEN, CØMP(I)

OPERATIONAL DESCRIPTION

The 12SA-4 consists of two major functional elements: the input network (left side of symbol) and the arithmetic and logical unit (ALU).

Input Network

The Input network controls the two operands which enter the ALU. Gating modifiers select A and/or B input highways through an Exclusive OR function. Gating modifiers also select the C input highway and select between its true or complement states.

The SELA, SELB, and SELC inputs control gating modifiers G5, G4, and G3 respectively.

- G5 active and G4 inactive selects the A input highway.
- G4 active and G5 inactive selects the B input highway to the register.
- G4 and G5 both active results in an exclusive OR of the A and B input highways.

When clock on pin CLCK goes LO, clock modifier C clocks the selected data into the register.

- G3 selects the C input highway and G1 and G2 select between true or complement data.
- G3 active and G2 active selects C input highway data to the ALU.
- G3 active and G1 active selects the complement of the C input highway data to the ALU.

12SA-4 (Cont'd)

When G3 is inactive, G2 active gates HIs(zeros) and G1 active gates LOs(ones) to the ALU.

A one-bit latch in the common control block controls gating modifiers Gl and G2. When the latch is set, Gl is active. When the latch is clear, G2 is active. Clock and input COMP(2) controls the latch.

ALU

The ALU produces the summation of the A, B, and C operands and also produces the enable and generate signal which connect to a carry network external to the 12SA-4 array.

A and B Operand Inputs

The A and B operands enter the ALU where they are each weighted binarily and designated as operands A and B respectively.

C Operand Input

The carry input enters the ALU on pins CARIN(0,1). The carry input has a binary weight of 1 and is designated as operand C. Note that the carry signal is active HI, i.e., the carry input has a value of 1 when it is HI.

SUM Outputs

The SUM(0-7) outputs are the summation of the A, B, and C operands.

Zero Check Output

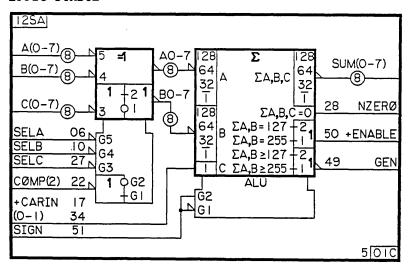
Output pin NZERO is HI when the summation of A, B, and C is equal to zero.

Enable and Generate Outputs

The value of the summation of A and B and gating modifiers G1 and G2 control the ENABLE and GEN outputs. Input pin SIGN controls G1 and G2. The SIGN input is LO when the most-significant bits of the A and B operands are sign. Thus when the most-significant bit is sign, G1 is active and the seven least-significant bits (maximum value of 127) control the enable and generate outputs. When the SIGN input is HI, all eight bits (maximum value of 255) control the enable and generate outputs.

The ENABLE output is HI when Gl is active AND the summation of A and B is equal to 255 or G2 is active AND the summation of A and B is equal to 127.

The GEN output is LO when Gl is active AND the summation of A and B is greater then or equal to 255 or G2 is active AND the summation of A and B is greater than or equal to 127.



BIAS LØ = CLCK, CØMP(O), PLUS6 BIAS HI = CLKEN, CØMP(I)

OPERATIONAL DESCRIPTION

The 12SA-5 consists of two major functional elements: the input network (left side of symbol) and the arithmetic and logical unit (ALU).

Input Network

The Input network controls the two operands which enter the ALU. Gating modifiers select A and/or B input highways through an Exclusive OR function. Gating modifiers also select the C input highway and select between its true or complement states.

The SELA, SELB, and SELC inputs control gating modifiers G5, G4, and G3 respectively.

- G5 active and G4 inactive selects the A input highway to the register.
- G4 active and G5 inactive selects the B input highway to the register.
- G4 and G5 both active results in an Exclusive Or of the A and B input highways.
- G3 selects the C input highway and G1 and G2 select between true or complement data.
- G3 active and G2 active selects C input highway data to the ALU.
- G3 active and G1 active selects the complement of the C input highway data to the ALU.

When G3 is inactive, G2 active gates HIs(zeros) and G1 active gates LOs(ones) to the ALU.

12SA-5 (Cont'd)

The COMP(2) input controls G1 and G2. When COMP(2) is LO, G1 is active. When COMP(2) is HI, G2 is active.

ALU

The ALU produces the summation of the A, B, and C operands and also produces the enable and generate signal which connect to a carry network external to the 12SA-5 array.

A and B Operand Inputs

The A and B operands enter the ALU where they are each weighted binarily and designated as operands A and B respectively.

C Operand Input

The carry input enters the ALU on pins CARIN(0,1). The carry input has a binary weight of 1 and is designated as operand C. Note that the carry signal is active HI, i.e., the carry input has a value of 1 when it is HI.

SUM Outputs

The SUM(0-7) outputs are the summation of the A, B, and C operands.

Zero Check Output

Output pin NZERO is HI when the summation of A, B, and C is equal to O.

Enable and Generate Outputs

The value of the summation of A and B and gating modifiers G1 and G2 control the ENABLE and GEN outputs. Input pin SIGN controls G1 and G2. The SIGN input is LO when the most-significant bits of the A and B operands are sign. Thus, when the most-significant bit is sign, G1 is active and the 7 least-significant bits (maximum value of 127) control the enable and generate outputs. When the SIGN input is HI, all 8 bits (maximum value of 255) control the enable and generate outputs.

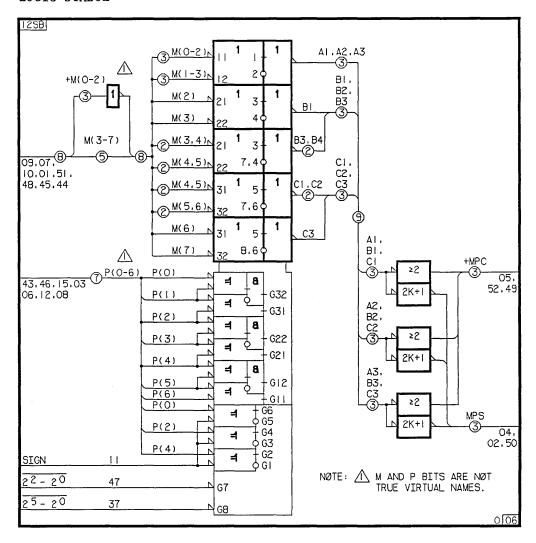
The ENABLE output is HI when Gl is active AND the summation of A and B is equal to 255 or G2 is active AND the summation of A and B is equal to 127.

The GEN output is LO when Gl is active AND the summation of A and B is greater then or equal to 255 or G2 is active AND the summation of A and B is greater than or equal to 127.

12SB

C DIN	DEAL	MDT
PIN NAME	REAL PIN	VIRT PIN
C(0)	38	V26
C(1) C(2)	35 17	V27 V28
C(3)	23	V29
CAND(0)		V08
CAND(1)		V09 V10
CAND(3)	51	V11
CAND(4)		V12 V13
CAND(5)		V13
CAND(7)	09	V15
D(0)	42 33	V22 V23
D(1) D(2)	18	V23 V24
D(3)	16	V25
NA(0) NA(1)	29 32	V34 V35
NA(1)	22	V36
NA(3)	20	V37
NB(0) NB(1)	34 36	V30 V31
NB(2)	19	V32
NB(3)	41	V33
PIN44 PIN46	37 47	V44 V46
PLIER(0)	08	V01
PLIER(1)	12	V02
PLIER(2) PLIER(3)	06 03	V03 V04
PLIER(4)	15	V05
PLIER(5)	46	V06
PLIER(6) SIGN	43 11	V07 V48
MPS(0)	04	V18
MPS(1) MPS(2)	02 50	V17 V16
NMPC(0)		V21
NMPC(1)	52 49	V20 V19
NPC(0)	28	V19 V47
NPC(0)	27	V43
NPC(1) NPC(2)	24 31	V42 V41
PS(0)	26	V45
PS(0)	25	V40
PS(1) PS(2)	21 30	V39 V38

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OPERATIONAL DESCRIPTION

NOTE

Element input names used in this description apply to CYBERPLUS. They are not true virtual identifiers. The names in this description do match the logic symbol shown.

This circuit is a 3-to-2 partial adder consisting of three columns of logic. An array contains one circuit.

The left column contains a single element represented as an OR gate. This element inverts the three inputs +M(0-2) so they will be the same state as inputs M(3-7).

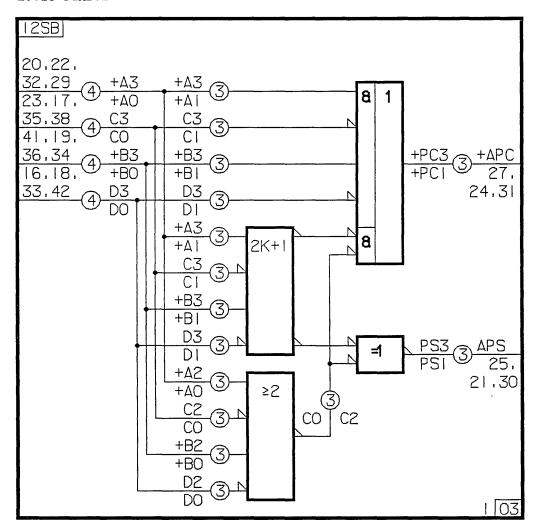
The middle column forms three, three-bit groups (A1-A3, B1-B3, C1-C3) from the inputs M(0-7) as determined by the G terms formed from combinations of the common control block inputs.

The active G terms are determined as follows:

Outputs	Active G Term	Control Block Inputs
A1, A2, A3	G1 G2	SIGN = $P(4)$ SIGN $\neq P(4)$
B1, B2, B3	G3 G4	$SIGN = P(2)$ $SIGN \neq P(2)$
C1, C2, C3	G5 G6	$SIGN = P(0)$ $SIGN \neq P(0)$
	G11 G12	$P(6) \neq P(5)$ P(6) = P(5) AND P(5) = P(4)
	G21 G22	$P(4) \neq P(3)$ P(4) = P(3) AND P(3) = P(2)
	G31 G32	P(2) = P(1) P(2) = P(1) AND $P(0)$
	G 7	$\frac{1}{2^2-2^0}$, (pin 47)
	G8	$\frac{1}{2^{5}-2^{0}}$, (pin 37)

Example: Outputs A1-A3 will be the same as inputs +M(0-2) when G1 and G11 are active. These outputs will be inverted when G2 and G11 are active.

The right column has three elements, each containing a logic threshold and an odd circuit. If two or three inputs are LO, the logic threshold circuit is active and its output, +MPC, is HI. If one or three inputs are LO, the odd circuit is active and its output MPS is LO.



NO BIAS
MOST SIGNIFICANT PS AND PC BIT
HAS A 2 WAY FANOUT

12SB-1 (Cont'd)

OPERATIONAL DESCRIPTION

This circuit is a 4-to-2 partial adder. An array contains three circuits.

The odd element has four inputs. If an odd number of inputs are active, the element is active and its two outputs are LO.

The logic threshold element has four inputs. If two or more inputs are active, the elements is active and its output is LO.

The exclusive OR element has two inputs, one from the odd element and one from the logic threshold element. If these inputs are unlike the element is active and its output is LO. The most significant bit (PS3) has a two-way fanout.

The AND/OR element's upper AND gate is active if the C and D inputs are LO and the A and B inputs are HI. The lower AND gate is active if both the odd element and the logic threshold element are active. If either AND gate is active, the OR gate is active and its output is HI. The most significant bit (PC3) has a two-way fanout.

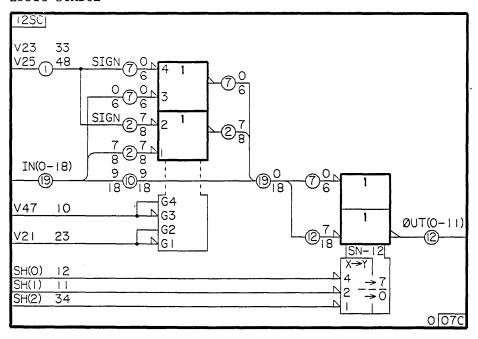
2K+1 AND/OR		2		+APC	2	APS	
Term	<u>Pin</u>	Term	<u>Pin</u>	Term	<u>Pin</u>	Term	<u>Pin</u>
+A3 +B3 C3 Dc	20 41 23 16	+A2 +B2 C2 D2	22 19 17 18	PC3	27,28	PS3	25,26
+A2 +B2 C2 D2	22 19 17 18	+A1 +B1 C1 D1	32 36 35 33	PC2	24	PS2	21
+A1 +B1 C1 D1	32 36 35 33	+A0 +B0 C0 D0	29 34 38 42	PC1	31	PS1	30

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12SC

PIN	REAL	VIRT
NAME	PIN	PIN
CARRY	16	V45
IN(0)	20	V01
IN(1)	32	V02
IN(2)	35	V03
IN(3)	38	V04
IN(4)	43	V05
IN(5)	46	V06
IN(6)	45	V07
IN(7)	44	V08
IN(8)	42	V09
IN(9)	41	V10
IN(10)	37	V11
IN(11)	36	V12
IN(12)	31	V13
IN(13)	29	V14
IN(14)	27	V15
IN(15)	01	V16
IN(16)	49	V17
IN(17)	25	V18
IN(18)	19	V19
SH(0)	12	V48
SH(1)	11	V26
SH(2)	34	V46
V20	07	V20
V21	23	V21
V22	22	V22
V23	33	V23
V24	17	V24
V25	48	V25
V27	08	V27
V28	09	V28
V29	15	V29
V30	21	V30
V31	18	V31
V32	52	V32
V47	10	V47
OUT(0)	06	V33
OUT(1)	05	V34
OUT(2)	04	V35
OUT(3)	02	V36
OUT(4)	03	V37
OUT(5)	47	V38
OUT(6)	51	V39
OUT(7)	26	V40
OUT(8)	24	V41
OUT(9)	28	V42
OUT(10) OUT(11)	30	V43 V44

	•	



BIAS LØ = V20, V27, V28, V29, V24, V31, V30, V22, V32 BIAS HI = CARRY

OPERATIONAL DESCRIPTION

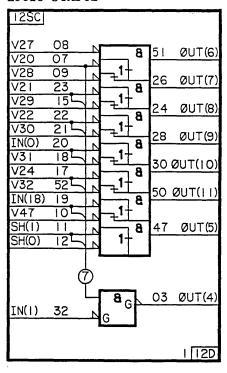
Shift Functions

The shift network function performs a right (down) shift of 0 to 7-bit positions controlled by SH (0-2). A shift of 0 causes input bits 7 through 18 to go to output highway pins OUT (0-11). A right shift of 1 causes input bit 6 to shift to OUT (0), input bits 7 through 17 to shift to OUT (1-11), and input bit 18 is shifted end-off. A right shift of 7 shifts input bits 0 through 6 to OUT (0-6), input bits 7 through 11 to OUT (7-11), and input bits 12 through 18 are shifted end-off.

Mux Functions

The mux function selects which input pins go to bits 0 through 8 of the shift function. The sign bit enters the mux function on input pins V23 and V25.

Pin V47 selects between input pins IN (0-6) or sign. Pin V21 selects IN (7-8) or sign.



BIAS LØ = CARRY

BIAS HI = V23, SH(2), IN(2)

OPERATIONAL DESCRIPTION

Inputs and Outputs

- + Enables enter pins V20, V21, V22, IN(0), V24, IN(18), and SH(1). Since the enables are preceded by a high level indicator (+ enables), they are high when there is an enable. Note on the enable inputs to the symbol, however, that the active state indicator's indicate that LO's are required to activate the OR functions they enter. Thus, an OR function is active when the enable entering it is LO (i.e. $\overline{\text{ENABLE}}$).
- Propagates enter pins V27, V28, V29, V30, V31, V32, V47, and SH(0).
- + Carries leave pins OUT (6-11) and OUT(5). The high level indicator indicates that the output is HI when there is a carry.

Carry Network

The carry network is composed of a series of OR and AND functions interconnected to propagate a carry upward through the network.

The following equations are listed in descending order of significance. Note how the least-significant carry [OUT(5)] is used in the OR function for the next move significant carry OUT(11)]. Thus the carry can propagate upward.

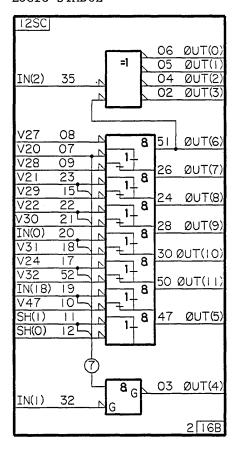
```
OUT(6) is HI when V27 is LO and [V20 is LO OR OUT (7) is HI].
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- OUT(7) is HI when V28 is LO and [V21 is LO OR OUT (8) is HI].
- OUT(8) is HI when V29 is LO and [V22 is LO OR OUT (9) is HI].
- OUT(9) is HI when V30 is LO and [IN(0) is LO OR OUT (10) is HI].
- OUT(10) is HI when V31 is LO and [V24 is LO OR OUT (11) is HI].
- OUT(11) is HI when V32 is LO and [IN(18) is LO OR OUT (5) is HI].
- OUT(5) is HI when V47 is LO and [SH(1) OR SH(0) are LO].

Group Enable

Output pin OUT(4) is active (LO) when all seven enables are HI and IN(1) is LO.

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		. •	



BIAS LØ = CARRY BIAS HI = V23, SH(2)

OPERATIONAL DESCRIPTION

Inputs and Outputs

- + Enables enter pins V20, V21, V22, IN(0), V24, IN(18), and SH(1). Since the enables are preceded by a high level indicator (+ enables), they are high when there is an enable. Note on the enable inputs to the symbol, however, that the active state indicators indicate that LO's are required to activate the OR functions they enter. Thus, an OR function is active when the enable entering it is LO (i.e. ENABLE).
- Propagates enter pins V27, V28, V29, V30, V31, V32, V47, and SH(0).
- + Carries leave pins out (6-11) and OUT(5). The high level indicator indicates that the output is HI when there is a carry.

Carry Network

The carry network is composed of a series of OR and AND functions interconnected to propagate a carry upward through the network.

12SC-2 (Cont'd)

The following equations are listed in descending order of significance. Note how the least-significant carry [OUT(5)] is used in the OR function for the next more significant carry OUT(11)]. Thus the carry can propagate upward.

```
OUT(6) is HI when V27 is LO and [V20 is LO OR OUT (7) is HI].

OUT(7) is HI when V28 is LO and [V21 is LO OR OUT (8) is HI].

OUT(8) is HI when V29 is LO and [V22 is LO OR OUT (9) is HI].

OUT(9) is HI when V30 is LO and [IN(0) is LO OR OUT (10) is HI].

OUT(10) is HI when V31 is LO and [V24 is LO OR OUT (11) is HI].

OUT(11) is HI when V32 is LO and [IN(18) is LO OR OUT (5) is HI].

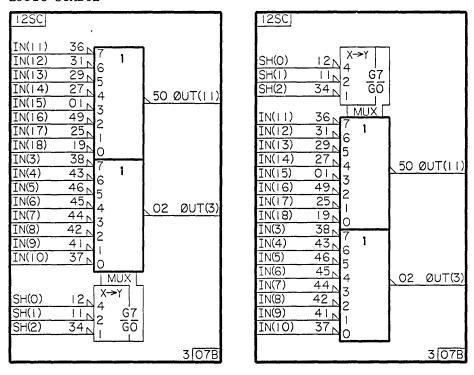
OUT(5) is HI when V47 is LO and [SH(1) OR SH(0) are LO].
```

Miscellaneous Functions

Output pins OUT (0-3) are all copies of an exclusive OR between IN(2) and OUT(6).

Output pin OUT(4) is active (LO) when all seven enables are HI and IN(1) is LO.

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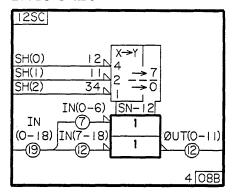
1 BIAS LØ = V20, V27, V28, V47, V29, V24, V31, V30, V22, V21, V32
2 BIAS HI = CARRY, V23, V25

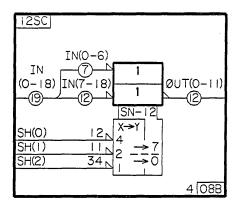
OPERATIONAL DESCRIPTION

Pins SH(0-2) select one of eight inputs to output OUT(11) and one of eight inputs to output OUT(3).

12SC-4 Right Shift Network.

LOGIC SYMBOL





BIAS LØ = V20, V27, V28, V47, V29, V24, V31, V30, V22, V21, V32 BIAS HI = CARRY, V23, V25

OPERATIONAL DESCRIPTION

The 12SC-4 performs a right (down) shift of 0 to 7-bit positions controlled by pins SH(0-2). A shift of 0 causes data from input pins IN(7-18) to go to output highway pins OUT(0-11). A right shift of 1 causes data from input pin IN(6) to shift to OUT(0), IN(7-17) to shift to OUT(1-11), and IN(18) is shifted end-off. A right shift of 7 shifts IN(0-6) to OUT(0-6), IN(7-11) to OUT(7-11), and IN(12-18) to shift end-off.

12SC)					
V27 V20	08 _N		8	51	ØUT(6)
V28 V21	09		_	26	ØUT(7)
V29	23 _A	7	8	24	ØUT(8)
V22 V30	517	_ <u>_</u>	8	28	ØUT(9)
IN(O) V31	20 ₇	1-	8	30	ØUT(10)
V24 V32	52 _N	1-	8	50	ØUT(11)
IN(18) V47	197	_ <u>_</u> 1-	8		
SH(I) SH(O)	12/	1_	8	47	ØUT(5)
				J 	5 13B

BIAS $L\emptyset$ = CARRY BIAS HI = V23, SH(2), IN(2)

OPERATIONAL DESCRIPTION

Inputs and Outputs

- + Enables enter pins V20, V21, V22, IN(0), V24, IN(18), and SH(1). Since the enables are preceded by a high level indicator (+ enables), they are high when there is an enable. Note on the enable inputs to the symbol, however, that the active state indicators indicate that LO's are required to activate the OR functions they enter. Thus, an OR function is active when the enable entering it is LO (i.e. ENABLE).
- Propagates enter pins V27, V28, V29, V30, V31, V32, V47, and SH(0).
- + Carries leave pins OUT (6-11) and OUT(5). The high level indicator indicates that the output is HI when there is a carry.

Carry Network

The carry network is composed of a series of OR and AND function interconnected to propagate a carry upward through the network.

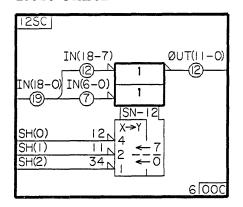
The following equations are listed in descending order of significance. Note how the least-significant carry [OUT(5)] is used in the OR function for the next more significant carry [OUT(11)]. Thus the carry can propagate upward.

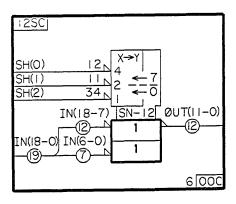
OUT(6) is HI when V27 is LO and [V20 is LO OR OUT (7) is HI].
OUT(7) is HI when V28 is LO and [V21 is LO OR OUT (8) is HI].
OUT(8) is HI when V29 is LO and [V22 is LO OR OUT (9) is HI].
OUT(9) is HI when V30 is LO and [IN(0) is LO OR OUT (10) is HI].
OUT(10) is HI when V31 is LO and [V24 is LO OR OUT (11) is HI].
OUT(11) is HI when V32 is LO and [IN(18) is LO OR OUT (5) is HI].

OUT(5) is HI when V47 is LO and [SH(1) OR SH(0) are LO].

12SC-6 Left Shift Network.

LOGIC SYMBOL





BIAS LØ = V20, V27, V28, V47, V29, V24, V31, V30, V22, V21, V32 BIAS HI = CARRY, V23, V25

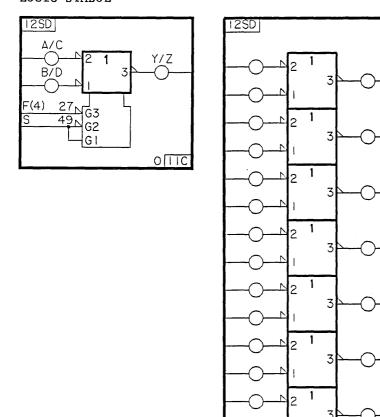
OPERATIONAL DESCRIPTION

The 12SC-6 performs a left (up) shift of 0 to 7-bit positions controlled by SH(0-2). A shift of 0 causes data from input pins IN(18-7) to go to output highway pins OUT(11-0). The most-significant bit enters the shift network on pin IN(18). A left shift of 1 causes data from input pin IN(6) to shift to OUT(0), IN(17-7) to shift to OUT(11-1), and IN(18) to shift end-off. A left shift of 7 shifts IN(6-0) to OUT(6-0), IN(11-7) to OUT(11-7), and IN(18-12) to shift end-off.

12SD

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	07	V06
A(1)	09	V05
A(2)	11	V04
A(3)	18	V03
A(4)	20	V02
A(5)	45	V01
B(0)	44	V18
B(1)	08	V17
B(2)	10	V16
B(3)	16	V15
B(4)	17	V14
B(5)	19	V13
C(0)	46	V12
C(1)	42	V11
C(2)	37	V10
C(3)	35	V09
C(4)	34	V08
C(5)	33	V07
CLCK	03	V48
D(0)	48	V24
D(1)	43	V23
D(2)	41	V22
D(3)	38	V21
D(4)	36	V20
D(5)	32	V19
F(0)	26	V46
F(1)	15	V45
F(2) F(3) F(4) R	12 02 27 51 49	V44 V43 V27 V25 V47
DFLAG	47	V26
M(1)	25	V28
M(2)	28	V29
M(3)	23	V30
Y(0)	52	V36
Y(1)	50	V35
Y(2)	01	V34
Y(3)	30	V33
Y(4)	31	V32
Y(5)	29	V31
Z(0)	04	V42
Z(1)	05	V41
Z(2)	06	V40
Z(3)	24	V39
Z(4)	21	V38
Z(5)	22	V37

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NØTE: G2 GATES IN A AND/ØR C TRUNKS, GI GATES IN B AND/ØR D TRUNKS, AND G3 GATES ØUT Y AND/ØR Z TRUNKS. THE DESIGNER MUST INDICATE THE TRUNK AND BITS HE IS USING.

27_NG3

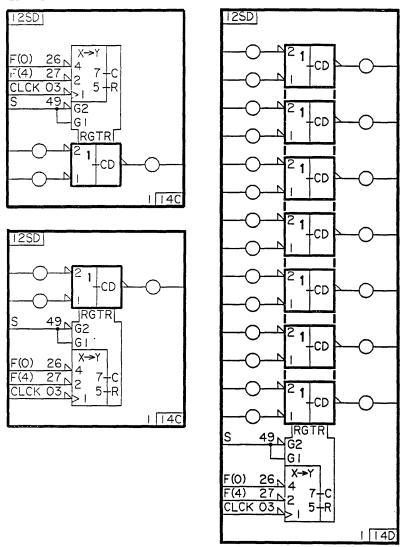
GΙ

BIAS LØ = CLCK, F(O), R BIAS HI = F(I-3)

OPERATIONAL DESCRIPTION

Pin S selects one of two input highways. Pin F(4) gates the selected data to the output highway.

OTTO

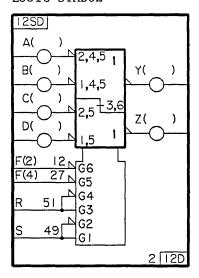


NØTE: G2 GATES IN A AND/ØR C TRUNKS, GI GATES IN B AND/ØR D TRUNKS. Y AND/ØR Z ARE ØUTPUT TRUNKS. THE DESIGNER MUST INDICATE THE TRUNK AND BITS HE IS USING.

BIAS LØ = F(1), R BIAS HI = F(3), F(2)

OPERATIONAL DESCRIPTION

Pin S selects one of two input highways. Pins F(0), F(4), and CLCK control the register. A translation of 7 clocks the register, 5 clears the register, and translations of 0-4 and 6 have no effect.

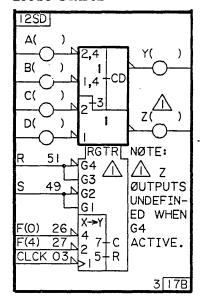


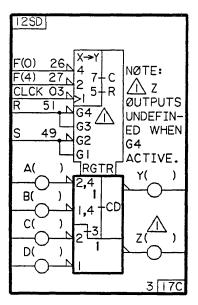
BIAS LØ = CLCK, F(0)BIAS HI = F(3), F(1)

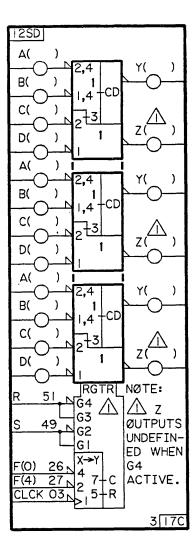
OPERATIONAL DESCRIPTION

The control pins select one of four input highways to output highway Y and one of two input highways (C or D) to output highway Z.

When G modifiers are grouped together as they are next to input highway A, an AND relationship exists between them. Therefore in order to gate input highway A to the Y output highway, gating modifiers G2, G4, and G5 must all be active. In order to gate input highway C to the Y output highway, G2 and G5 must both be active as well as G3 and G6.







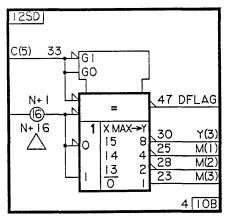
BIAS LØ = F(2), F(1)BIAS HI = F(3)

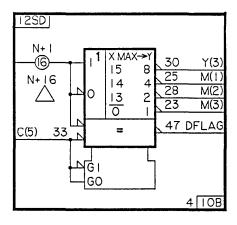
OPERATIONAL DESCRIPTION

Pins R and S select one of four input highways to the input of a register, and one of two input highways (C or D) to output highway Z. Pins F(0), F(4), and CLCK control the register. A translation of 7 clocks the register, 5 clears the register, and translations of 0-4 and 6 have no effect.

When G modifiers are grouped together as they are next to input highway A, an AND relationship exists between them. Therefore in order to gate input highway A into the OR function, gating modifiers G2 and G4 must both be active.

G3 gates the selection of C or D into the upper portion of the mux.





NØTE: ATHE FØLLØWING TABLE SHØWS THE PIN NAMES AND REAL PIN NUMBERS FØR EACH INPUT BIT TØ THE 12CD-4. NØTE THAT BITS N+7, N+8, N+11, N+13, N+14, AND N+15 REQUIRE TWØ INPUTS EACH.

BIT NØ.	N N+	I N+2	N+3	N+4	N+5	N+6	N+7	N+7	N+8	N+8	
PIN NAME	C(5) C(4) C(3)	C(2)	C(1)	C(O)	A(5)	B(5)	Δ(4)	B(4)	A(2)	
REAL PIN NØ.	33 34	35	37	42	46	45	19	20	17		
BIT NØ.	N+9 N+1	II+NC	N+11	N+12	N+13	N+13	N+14	N+14	N+15	N+15	N+16
PIN NAME	B(2) A() B(I)	A(0)	B(0)	D(5)	D(4)	D(3)	D(2)	D(1)	D(O)	R
REAL PIN NØ.	10 9	8	7	44	32	36	38	41	43	48	51

BIAS LØ = A(3), CLCK, F(0,3,4), S BIAS HI = B(3), F(1-2)

OPERATIONAL DESCRIPTION

The 12SD-4 receives 17 bits of data (N to N+16) and determines the highest-order bit which is different than bit N. It then produces a 4-bit code which contains the weight of that bit. Sign usually enters bit position N.

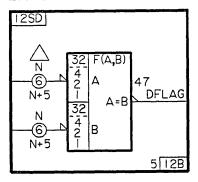
If bit N (pin C(5)) is LO, data bits N+1 to N+16 are gated into the priority coder function (X MAX->Y) active HI. This causes the priority coder function to produce a code for the highest order bit which is HI.

If bit N (pin C(5)) is HI, data bits N+1 to N+16 are gated into the priority coder function (X MAX->Y) active LO. This causes the priority coder function to produce a code for the highest order bit which is LO.

Bit N (pin C(5)) and data bits N+1 to N+16 also enter a logical identity function (=). If all the bits are alike, the data flag output (pin DFLAG) will be LO.

12SD-5 Six-Bit Compare Network.

LOGIC SYMBOL



BIT	REAL	PIN	CØMPARES	REAL	PIN
	PIN	NAME	TØ	PIN	NAME
N	20	A(4)		17	B(4)
N+ I	11,9	A(2),A(1)		10,8	B(2),B(1)
N+2	7	A(0)		44,32	B(0),D(5)
N+3	48	D(0)		51	R
N+4	43	D(1)		41	D(2)
N+5	38	D(3)		36	D(4)

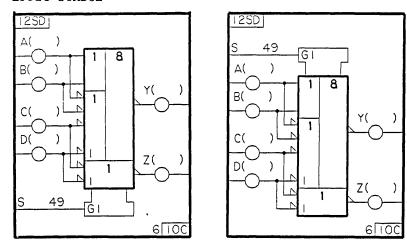
BIAS LØ = CLCK, F(0,3,4), S, A(3) BIAS HI = A(5), B(5), C(0-5), F(1-2), B(3)

OPERATIONAL DESCRIPTION

Output pin DFLAG will be LO when A equals B.

12SD-6 OR/AND Combination.

LOGIC SYMBOL



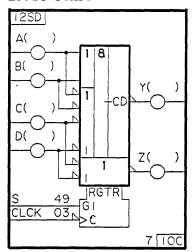
BIAS LØ = F(3), CLCK, F(2), F(4) BIAS HI = F(1), F(0), R

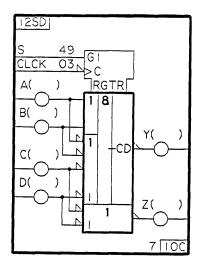
OPERATIONAL DESCRIPTION

For the following equations assume that pin S is HI.

Output highway Y = $(\overline{A} + \overline{B}) \bullet (A + B + C + D)$

Output highway Z = C + D





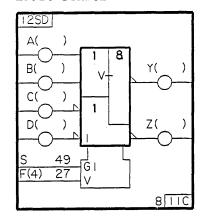
BIAS $L\emptyset = F(1-4)$ BIAS HI = F(0), R

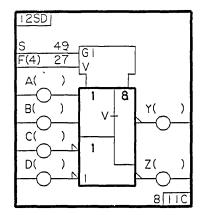
OPERATIONAL DESCRIPTION

For the following equations assume that pin S is HI and a clock pulse occurred on pin CLCK.

Register contents = $(\overline{A} + \overline{B}) \cdot (A + B + C + D)$

Output highway Z = C + D



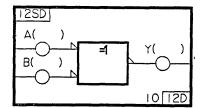


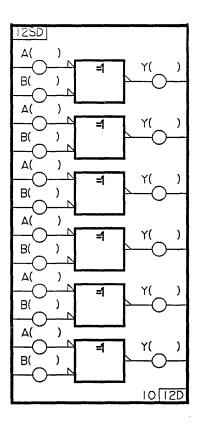
BIAS LØ = F(3), CLCK, F(2), F(0)BIAS HI = F(1), R

OPERATIONAL DESCRIPTION

Assume pin S is HI for the following equations:

Output highway $Y = (\overline{A} + \overline{B} + \overline{F(4)}) \bullet (C + D)$ Output highway Z = C + D

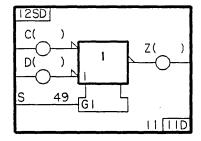


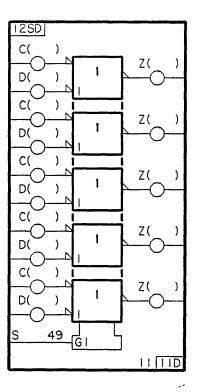


BIAS LØ = F(2-4), CLCK, R BIAS HI = F(0,1)

OPERATIONAL DESCRIPTION

The 12SD-10 performs an exclusive OR operation on input highways A and B.

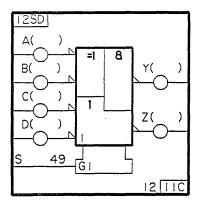




BIAS LØ = F(2-4), CLCK, R BIAS HI = F(0,1)

OPERATIONAL DESCRIPTION

Pin S gates highway D into the OR function.

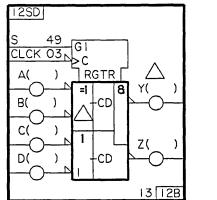


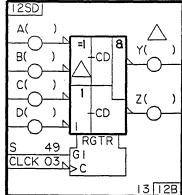
BIAS LØ = CLCK, F(O), F(2-4), R
BIAS HI =
$$F(I)$$

OPERATIONAL DESCRIPTION

Assume pin S is HI for the following equations:

Output highway $Y = A \oplus B \bullet (C + D)$ Output highway Z = C + D





NØTE: \triangle Y IS UNDEFINED IF A AND B ARE LØ SIMULTANEØUSLY.

BIAS LØ = F(0,1), F(3,4), R BIAS HI = F(2)

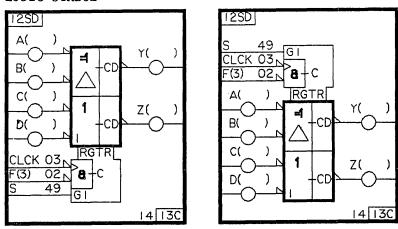
OPERATIONAL DESCRIPTION

The 12SD-13 contains two registers clocked by input pin CLCK. The upper register has an exclusive OR function as its input (A \bigoplus B). However, due to a design peculiarity of the 12SD array the contents of the upper register are undefined if both inputs to the exclusive OR are LO when the register is clocked.

The lower register has an OR function as its input (C + D). Pin S gates input highway D into the OR function.

Output highway Y is the AND of the contents of the two registers.

Output highway Z is the output from the lower register.



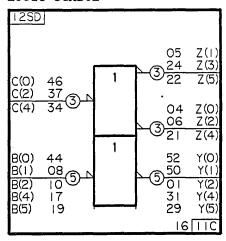
NØTE: / Y IS UNDEFINED IF A AND B ARE LØ SIMULTANEØUSLY.

BIAS LØ = F(1), F(4), R BIAS HI = F(2), F(0)

OPERATIONAL DESCRIPTION

The 12SD-14 contains two registers clocked by input CLCK. The upper register has an exclusive OR function as its input ($A \oplus B$). However, due to a design peculiarity of the 12SD array the contents of the upper register are undefined if both inputs to the exclusive OR are LO when the register is clocked.

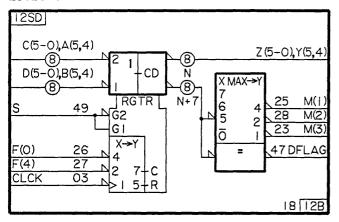
The lower register has an OR function as its input (C + D). Pin S gates input highway D into the OR function.



BIAS LØ = CLCK, F(O), F(3,4), S, R BIAS HI = A(O-5), C(1,3,5), F(1,2)

OPERATIONAL DESCRIPTION

The 12SD-16 contains two fanouts. The upper fanout provides two copies of 3 bits and the lower fanout provides one copy of 5 bits.



INPUT		INPUT	ØUTPUT				
BIT	Δ,	/C	B,	/D	CØDE		
SET	REAL	PIN	REAL	PIN	PINS		
JL 1	PIN	NAME	PIN	NAME	25, 28, 23		
N	33	C(5)	32	D(5)	111		
N+1	34	C(4)	36	D(4)	110		
N+2	35	C(3)	38	D(3)	101		
N+3	37	C(2)	41	D(2)	100 -		
N+4	42	C(1)	43	D(I)	011		
N+5	46	C(O)	48	D(0)	010		
N+6	45	A(5)	19	B(5)	001		
N+7	20	Δ(4)	17	B(4)	000		

BIAS LØ = F(1), R BIAS HI = A(0-3), B(0-3), F(2-3)

OPERATIONAL DESCRIPTION

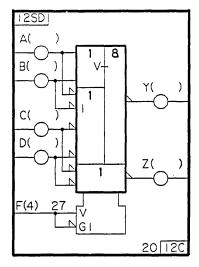
Register

Pin S selects one of two input highways. Pins F(0), F(4), and CLCK control the register. A translation of 7 clocks the register, 5 clears the register, and translations of 0-4 and 6 have no effect.

Priority Coder

The X MAX->Y function is a priority coder. It receives 8 input-bits weighted 0-7 and produces a 3-bit code which contains the weight of the highest order active bit.

The DFLAG output pin will be LO if all eight inputs are equal.



BIAS LØ = F(2-3), CLCK BIAS HI = F(0-1), S, R

OPERATIONAL DESCRIPTION

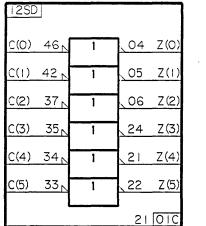
Output highway $Y = (\overline{A} + \overline{B} + \overline{F(4})) \bullet (A + (B \bullet F(4)) + C + D)$

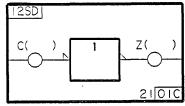
Note that F(4) when HI forces the upper input of the AND function active and when LO gates input highway B into the middle OR function.

Output highway Z = C + D.

12SD-21 Fanout.

LOGIC SYMBOL



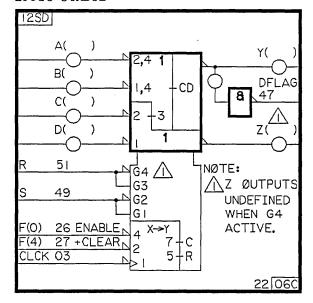


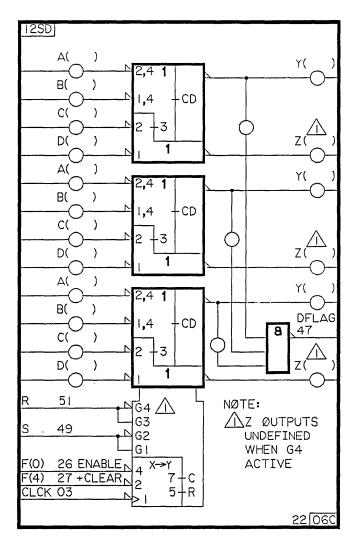
BIAS LØ = R, F(2-4), S, CLCK BIAS HI = F(O,1)

OPERATIONAL DESCRIPTION

Each input pin drives one output pin.

LOGIC SYMBOL





NØTE: ZERØ CHECK REQUIRES 6 INPUTS; THEREFØRE UNUSED INPUTS MUST BE BIASED TØ ZERØ.

BIAS LØ = F(2), F(1)

BIAS HI = F(3)

OPERATIONAL DESCRIPTION

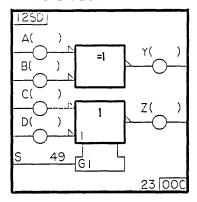
Pins R and S select one of four input highways to the input of a register, and one of two input highways (C or D) to output highway Z. Pins F(0), F(4), and CLCK control the register. A translation of 7 clocks the register, 5 clears the register, and translations of 0-4 and 6 have no effect.

When G modifiers are grouped together as they are next to input highway A, an AND relationship exists between them. Therefore in order to gate input highway A into the OR function, gating modifiers G2 and G4 must both be active.

12SD-22 (Cont'd)

G3 gates the selection of C or D into the upper portion of the mux.

Output pin DFLAG will be LO when the register data is all HI.



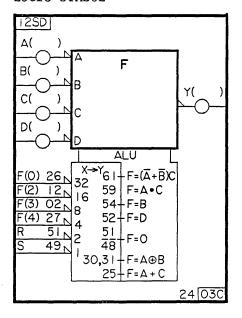
BIAS LØ = CLCK, F(2-4), R BIAS HI = F(0-1)

OPERATIONAL DESCRIPTION

The $12\,\mathrm{SD}\text{-}23$ contains two separate symbols; an exclusive OR of highways A and B and an OR of highways C and D.

Pin S gates input highway D into the OR function.

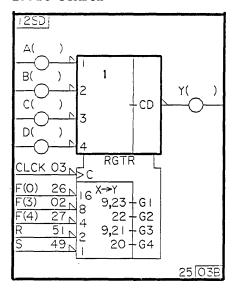
60458120 B



BIAS LØ = CLCK BIAS HI = F(I)

OPERATIONAL DESCRIPTION

The 12SD-24 performs logical operations on four input highways designated A, B, C, and D. The equations to the right of the coder function in the common control block describe the logical operations and identify the control code necessary for each. For example, a control code of 59 will cause a logical AND of the A and C input highways. Control codes of 48 through 51 cause the output to equal zero (All HI). Control codes of 30 and 31 cause an exclusive OR of input highways A and B. A control code of 52 causes the output to equal the contents of input highway D.



BIAS LØ = F(1-2)BIAS HI = NØNE

OPERATIONAL DESCRIPTION

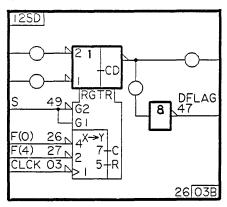
A 5-bit control code selects one or more input highways to a register. A select code of 23 selects input highway A. A select code of 9 selects both the A and the C highways. The two selected highways are ORed together in the OR function.

Select codes of 0-8, 10-19, and 24-31 make no selections and therefore select all zeros to the register.

Pin CLCK is the register clock.

12SD-26 Two-Input Multiplexer to a Register.

LOGIC SYMBOL



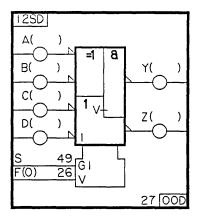
NØTE: G2 GATES IN A AND/ØR C TRUNKS, GI GATES IN B AND/ØR D TRUNKS, AND Y AND/ØR Z TRUNK ARE ØUTPUTS. THE DESIGNER MUST INDICATE THE TRUNK AND BITS HE IS USING.

BIAS LØ = F(1), R BIAS HI = F(2), F(3)

OPERATIONAL DESCRIPTION

Pin S selects one of two input highways. Pins F(0), F(4), and CLCK control the register. A translation of 7 clocks the register, 5 clears the register, and translations of 0-4 and 6 have no effect.

The DFLAG output pin will be LO when the contents of the register are all ${\tt HI}$.



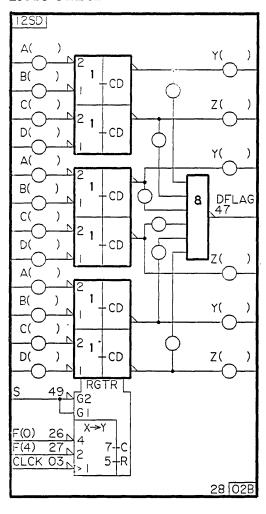
BIAS LØ =
$$F(2-4)$$
, CLCK, R
BIAS HI = $F(1)$

OPERATIONAL DESCRIPTION

Assume pin S is HI for the following equations.

Output highway $Y = A \oplus B \bullet (C + D + \overline{F(0)})$

Output highway Z = C + D



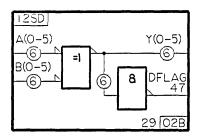
NØTE: ZERØ CHECK REQUIRES SIX INPUTS; THEREFØRE, UNUSED INPUTS MUST BE BIASED TØ ZERØ.

BIAS LØ = F(1), R BIAS HI = F(2,3)

OPERATIONAL DESCRIPTION

Pin S selects one of two input highways to each register. Pins F(0), F(4), and CLCK control the registers. A translation of 7 clocks the register, 5 clears the register, and translations of 0-4 and 6 have no effect.

Output pin DFLAG will be LO when the contents of all registers are HI.

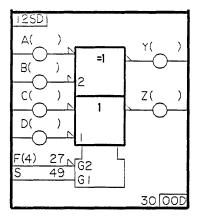


BIAS L0 = CLCK, F(2-4), R BIAS HI = F(0-1)

OPERATIONAL DESCRIPTION

 $Y = A \oplus B$

DFLAG will be LO when the result of the exclusive OR is all HI.

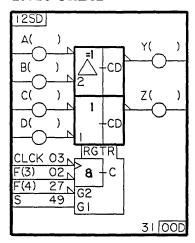


BIAS LØ = CLCK, F(2,3), R BIAS HI = F(0,1)

OPERATIONAL DESCRIPTION

Output highway $Y = A \oplus B$ Output highway Z = C + D

Pin F(4) gates input highway B into the exclusive OR function. Pin S gates input highway D into the OR function.



NØTE: A Y IS UNDEFINED IF A AND B ARE LØ SIMULTANEØUSLY.

BIAS LØ = F(1), R BIAS HI = F(0.2)

OPERATIONAL DESCRIPTION

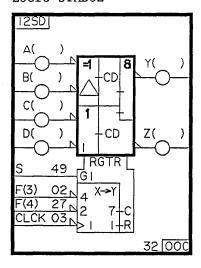
The 12SD-31 contains two registers controlled by CLCK and F(3).

The upper register has an exclusive OR as its input $(A \oplus B)$. Due to a design peculiarity of the 12SD array, the contents of the upper register are undefined if both inputs to the exclusive OR are LO when the register is clocked.

The lower register has an OR function as its input (C + D).

Pin S gates input highway D into the OR function.

Pin F(4) gates input highway B into the exclusive OR function.



NØTE: A Y IS UNDEFINED IF A AND B ARE LØ SIMULTANEØUSLY.

BIAS LØ = F(0), F(1), R

BIASHI = F(2)

OPERATIONAL DESCRIPTION

The 12SD-32 contains two registers controlled by pin F(3), F(4), and CLCK.

The upper register has an exclusive OR function as its input ($A \oplus B$). Due to a design peculiarity of the 12SD array, the contents of the upper register are undefined if both inputs to the exclusive OR are LO when the register is clocked.

The lower register has an OR function as its input (C + D). Pin S gates input highway D into the OR function.

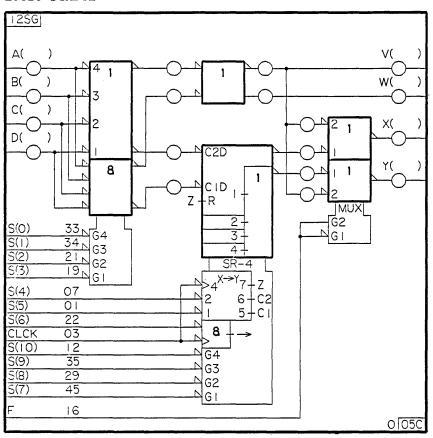
Output highway Y is the logical AND of the contents of the two registers.

Output highway Z is the output from the lower register.

12SG

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	41	V01
A(1) A(2)	37 09	V02 V03
A(3)	20	V04
B(0)	44	V05
B(1) B(2)	38 10	V06 V07
B(3)	15	V08
C(0)	46	V09
C(1) C(2)	36 11	V10 V11
C(3)	18	V112
CLCK	03	V28
D(0)	43 42	V13 V14
D(1) D(2)	08	V14
D(3)	17	V16
F S(0)	16 33	V48 V17
S(1)	33 34	V17
S(2)	21	V19
S(3) S(4)	19 07	V20 V21
S(5)	01	V21
S(6)	22	V23
S(7) S(8)	45 29	V24 V25
S(9)	35	V26
S(10)	12	V27
V(0)	48	V29
V(1) V(2)	51 32	V30 V31
V(3)	26	V32
W(0)	47 52	V33
W(1) W(2)	52 31	V34 V35
X(0)	50	V36
X(1)	02 30	V37 V38
X(2) X(3)	30 24	V38 V39
Y(0)	49	V40
Y(1) Y(2)	04 28	V41 V42
Y(3)	23	V42
Z(0)	06	V45
Z(1) Z(2)	05 27	V44 V46
Z(3)	25	V47

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BIAS NONE

OPERATIONAL DESCRIPTION

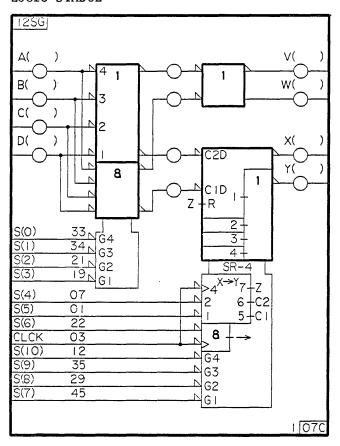
The shift register (SR-4) has two highwayed inputs, one from the four-highway input mux and one which is the AND of the same four input highways.

Pins S(4), S(5), and CLCK control the upper (first) rank of the shift register. A translation of 5 selects and clocks the AND data, 6 selects and clocks the mux data, and 7 clears the upper rank.

When pin S(6) is LO and clock (pin CLCK) goes LO, a right (down) shift of 1 takes place. The contents of the upper rank shift down to the second rank and the contents of the second rank shift down to the third rank etc. If a load of the first rank occurs at the same time as a shift, the new data is loaded and the previous contents are shifted.

The shift register has two highwayed outputs. The upper highway is always the output of the first rank. The lower output highway is controlled by pins S(7-10) and is the mux of any or all of the four ranks of the shift register. If more than one select signal is active (LO) at the same time, the contents of the selected ranks are ORed to the output highway.

Output highways V and W are the result of an OR of the input mux and the AND of the four input highways.



BIAS LØ = F BIAS HI = NØNE

OPERATIONAL DESCRIPTION

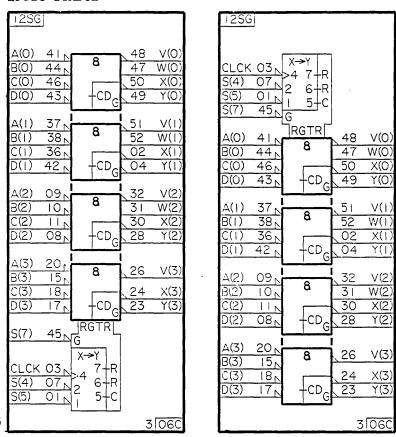
The shift register (SR-4) has two highwayed inputs, one from the four-highway input mux and one which is the AND of the same four input highways.

Pins S(4), S(5), and CLCK control the upper (first) rank of the shift register. A translation of 5 selects and clocks the AND data, 6 selects and clocks the mux data, and 7 clears the upper rank.

When pin S(6) is LO and clock (pin CLCK) goes LO, a right (down) shift of 1 takes place. The contents of the upper rank shift down to the second rank and the contents of the second rank shift down to the third rank etc. If a load of the first rank occurs at the same time as a shift, the new data is loaded and the previous contents are shifted.

The shift register has two highwayed outputs. The upper highway is always the output of the first rank. The lower output highway is controlled by pins S(7-10) and is the mux of any or all of the four ranks of the shift register. If more than one select signal is active (LO) at the same time, the contents of the selected ranks are ORed to the output highway.

Output highways V and W are the result of an OR of the input mux and the AND of the four input highways.

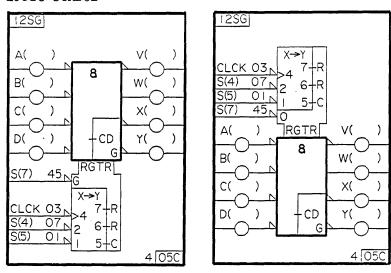


BIAS LØ = FBIAS HI = S(0-3), S(6), S(8-10)

OPERATIONAL DESCRIPTION

The V and W outputs are direct from the AND gates. The X and Y outputs are from the register. Pin S(7) gates the contents of the register to the Y outputs.

A control translation of 5 clocks the result of the AND gates into the register. Translations of 6 and 7 clear the register.

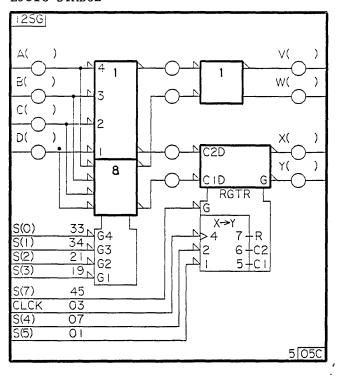


BIAS LØ = F BIAS HI = S(0-3), S(6), S(8-10)

OPERATIONAL DESCRIPTION

Output highways V and W are direct from the AND of the four input highways. The X and Y output highways are from the register. Pin S(7) gates the contents of the register to output highway Y.

A control translation of 5 clocks the result of the AND into the register. Translations of 6 and 7 clear the register.



BIAS LØ = F BIAS HI = S(6), S(8-10)

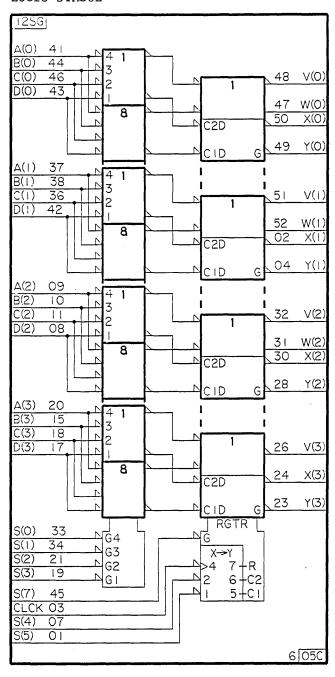
OPERATIONAL DESCRIPTION

The register has two highwayed inputs, one from the four-highway input mux and one from the AND of the same four input highways.

Pins S(4), S(5), and CLCK control the register. A translation of 5 selects and clocks the AND data, 6 selects and clocks the mux data, and 7 clears the register.

Pin S(7) gates the contents of the register to output highway.

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BIAS LØ = F BIAS HI = S(6), S(8-10)

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12SG-6 (Cont'd)

OPERATIONAL DESCRIPTION

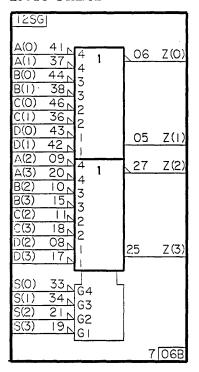
Output pins V and W are the result of OR functions. Output pins X and Y are the contents of the register. Pin S(7) gates the contents of the register to the Y outputs.

Each bit of the register has two inputs, one from the 4-input mux and one from the AND of the same 4 inputs.

Pins S(4), S(5), and CLCK control the register. A control translation of 5 selects and clocks the results of the AND gates into the register, 6 selects and clocks the mux result to the register, and 7 clears the register.

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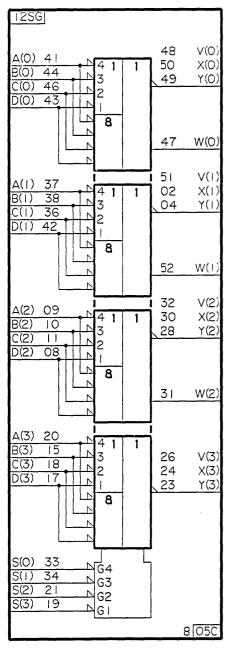


BIAS NØNE

OPERATIONAL DESCRIPTION

Each control pin, S(0-3), gates two inputs to the upper OR function and two inputs to the lower OR function. Selected inputs are ORed together in each OR function.

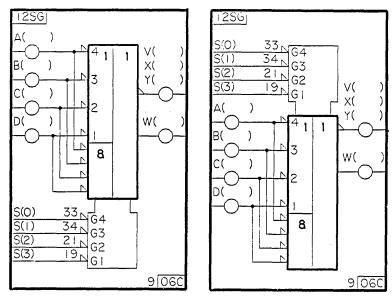
Output pins Z(0-1) are both the result of the upper OR function. Pins Z(2-3) are both the result of the lower OR function.



BIAS LØ = NØNE BIAS HI = F

OPERATIONAL DESCRIPTION

The outputs come from OR functions. Each of these OR functions has two inputs, a four-input \max and an AND of the same four inputs.



BIAS LØ = NØNE BIAS HI = F

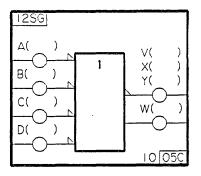
OPERATIONAL DESCRIPTION

The OR function has two highwayed inputs. One input from the four-highway mux, the other from an AND of the same four input highways.

Outputs V, X, and Y are three copies of the active LO highwayed result. Output W is an active HI highwayed result.

12SG-10 OR Function.

LOGIC SYMBOL



BIAS LØ =
$$S(O-3)$$

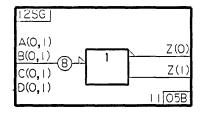
BIAS HI = F

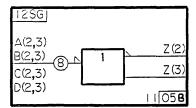
OPERATIONAL DESCRIPTION

Outputs V, X, and Y are three copies of the active LO highwayed result (A + B + C + D). Output W is the active HI highwayed result.

12SG-11 OR Function.

LOGIC SYMBOL

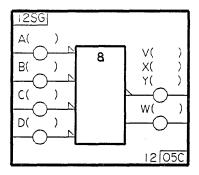




BIAS LØ = S(O-3) BIAS HI = NØNE

OPERATIONAL DESCRIPTION

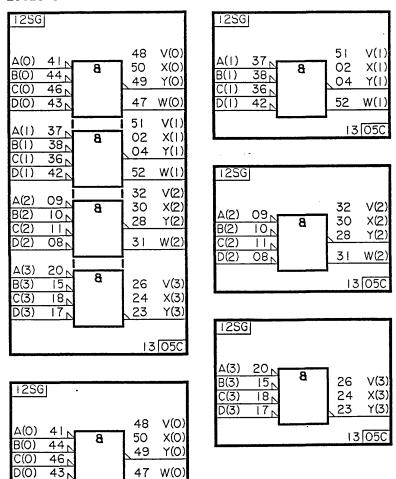
The Z(0) output is the active LO result of an 8-bit OR function. Output Z(1) is the active HI result of the OR function.



BIAS LØ = NØNE BIAS HI = F, S(O-3)

OPERATIONAL DESCRIPTION

Outputs V, X, and Y are three copies of the active LO highwayed result (A \bullet B \bullet C \bullet D). Output Z is the active HI highwayed result.



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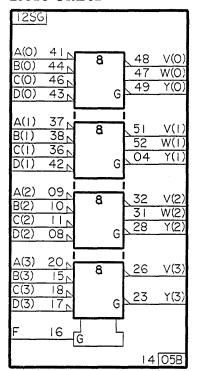
BIAS LØ = NØNE BIAS HI = F, S(0-3)

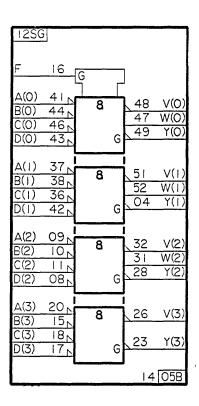
OPERATIONAL DESCRIPTION

(None required).

12SG-14 AND Gates.

LOGIC SYMBOL

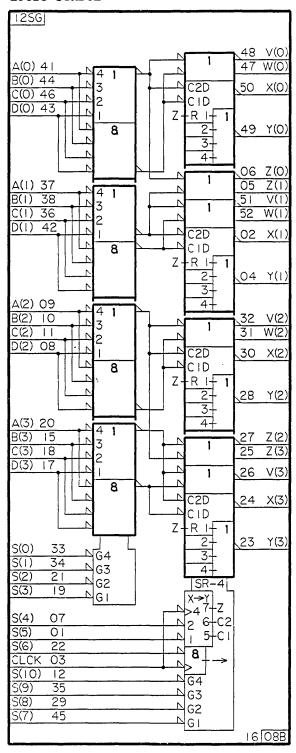




BIAS LØ = NØNE BIAS HI = S(O-10)

OPERATIONAL DESCRIPTION

Pin F gates the AND results to the Y output pins.



BIAS LØ = F BIAS HI = NØNE

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12SG-16 (Cont'd)

OPERATIONAL DESCRIPTION

Each bit of the shift register (SR-4) has two inputs, one from the four-input mux and one from the AND of the same 4 bits.

Pins S(4), S(5), and CLCK control the upper (first) rank of the shift register. A translation of 5 selects and clocks the AND data, 6 selects and clocks the mux data, and 7 clears the upper rank.

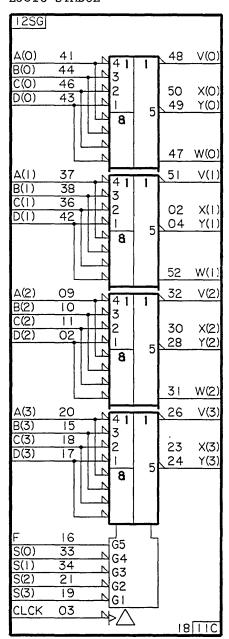
When pin S(6) is LO and clock (pin CLCK) goes LO, a right (down) shift of one takes place. The contents of the upper rank shift down to the second rank and the contents of the second rank shift down to the third rank etc. If a load of the first rank occurs at the same time as a shift, the new data is loaded and the previous data are shifted.

Each bit of the shift register has two outputs. The X outputs are always the output of the first rank. The Y outputs are controlled by pins S(7-10) and are the mux of any or all of the four ranks of the shift register. If more than one select signal is active (LO) at the same time, the contents of the selected ranks are ORed to the Y outputs.

The V, W, and Z outputs are from OR functions which have nothing to do with the shift register. Each of their OR functions receives the same two inputs as the shift register and ORs them together.

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NØTE: A THE X(O-3) ØUTPUTS ØF THE SG TYPE 18 RELY ØN THE RESET STATE ØF AN INTERNAL REGISTER. THE CØNNECTIØN ØF THE CLCK INPUT TØ A CLØCK SIGNAL INSURES THE RESET STATE ØF THAT REGISTER. ØNLY ØNE CLØCK PULSE IS NEEDED.

BIAS LØ = S(4-5)BIAS HI = S(6-10)

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12SG-18 (Cont'd)

OPERATIONAL DESCRIPTION

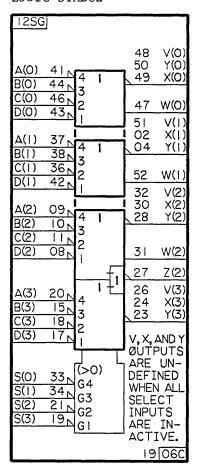
The outputs come from OR functions. Each of these OR functions has two inputs, a four-input mux and an AND of the same four inputs.

Pin F gates the X and Y outputs.

Clock must be connected to the 12SG-18 to clear an internal register. This register is not shown but the clock input (pin CLCK) is. Refer to the note below the symbol.

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BIAS LØ = NØNE BIAS HI = F

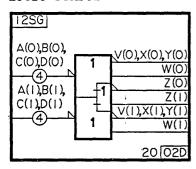
OPERATIONAL DESCRIPTION

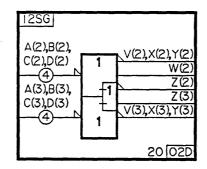
The V, Y, X, and W outputs are fed by four-input muxes controlled by pins S(0-3). The (>0) symbol located above the G modifier in the common control block is a coincident input modifier. It indicates that at least one control input must be active or the outputs are undefined.

Pin Z(2) is the output of an OR of the selected inputs from the two lower muxes.

12SG-20 Four/Eight-Input OR.

LOGIC SYMBOL





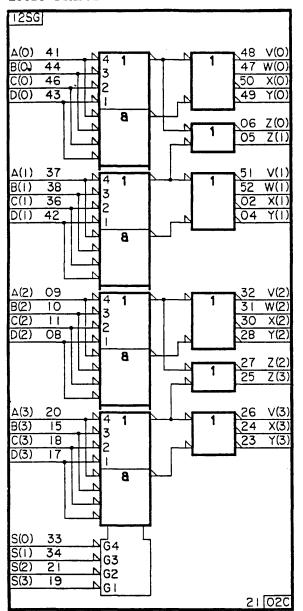
BIAS LØ = S(O-3)BIAS HI = F

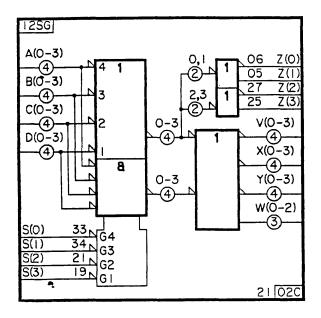
OPERATIONAL DESCRIPTION

Each symbol contains three OR gates. The top and bottom gates each OR 4 bits together. The center gate ORs the results of the top and bottom gates.

The active LO result from each 4-bit OR gate is fanned out on three pins.

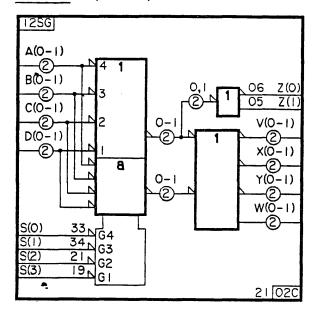
LOGIC SYMBOL

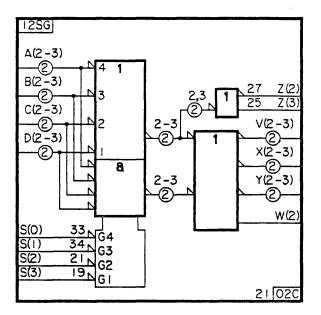




BIAS LØ = NØNE BIAS HI = F

12SG-21 (Cont'd)





BIAS LØ = NØNE BIAS HI = F

12SG-21 (Cont'd)

OPERATIONAL DESCRIPTION

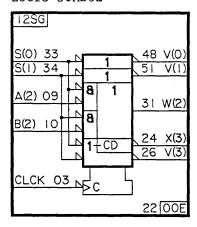
The V, W, X, and Y outputs come from OR functions each with two inputs, a mux of four inputs and an AND of the same four inputs.

The Z outputs come from OR functions each with two inputs.

Pins Z(0-1) are fed by an OR of the 2 most-significant bits from the mux.

Pins Z(2-3) are fed by an OR of the 2 least-significant bits from the mux.

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BIAS LØ = A(O), A(3), B(I), B(3), F, S(4), S(7) BIAS HI = A(I), B(O), D(O-3), S(2), S(5), S(8-IO)

OPERATIONAL DESCRIPTION

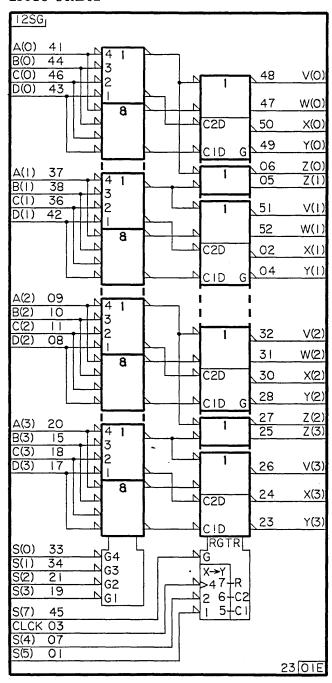
Pins V(0) and V(1) are outputs from 1-input OR functions.

Pin W(2) is the output from an OR of 2 ANDs.

Pin X(3) is the output from a flip-flop fed by a 2-input OR and clocked by pin CLCK.

Pin V(3) is the output from the same 2-input OR which feeds the flip-flop.

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BIAS LØ = F BIAS HI = S(6), S(8), S(9), S(10)

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12SG-23 (Cont'd)

OPERATIONAL DESCRIPTION

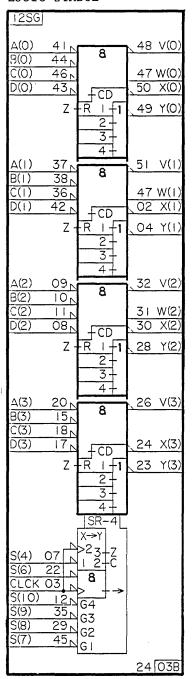
Pins V, W, and Z are the result of OR functions. Pins X and Y are the contents of a register. Pin S(7) gates the contents of the register to the Y outputs.

Each bit of the register has two inputs, one from a four-input mux and one from the AND of the same four inputs.

Pins S(4), S(5), and CLCK control the register. A control translation of 5 selects and clocks the results of the AND gates into the register, 6 selects and clocks the mux result into the register, and 7 clears the register.

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BIAS LØ = S(5), F BIAS HI = S(0-3)

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12SG-24 (Cont'd)

OPERATIONAL DESCRIPTION

Each bit of the shift register is fed by a four-input AND gate.

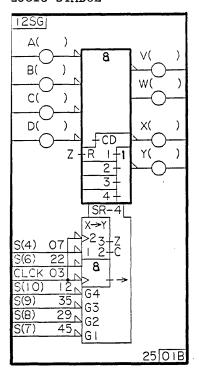
Pins S(4) and CLCK control the upper (first) rank of the shift register. A translation of 2 clocks the AND results into the upper rank. A translation of 3 clears the upper rank.

When pin S(6) is LO and clock (pin CLCK) goes LO, a right (down) shift of 1 takes place. The contents of the upper rank shift down to the second rank and the contents of the second rank shift down to the third rank etc. If a load of the first rank occurs at the same time as a shift, the new data is loaded and the previous contents are shifted.

Each bit of the shift register has 2 outputs (X and Y). The X outputs are the outputs from the first rank. The Y outputs are controlled by pins S(7-10) and are the mux of any or all of the 4 ranks of the shift register. If more than 1 select signal is active (LO) at the same time, the contents of the selected ranks are ORed to the output highway.

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BIAS LØ = S(5), F BIAS HI = S(0-3)

OPERATIONAL DESCRIPTION

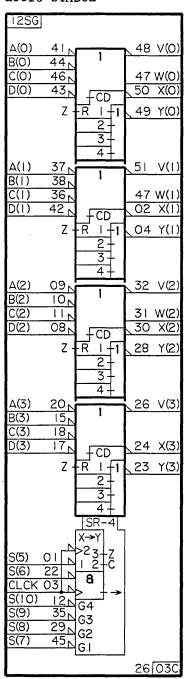
The shift register is fed by the AND of four input highways. Outputs highways V and W are also results of the AND.

Pins S(4) and CLCK control the upper (first) rank of the shift register. A translation of 2 clocks the AND result into the upper rank. A translation of 3 clears the upper rank.

When pin S(6) is LO and clock (pin CLCK) goes LO, a right (down) shift of one takes place. The contents of the upper rank shift down to the second rank and the contents of the second rank shift down to the third rank etc. If a load of the first rank occurs at the same time as a shift, the new data is loaded and the previous contents are shifted.

The shift register has two highwayed outputs. The upper highway is always the output of the first rank. The lower output highway is controlled by pins S(7-10) and is the mux of any or all of the 4 ranks of the shift register. If more than 1 select signal is active (LO) at the same time, the contents of the selected ranks are ORed to the output highway.

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BIAS LØ = S(O-4), F BIAS HI = NØNE

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12SG-26 (Cont'd)

OPERATIONAL DESCRIPTION

Each bit of the shift register is fed by a four-input OR gate.

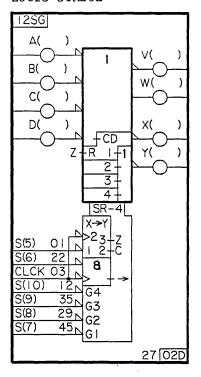
Pins S(4) and CLCK control the upper (first) rank of the shift register. A translation of 2 clocks the OR results into the upper rank. A translation of 3 clears the upper rank.

When pin S(6) is LO and clock (pin CLCK) goes LO a right (down) shift of 1 takes place. The contents of the upper rank shift down to the second rank and the contents of the second rank shift down to the third rank etc. If a load of the first rank occurs at the same time as a shift, the new data is loaded and the previous contents are shifted.

Each bit of the shift register has 2 outputs (X and Y). The X outputs are the outputs from the first rank. The Y outputs are controlled by pins S(7-10) and are the mux of any or all of the 4 ranks of the shift register. If more than 1 select signal is active (LO) at the same time, the contents of the selected ranks are ORed to the output highway.

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NØTE: 12SG TYPES 31 AND 32 USE THE SAME BIAS.

BIAS LØ = S(0-4), F BIAS HI = NØNE

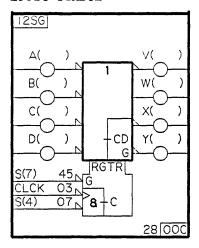
OPERATIONAL DESCRIPTION

The shift register is fed by OR of four input highways. Outputs highways V and W are also results of the OR.

Pins S(4) and CLCK control the upper (first) rank of the shift register. A translation of a 2 clocks the OR result into the upper rank. A translation of 3 clears the upper rank.

When pin S(6) is LO and clock (pin CLCK) goes LO a right (down) shift of one takes place. The contents of the upper rank shift down to the second rank and the contents of the second rank shift down to the third rank etc. If a load of the first rank occurs at the same time as a shift, the new data is loaded and the previous contents are shifted.

The shift register has two highwayed outputs. The upper highway is always the output of the first rank. The lower output highway is controlled by pins S(7-10) and is the mux of any or all of the 4 ranks of the shift register. If more than 1 select signal is active (LO) at the same time, the contents of the selected ranks are ORed to the output highway.

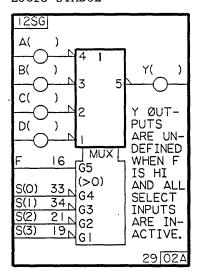


BIAS $L\emptyset = F$, S(0-3)BIAS HI = S(5-6), S(8-10)

OPERATIONAL DESCRIPTION

Output highways V and W are results of an OR of the four input highways. The OR result also feeds a register controlled by pins S(4) and CLCK.

Pin S(7) gates the contents of the register to output high Y.



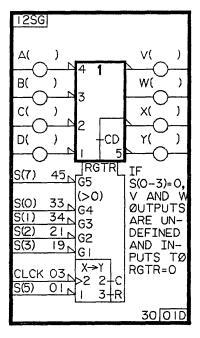
BIAS LØ = S(4-6)BIAS HI = S(7-10)

OPERATIONAL DESCRIPTION

If more than one gating modifier (G) is active at the same time an OR of the selected highways takes place.

Pin F gates the output to highway Y.

The (>0) symbol located above the G modifier in the common control block is a coincident input modifier. It indicates that at least one control input must be active or the outputs are undefined.

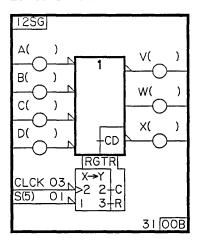


BIAS LØ = S(4), F BIAS HI = S(6), S(8-10)

OPERATIONAL DESCRIPTION

Output highways V and W and the inputs to the register are the result of a mux/OR function controlled by pins S(0-3). If more than one select signal is active at the same time, the selected input highways are ORed together. If no select signals are active, output highways V and W are undefined (denoted by > 0) and the input to the register is zero.

Pin S(7) gates the contents of the register to output highway Y.



NØTE: THIS IS THE SAME BIAS AS 12SG TYPE 27.

BIAS LØ = S(O-4), F BIAS HI = NØNE

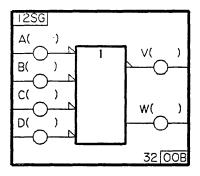
OPERATIONAL DESCRIPTION

Output highways V and W and the input to the register are the result of an OR of the 4 input highways. Output highway X is the output of the register.

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12SG-32 Highwayed OR.

LOGIC SYMBOL



NØTE: THIS IS THE SAME BIAS AS THE 12SG TYPE 27.

BIAS LØ = S(O-4), F BIAS HI = NØNE

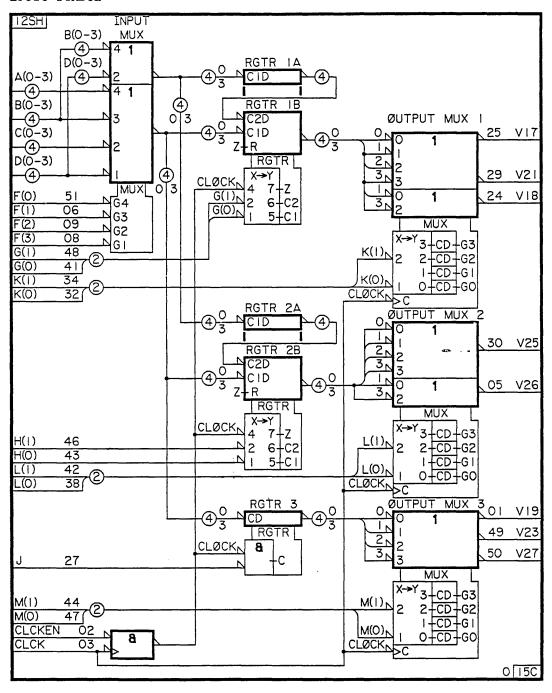
OPERATIONAL DESCRIPTION

(None required).

12SH

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	35	V01
A(1)	36	V02
A(2)	26	V03
A(3)	10	V04
B(0)	19	V05
B(1)	17	V06
B(2)	18	V07
B(3)	12	V08
C(0)	31	V09
C(1)	28	V10
C(2)	37	V11
CLCK CLCKEN	16 03 02	V12 V30 V46
D(0)	23	V13
D(1)	20	V14
D(2)	15	V15
D(3) F(0) F(1)	11 51 06	V16 V40 V41 V42
F(3) G(0) G(1)	09 08 41 48	V43 V44 V45
H(0)	43	V31
H(1)	46	V32
J	27	V33
K(0)	32	V34
K(1)	34	V35
L(0)	38	V36
L(1)	42	V37
M(0)	47	V38
M(1) V29	44 52 22	V39 V29 V47
S(0) S(1) P(0)	21 33	V47 V48 V20
P(1)	07	V24
P(2)	45	V28
V17	25	V17
V18	24	V18
V19	01	V19
V21	29	V21
V22	04	V22
V23	49	V23
V25	30	V25
V26	05	V26
V27	50	V27

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BIAS LØ = V29 BIAS HI = NØNE

12SH-0 (Cont'd)

OPERATIONAL DESCRIPTION

The 12SH-0 selects data from four 4-bit input highways, holds the selected data in any one of three data buffers, and disassembles it 1 bit per clock period through a mux on the output of each data buffer.

Input Mux

The data portion (top) of the Input Mux consists of two muxes. The top mux selects between the B and D input highways. The bottom mux selects from all four input highways. Gating modifiers G1-G4 gate the selected data through the muxes. When more than one gating modifier is active at the same time, the muxes OR the selected highways together. Inputs F(0-3) control the gating modifiers.

Clock

Clock and a clock enable signal enter the array on pins CLCK and CLCKEN respectively (lower left corner of the symbol). The two signals are ANDed to control the clocks for the registers (data buffers) in the center of the symbol. Note that the clock signal sent to the control registers in the output muxes is not ANDed with the clock enable. Thus when pin CLCKEN is HI, it disables clock to the data buffers but not to the control registers in the output muxes.

Registers 1A and 1B

These two registers form one of the three data buffers. Inputs G(0,1) along with clock are translated to control both registers.

Control translations of 0-4 do not activate any modifiers and therefore cause the registers to hold their contents.

A control translation of 5 activates clock modifier Cl. Cl clocks selected mux data into both registers.

A control translation of 6 activates C2. C2 clocks data from Register 1A into Register 1B.

A control translation of 7 activates Z which clears Register 1B.

Registers 2A and 2B

These two registers form one of the three data buffers. They operate in the same manner as Registers 1A and 1B and are controlled by inputs $\mathrm{H}(0,1)$ and clock. Registers 3

Register 3 is one of the three data buffers. Input pin J is ANDed with clock to control clock modifier C. When C is active, it clocks Input Mux data into Register 3.

Output Muxes

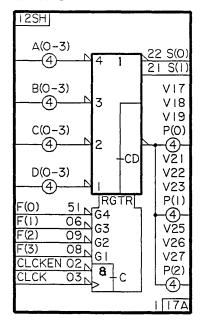
Each output mux disassembles (selects 1 bit per clock) the 4 bits held in its respective data buffer. Gating modifiers in the top OR function of each output mux select one of four bits to the mux outputs. For fanout purposes, Output Mux 1 outputs two copies of the selected bit (outputs V17 and V21) and Output Mux 3 outputs three copies of its selected bit (outputs V19, V23, and V27).

12SH-0 (Cont'd)

Output Muxes 1 and 2 also each have an additional OR function where gating modifiers select between bits 1 and 3 from their respective data buffers.

Two control signals and clock enter the common control block of each output mux. The two control signals are translated and clock clocks the translation into a register. The output of the register controls the gating modifiers.

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NØTE: THERE ARE 3 ØUTPUTS (FANØUTS) PER BIT. REFER TØ THE TABLE FØR THE ØUTPUT PIN NUMBERS.

	INPUTS	FAN	ØUT	PINS
ı	A0+B0+C0+D0	V17	V21	V25
1	AI+BI+CI+DI	V18	V22	V26
	A2+B2+C2+D2			
ı	A3+B3+C3+D3			

BIAS $L\emptyset = J$, G(O), H(O), M(I), V29BIAS HI = K(O-I), L(O-I), M(O), G(I), H(I)

OPERATIONAL DESCRIPTION

The 12SH-1 performs two functions: a mux of four 4-bit input highways to a 4-bit register, and a 4, 8, 12, or 16 input OR.

Mux/Register

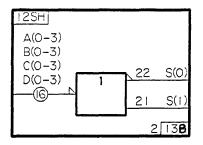
Inputs F(0-3) control gating modifiers which gate one or more 4-bit input highways to the 4-bit register. When the gating modifiers gate more than one input highway to the register, the highways are ORed together to form one 4-bit highway. Clock modifiers clock the selected data into the register. The register has three sets of outputs.

OR Function

Inputs F(0-3) control gating modifiers which gate one or more 4-bit highways into an OR function which ORs all the bits together. Output S(0) is an active LO output and S(1) is an active HI output from the OR function.

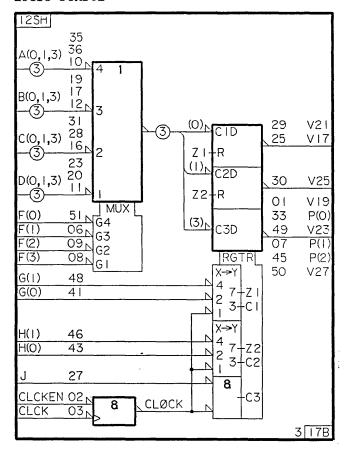
12SH-2 16 Input OR.

LOGIC SYMBOL



OPERATIONAL DESCRIPTION

(None required.)



NØTE: INPUT PINS 26, 18, 37, 15 (A(2), B(2), C(2), D(2) ARE NØT USED.)

BIAS LØ = L(O), M(O-1), V29 BIAS HI = K(O-1), L(1)

OPERATIONAL DESCRIPTION

The 12SH-3 contains two major functions, an input mux and a 3-bit register.

Input Mux

Inputs F(0-3) control gating modifiers which gate one or more input highways to the output of the mux. When the gating modifiers gate more than one input highway at the same time, the mux ORs the selected highways together.

12SH-3 (Cont'd)

Register

Each bit in the register has its own clock control and bits 0 and 1 have individual reset controls.

The CLOCK input to the register is the AND of the clock signal on pins CLCK and the clock enable signal on pin CLCKEN.

Input pins G(0,1) and CLOCK are translated to control bit 0 of the register. Translations of 0-2, 4, and 5 do not activate any modifiers and therefore cause bit 0 to hold.

A translation of 3 activates clock modifier Cl which clocks bit 0.

A translation of 7 activates Z1 which clears bit 0.

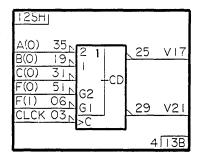
Inputs H(0,1) and CLOCK are translated to control bit 1 in the same manner as G(0,1) and CLOCK control bit 0.

Input pin J is ANDed with CLOCK to activate clock modifier C3. C3 clocks bit 3. Bit 3 has six output pins.

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12SH-4 OR/Latch.

LOGIC SYMBOL



BIAS LØ = CLCKEN, F(2), G(0-1), H(0-1), V29 BIAS HI = F(3), K(0-1)

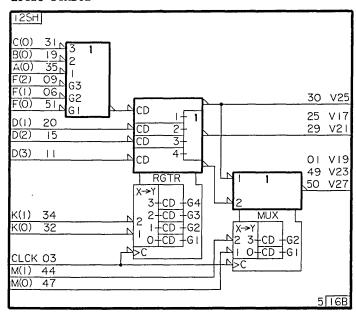
OPERATIONAL DESCRIPTION

The 12SH-4 is a three-input OR gate on the input to a latch. Two control inputs, F(0,1), control gating modifiers which gate pins A(0) and B(0) into the OR function. The equation for the input to the latch is: (A(0) AND F(0) OR (B(0) AND F(1)) OR C(0).

Clock on pin CLCK clocks the result of the OR function into the latch.

12SH-5 Register With Mux Outputs.

LOGIC SYMBOL



BIAS LØ = CLCKEN, F(3), G(0), H(0), V29 BIAS HI = A(1-3), B(1-3), C(1-3), D(0), L(0-1), H(1), G(1)

OPERATIONAL DESCRIPTION

The 12SH-5 is a 4-bit register with an OR function connected to the input of the most-significant bit and two mux functions on the register outputs.

Output pins V17 and V21 are the output of a mux which selects one of the 4 bits from the register.

Outputs V19, V23, and V27 are the output of a mux which selects between the most and least-significant bits from the register.

OR Function

Input pins F(0-2) control gating modifiers G1-G3 respectively, which gate pins A(0), B(0), and C(0) into the three-input OR function.

Register and Four-Bit Output Mux

Clock on input CLCK controls clock modifier C. C clocks the result of the OR function and inputs D(1-3) into the register. Output pin V25 is the ungated output from the most-significant bit. The least-significant bit also has an ungated output which connects to the two-bit output mux.

12SH-5 (Cont'd)

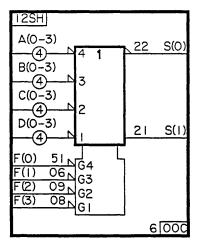
Gating modifiers G1-G4 select one of the 4 register bits through an output mux to pins V17 and V21.

Input pins K(0,1) are translated in the common control block of the register. Clock modifier C clocks the result of the translation into a control register which controls gating modifiers G1-G4.

Two-Bit Output Mux

Input pins M(0,1) are translated in the common control block of the 2-bit output mux. Clock modifier C clocks translations of 0 and 3 into a 2-bit control register which controls gating modifiers Gl and G2. Translations of 1 and 2 are not used, therefore the outputs of the mux are HI for those translations.

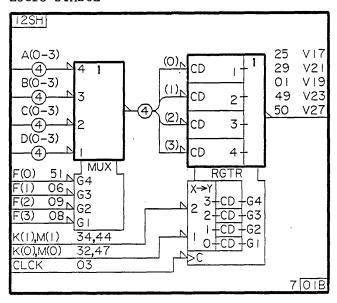
60458120 F



BIAS NONE

OPERATIONAL DESCRIPTION

Inputs F(0-3) control gating modifiers which gate one or more 4-bit highways into an OR function which ORs all the bits together. Output S(0) is an active LO output and S(1) is an active HI output from the OR function.



BIAS LØ = G(O), H(O), CLCKEN, J, V29 BIAS HI = G(I), H(I)

OPERATIONAL DESCRIPTION

The 12SH-7 is a 4-bit register with a 4-highway mux on its input and a 4-bit mux on its output.

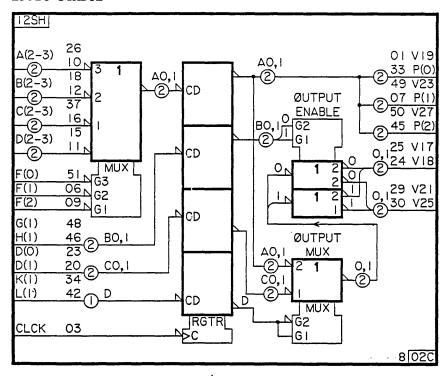
Input Mux

Inputs F(0-3) control gating modifiers which gate one or more input highways to the output of the mux. When the gating modifiers gate more than one input highway at the same time, the mux ORs the selected highways together.

Register and Output Mux

Clock on input CLCK controls clock modifier C. C clocks data into the register. Gating modifiers G1-G4 select one of the 4 register-bits through an output mux to pins V17, V21, V19, V23, and V27.

Two signals control the output mux. One control signal connects to input pins K(1) and M(1). The other connects to pins K(0) and M(0). The two control signals are translated in the common control block of the register. Clock modifier C clocks the result of the translation into a control register which controls gating modifiers G1-G4.



BIAS LØ = V29, F(3), L(0), M(1), CLCKEN, G(0), H(0), J BIAS HI = A(0-1), B(0-1), C(0-1), K(0), M(0).

OPERATIONAL DESCRIPTION

The 12SH-8 consists of four registers, designated A-D, with an input mux for Register A, an Output Mux, and an Output Enable function.

Input Mux

The D(2,3) input highway enters the input mux ungated. Therefore when gating modifiers G1-G3 enable any of the other three input highways, the selected highways are ORed with the D(2,3) inputs. Input pins F(0-2) control gating modifiers G3-G1 respectively.

Registers

Clock enters the array on pin CLCK and clocks all four registers.

Output Mux

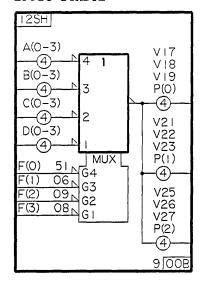
The output of register D selects between the ouptuts from registers A and C. When D is LO, G2 is active and selects register A. When D is HI, G1 is active and selects Register C.

12SH-8 (Cont'd)

Output Enable

The outputs from register B enable the Output Mux outputs to the V17, V18, V21 and V25 outputs. When register B bit 0 is HI, G2 is active and enables output bits 0 and 1 to output pins V17 and V18 respectively. G2 also enables bit 0 to output to V21. When register B bit 1 is HI, G1 is active and enables output bit 1 to output to V25.

60458120 B 2 of 2



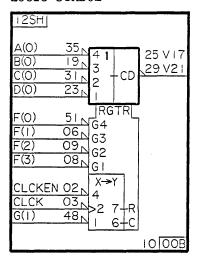
NØTE: THERE ARE 3 ØUTPUTS (FANØUTS) PER BIT. REFER TØ THE TABLE FØR THE ØUTPUT PIN NUMBERS.

INPUTS	FAN	ØŬT	PINS
AO+BO+CO+DO	V17	V21	V25
AI+BI+CI+DI	V18	V22	V26
A2+B2+C2+D2	V19	V23	V27
A3+B3+C3+D3	P(0)	P(1)	P(2)

BIAS $L\emptyset$ = CLCKEN, CLCK, J, G(O), H(O), M(I) BIAS HI = K(O-I), L(O-I), M(O), G(I), H(I), V29

OPERATIONAL DESCRIPTION

Inputs F(0-3) control gating modifiers which gate one or more input highways to the output of the mux. When the gating modifiers gate more than one input highway at the same time, the mux ORs the selected highways together. The mux has three sets of outputs.



BIAS $L\emptyset = J$, G(O), H(O), M(I), V29BIAS HI = K(O-I), L(O-I), H(I), M(O)

OPERATONAL DESCRIPTION

Input Mux

Inputs F(0-3) control gating modifiers which gate one or more input highways to the input of the register. When the gating modifiers gate more than one input highway at the same time, the mux ORs the selected highways together.

Register

Clock enters the array on pin CLCK, a clock enable signal enters on pin CLCKEN, and a reset enable signal enters on pin G(1). All three signals are translated to control the register.

Translations of 0-5 activate no modifiers and therefore cause the register to hold.

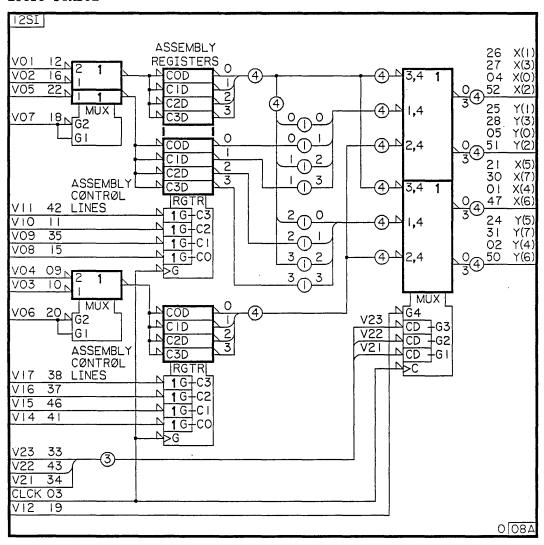
A translation of 6 activates clock modifier C which clocks selected data into the register.

A translation of 7 clears the register.

12SI

ļ	PIN	REAL	VIRT
	NAME	PIN	PIN
	CLCK	03	V19
	V01	12	V01
	V02	16	V02
	V03	10	V03
	V04	09	V04
	V05	22	V05
	V06	20	V06
	V07	18	V07
	V08	15	V08
	V09	35	V09
	V10	11	V10
	V11	42	V11
	V12	19	V12
	V13	07	V13
	V14	41	V14
	V15	46	V15
	V16	37	V16
	V17	38	V17
	V18	08	V18
	V20 V21 V22	17 34 43 33	V20 V21 V22
	V23 V24 V25 V26	45 48 44	V23 V24 V25 V26
i	V27	36	V27
	V28	32	V28
	X(0)	04	V33
	X(1)	26	V29
	X(2)	52	V35
	X(3)	27	V31
	X(4)	01	V41
	X(5)	21	V37
	X(6)	47	V43
	X(7)	30	V39
	Y(0)	05	V34
	Y(1)	25	V30
	Y(2)	51	V36
	Y(3)	28	V32
	Y(4)	02	V42
	Y(5)	24	V38
	Y(6)	50	V44
	Y(7)	31	V40
	Z(0)	06	V47
	Z(1)	23	V45
	Z(2)	49	V48
	Z(3)	29	V46

.



BIAS LØ = V18, V27 BIAS HI = V13, V20, V28, V24

			•
	•		
	•		
	•		

12SI-0 (Cont'd)

OPERATIONAL DESCRIPTION

Input Muxes

Pin V07 selects one of two inputs to the top assembly register and gates pin V05 to the second assembly register.

Pin V06 controls the input mux selection for the lower assembly register.

Assembly Registers

Pins VII, VIO, VO9, VO8, and clock (pin CLCK) control the assembly of the top 2 registers. Each clock pulse latches the selected input into the selected bit positions of each register. Bits in each assembly register are numbered 0-3 and are sent to the output muxes.

Pins V17, V16, V15, V14, and clock (pin V19) control the assembly of the bottom register.

Output Muxes

Signals entering pins V23, V22, and V21 are latched into a register (shown in the common control block of the output muxes). The register outputs and V12 control the output muxes.

G4 must be active (controlled by pin V12) in order to make any selections to either output \max .

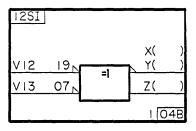
 ${\tt G3}$ and ${\tt G2}$ select the contents of the top or bottom assembly registers through the output muxes.

G1 selects a combination of bits from the upper and middle assembly registers to enter the output muxes. Bits 0 and 1 from the upper assembly register feed bits 0 and 2 of the upper output mux. Bits 0 and 1 of the middle assembly register feed bits 1 and 3 of the upper output mux. Bits 2 and 3 from the upper and middle assembly registers feed the lower output mux.

60458120 B 2 of 2

12SI-1 Exclusive OR with Fanout.

LOGIC SYMBOL



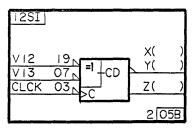
NØTE: ACTIVE HI ØUTPUT MUST BE USED ØR TERMINATED.

BIAS LØ = V26, V24 BIAS HI = V20

OPERATIONAL DESCRIPTION

12SI-2 Exclusive OR to a Flip-Flop.

LOGIC SYMBOL



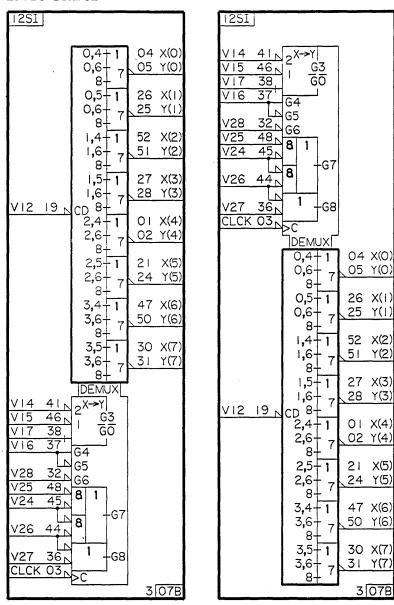
NØTE: IF USED AS A RGTR, EITHER PIN 19 ØR 7 MUST BE HIGH.

....

BIAS LØ = V18, V20, V26, V24 BIAS HI = NØNE

OPERATIONAL DESCRIPTION

LOGIC SYMBOL



BIAS LØ = V18, V20 BIAS HI = V13

•		

12SI-3 (Cont'd)

OPERATIONAL DESCRIPTION

Pin V12 is the data input pin to a flip-flop controlled by pin CLCK (clock). The contents of the flip-flop may be gated out one or more of the 8 outputs.

OR functions feed each of the 8 outputs (2 pins per output). G7 gates the contents of each OR function to the output pins.

The OR functions each have 3 inputs. The top OR function is used as an example. The top OR function will equal the contents of the flip-flop with the following active gating modifiers: $(GO \circ GA) + (GO \circ GA) + GA$.

Pin V17 inhibits the coder function which produces G0-G3. With Pin V17 HI, G0-G3 will be inactive.

60458120 B 2 of 2

		,		

12SI				
	X->Y	7	30 31	X(7) Y(7)
V14 41	4	6	47 50	X(6) Y(6)
	7	5	21 24	X(5) Y(5)
V15 46 _N	2	4	01	X(4) Y(4)
V16 37	1	3	27 28	X(3) Y(3)
	'	2	52 51	X(2) Y(2)
V17 38			26 25	X(1) Y(1)
		0	04 05	X(O) Y(O)
	l	<u></u>	4	04D

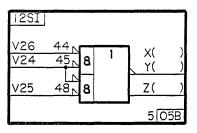
BIAS LØ = VI2, V24, V25 BIAS HI = VI3, V20, V28, V27, V26

OPERATIONAL DESCRIPTION

Pins V14, V15, and V16 are translated and activate one of eight outputs. Pin V17 is an active HI inhibit. If V17 is HI, the translation is inhibited and all outputs are inactive.

12SI-5 AND/OR Combinational Logic.

LOGIC SYMBOL



BIAS LØ = CLCK, VI2, V27 BIAS HI = VI3, VI8, V20, V23, V21, V22

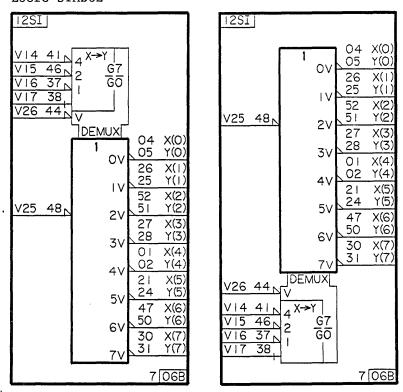
OPERATIONAL DESCRIPTION

12SI				
	X -> Y	7	30 31	X(7) Y(7)
V14 41	4	6	47 50	X(6) Y(6)
	'	5	21 24	X(5) Y(5)
V15 46 _N	2	4	01 02	X(4) Y(4)
V16 37	1	l	27 28	X(3) Y(3)
	'	3	29	Z(3) X(2)
V17 38		2	52 51 49	Y(2)
		2		Z(2) X(1)
		1	26 25 23	Y(1) Z(1)
		1	04	X(O) Y(O)
		0	06	Z(O)
			6	04C

BIAS LØ = V12, V24, V25 BIAS HI = V13, V20, V28, V27, V26

OPERATIONAL DESCRIPTION

Pins V14, V15, and V16 are translated and activate one or more of the outputs. If the inputs translate to 0, 1, 2, or 3, both active L0 and active HI outputs are produced. Translations of 4-7 produce only active L0 outputs.



BIAS LØ = CLCK, V20, V12, V24 BIAS HI = V13, V18, V28, V23, V21, V27, V22

OPERATIONAL DESCRIPTION

Pin V25 feeds an OR function whose contents are gated to one of eight outputs.

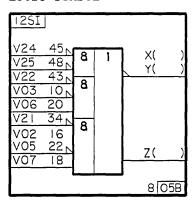
Pins V14, V15, and V16 select one of eight outputs.

Pin V17 is an active HI inhibit to the translation. If pin V17 is HI, GO-G7 are all inactive.

Pin V26 is the input to a V (OR) modifier. If V is active all outputs are forced active.

12SI-8 AND/OR Combinational Logic.

LOGIC SYMBOL



BIAS LØ = CLCK, VIO, VO8, VI2, V28, VO9, V27, VI6, VI7, VI4, VII, VI5
BIAS HI = VI3, VI8, VO4, VOI, V23, V26

OPERATIONAL DESCRIPTION

12SI-9 Two-Input Exclusive OR with a Fanout.

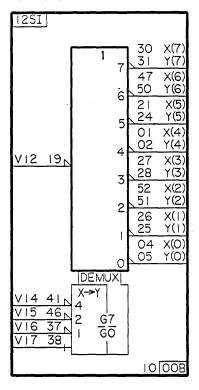
LOGIC SYMBOL

12SI				
			2 6	X(1)
		=1	26 25 27 28 04	Y(1)
	1		27	X(3) Y(3)
			28	Y(3)
			04	X(O)
V12	19		05	Y(O)
			52 51 21	X(2)
			$\frac{51}{2}$	Y(2)
1			21	X(5)
	~~		24	Y(5)
V13	07		30	X(7)
			 	Y(7) X(4)
			02	$\frac{\Lambda(4)}{\Upsilon(4)}$
			47	X(6)
			50	Y(G)
			23	Z(1)
		:	30 31 01 02 47 50 23 29 06	Z(3)
			06	Z(0)
			49	Z(1) Z(3) Z(0) Z(2)
	į		,	
			9	05B

NØTE: ACTIVE HI ØUTPUT MUST BE USED ØR TERMINATED.

BIAS LØ = V24, V26 BIAS HI = V20

OPERATIONAL DESCRIPTION



BIAS LØ = V24, V25 BIAS HI = CLCK, V13, V20, V28, V27, V26

OPERATIONAL DESCRIPTION

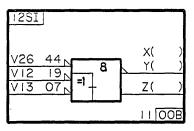
Pin V12 feeds an OR function which is gated to one of eight outputs.

Pins V14, V15, and V16 select one of eight outputs.

Pin V17 is an active HI inhibit to the translation. If pin V17 is HI, GO-G7 are all inactive.

12SI-11 Exclusive OR/AND Combinational Logic with a Fanout.

LOGIC SYMBOL



NØTE: ACTIVE HI ØUTPUT MUST BE USED ØR TERMINATED.

OPERATIONAL DESCRIPTION

There are 16 active LO outputs, X(0-7), Y(0-7), and 4 active HI outputs, Z(0-3).

12SI		-	
V26 44 _N	1	26 25 27 28 04 05 52 51 21	X(1) Y(1) X(3) Y(3) X(0) Y(0) X(2) Y(2) X(5)
V27 36 _N		21 24 30 31 01 02 47 50 23 29 06 49	X(7) Y(7) X(4) Y(4) X(6) Y(6) Z(1) Z(3) Z(0)
			Z(2)

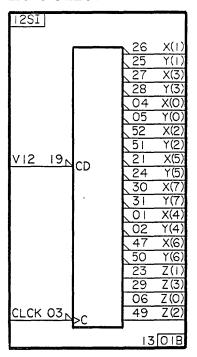
NØTE: ACTIVE HI ØUTPUT MUST BE USED ØR TERMINATED.

BIAS LØ = V24, V25, V12 BIAS HI = V13, V20, V17

OPERATIONAL DESCRIPTION

12SI-13 Flip-Flop with a Fanout.

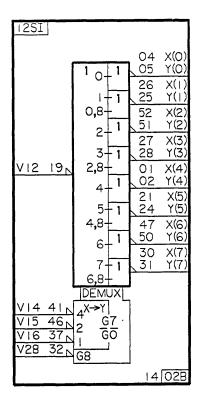
LOGIC SYMBOL



NØTE: ACTIVE HI ØUTPUT MUST BE USED ØR TERMINATED.

BIAS LØ = V24, V26, V18, V20 BIAS HI = V13

OPERATIONAL DESCRIPTION



BIAS LØ = V17, V24, V25 BIAS HI = V13, V20, V27, V26

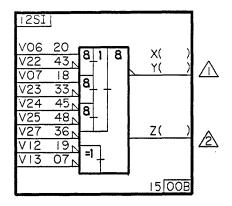
OPERATIONAL DESCRIPTION

Pin V12 feeds an OR function whose output is gated to one or more outputs.

Pins V14, V15, V16, and V28 control the output selection.

Each output is fed by a one or two input OR function. The top two OR functions serve as examples:

Output pins X(0) and $Y(0) = V12 \bullet G0$. Output pins X(1) and $Y(1) = (V12 \bullet G1) + (V12 \bullet G0 \bullet G8)$.



NØTES: ACTIVE LØ ØUTPUTS ARE X(0-6) AND Y(0-6).

ACTIVE HI ØUTPUTS ARE Z(0-3).

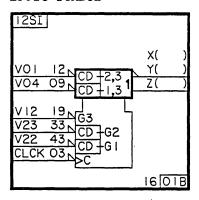
BIAS LØ = CLCK, VO3, VIO, VO8, VO2, VO9,

VI6, VI7, VI4, VII, VI5

BIAS HI = VI8, VO4, VOI, V28, V21, V26

OPERATIONAL DESCRIPTION

The outputs are fed by a three-input AND function. The top input to this AND function is from an OR of three ANDs. The middle input is from pin V27. The bottom input is from a two-input exclusive OR.



BIAS LØ = V06-11, V14-18, V27 BIAS HI = V13, V20, V21, V24, V28

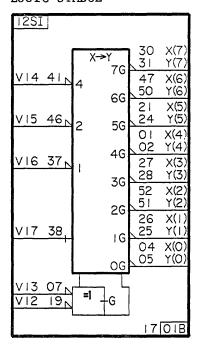
OPERATIONAL DESCRIPTION

Pins V01 and V04 are inputs to separate flip-flops. The contents of these two flip-flops enter a mux.

Signals entering pins V23, and V22 are latched into a register (shown in the common control block). The register outputs and V12 controls the selection of the mux.

G2 and G3 must both be active to gate the contents of the top flip-flop to the outputs. G1 and G3 must both be active to gate the contents of the bottom flip-flop to the outputs.

If all three gating modifiers are active at the same time, the contents of the two data flip-flops are ORed to the outputs.

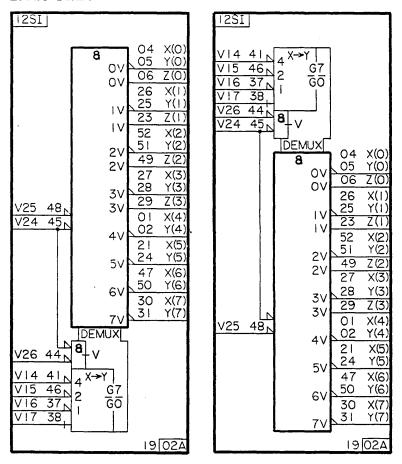


BIAS LØ = V24, V25 BIAS HI = V20, V28, V27, V26

OPERATIONAL DESCRIPTION

The three data input pins, V14, V15, and V16, are translated and select one of eight outputs. Gating modifier G gates the output of the translation.

Pin V17 is an active HI inhibit. If pin V17 is HI all translation outputs are inactive.



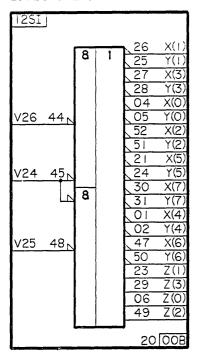
BIAS LØ = CLCK, V20, V12 BIAS HI = V13, V18, V28, V23, V21, V27, V22

OPERATIONAL DESCRIPTION

Input pins V25 and V24 are ANDed together and the result is gated to one of eight outputs.

Pins V14, \cdot V15, and V16 are translated and select the output. Pin V17 is an active HI inhibit. If pin V17 is HI the translation outputs are inactive and all gating modifiers (G0-G7) are inactive.

Pins V24 and V26 are ANDed together to control the OR modifier V. If V is active all outputs are forced active.



BIAS LØ = CLCK, V12, V27 BIAS HI = V13, V18, V20, V23, V21, V22

OPERATIONAL DESCRIPTION

1251					
		X-	→Y 7∨	30 31	X(7) Y(7)
V14	41	4	6V	47 50	X(6) Y(6)
			5v	21 24	X(5) Y(5)
V 15	46,	2	4V	01 02	X(4) Y(4)
V16	37 _N	,		27 28	X(3) Y(3)
		ļ '	3∨ 3∨	29 52	Z(3) X(2)
V27	36 _N	٧	2V 2V	51 49	Y(2) Z(2)
			۷ ا	26 25	X(1) Y(1)
			İV	23 04	Z(1) X(0)
			0V 0V	05 06	Y(O) Z(O)
			00	21	OIB

BIAS LØ = V12, V17, V24, V25 BIAS HI = V13, V20, V28, V26

OPERATIONAL DESCRIPTION

Pins, V14, V15, and V16, are translated and activate one or more of the outputs. If the inputs translate to 0, 1, 2, or 3, both active LO and active HI outputs are produced. Translations of 4-7 produce only active LO outputs.

Pin V27 controls the OR modifier V. If V is active, all outputs are forced active.

12SI-22 AND Gate.

LOGIC SYMBOL

12SI			
		N 26	X(1)
	8	25	Y(1)
		27	X(3)
		28	Y(3)
		04	X(O)
V26 44 _N		05	Y(O)
		52	X(2)
		$\sqrt{51}$	Y(2)
		21	X(5)
		24	Y(5)
		30	X(7)
		15/	Y(7)
		01	X(4)
V24 45		47	Y(4) X(6)
V24 45 _N		50	X(6)
		23	7(1)
		29	7(3)
		06	7(0)
		26 25 27 28 04 05 52 51 24 30 31 01 02 47 50 23 29 06 49	Y(6) Z(1) Z(3) Z(0) Z(2)
		 	
		22	ООВ

NØTE: ACTIVE HI ØUTPUT MUST BE USED ØR TERMINATED.

BIAS LØ = CLCK, V12, V27 BIAS HI = V13, V18, V20, V21, V22, V23, V25

OPERATIONAL DESCRIPTION

(None required.)

12\$I]		
	1 0V 0V	04 X(0) 05 Y(0) 06 Z(0) 26 X(1)
	V V	26 X(1) 25 Y(1) 23 Z(1) 52 X(2) 51 Y(2) 49 Z(2)
	2V 2V	49 Z(2) 27 X(3) 28 Y(3)
V17 38 _N	3V 3V	29 7(3)
	4٧	2 I X(5)
	5V	24 Y(5) 47 X(6) 50 Y(6)
	6V	30 X(7) 31 Y(7)
V14 41 _N	DEMUX	
V15 46 V16 37 V26 44 V27 36	4 X→1 2 G7 1 G0	
V26 44N V27 36N	1 + ∨	
L		23 00B

BIAS LØ = CLCK, V12, V24, V25 BIAS HI = V13, V18, V20, V21, V22, V23, V28

OPERATIONAL DESCRIPTION

Pin V17 feeds an OR function which is gated to one or more of the outputs.

Pins V14, V15, and V16 select one of eight G modifiers. The selected G modifier gates the contents of the OR function to one or more outputs. G0-G3 gate both active LO and active HI outputs. G4-G7 gate only active LO outputs.

Pins V26 and V27 are ORed together to control the OR modifier V. If V is active, all outputs are forced active.

		•	•	

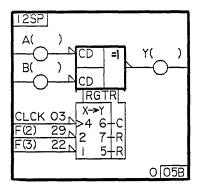
12SP

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	19	V01
A(1)	16	V02
A(2)	35 34	V03 V04
A(3)	34	V04
A(4)	45	V05
A(5)	46	V06
B(0)	12	V13
B(1)	09	V14
B(2)	33	V15
B(3)	32	V16
B(4)	37	V17
B(5)	38	V18
C(0)	18	V07
C(1)	11	V08
C(2)	15	V09
C(3)	27 01	V10 V11
C(5)	42	V12
CLCK	03	V48
D(0)	20	V19
D(1)	21	V20
D(2)	28	V21
D(3)	36	V22
D(4)	43	V23
D(5)	44	V24
F(0)	17	V44
F(1)	41	V45
F(2)	29	V46
F(3)	22	V47
F(4)	10	V30
M(0)	08	V25
M(1)	05 04	V26 V27
N(1)	02 51	V28 V29
X(4) X(5)	47	V29 V43
Y(0)	24	V31
Y(1)	23	V32
Y(2)	31	V33
Y(3)	25	V34
Y(4)	48	V35
Y(5)	49	V36
Z(0)	07	V37
Z(1)	06	V38
Z(2)	26	V39
Z(3)	30	V40
Z(4)	52	V41
Z(5)	50	V42

	• .		·

12SP-0 Registers to an Exclusive OR.

LOGIC SYMBOL



BIAS LØ = F(4), F(1)BIAS HI = F(0)

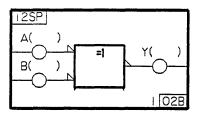
OPERATIONAL DESCRIPTION

Clock on pin CLCK and control inputs F(2,3) are translated to control the registers. Translations of 0-4 activate no modifiers and therefore cause the registers to hold. Translations of 5 or 7 clear the registers.

A translation of 6 clocks the A and B highways into their respective registers. The output of the registers passes through an exclusive OR to output highway Y.

12SP-1 Exclusive OR.

LOGIC SYMBOL



NØTE: THIS CIRCUIT IS AVAILABLE IN MØDE I ØR MØDE 4 BIAS CØNDITIØNS.

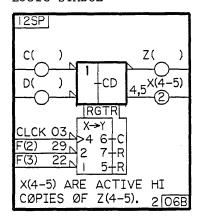
MØDE I - BIAS LØ = F(1-2), CLCK BIAS HI = F(0), F(3-4)MØDE 4 - BIAS LØ = CLCK, F(0)BIAS HI = F(1-4)

OPERATIONAL DESCRIPTION

Y(N) = A(N) exclusive OR B(N).

12SP-2 OR to a Register.

LOGIC SYMBOL



BIAS LØ = F(1), F(4)BIAS HI = F(0)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control inputs F(2,3) are translated to control the register.

Translations of 0-4 activate no modifiers and therefore cause the register to hold.

Translations of 5 or 7 clear the register.

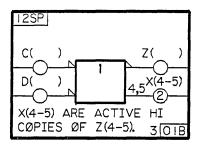
A translation of 6 clocks the result of the OR function into the register. Z(N) = C(N) OR D(N).

There is an active LO output for each bit in the register. There are active HI outputs only for the 2 least-significant bits.

60458120 B

12SP-3 OR.

LOGIC SYMBOL



NØTE: THIS CIRCUIT IS AVAILABLE IN MØDE I ØR MØDE 7 BIAS CØNDITIØNS.

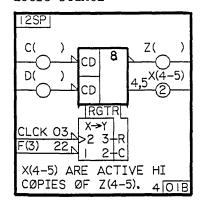
MØDE I - BIAS LØ = F(I-2), CLCK
BIAS HI = F(O), F(3-4)
6 CØPIES PER ARRAY X-ØUTPUT ØN-2 CØPIES

MØDE 7 - BIAS LØ = CLCK, F(O), F(I)
BIAS HI = F(2-4)
2 CØPIES PER ARRAY NØ X-ØUTPUT

OPERATIONAL DESCRIPTION

Z(N) = C(N) OR D(N).

There is an active LO output for each OR gate. There are active HI outputs only for the 2 least-significant OR gates.



BIAS LØ = F(0), F(4)BIAS HI = F(1-2)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control input F(3) are translated to control the registers.

Translations of 0 or 1 activate no modifiers and therefore cause the registers to hold.

A translation of 2 clocks the C and D highways into their respective registers.

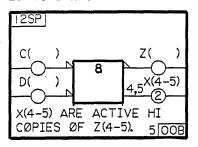
A translation of 3 clears the registers.

The register outputs pass through AND functions on the in way to output highway Z. Z(N) = C(N) AND D(N).

There is an active LO output for each AND gate. There are active HI outputs only for the two least-significant AND gates.

12SP-5 AND.

LOGIC SYMBOL



BIAS LØ = F(0), CLCK BIAS HI = F(1-4)

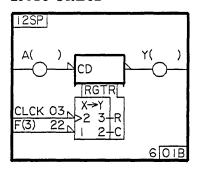
OPERATIONAL DESCRIPTION

Z(N) = C(N) AND D(N).

There is an active LO output from each AND gate. There are active HI outputs only for the two least-significant AND gates.

12SP-6 Register.

LOGIC SYMBOL



NØTE: THIS CIRCUIT IS AVAILABLE IN MØDE 5 ØR MØDE 6 BIAS CØNDITIØNS.

MØDE 5 - BIAS LØ = F(O), F(2), F(4) BIAS HI = F(I) 4 CØPIES PER ARRAY - A(2-5) MØDE 6 - BIAS LØ = F(O-2), F(4) BIAS HI = NØNE 6 CØPIES PER ARRAY - A(O-5)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control input F(3) are translated to control the register.

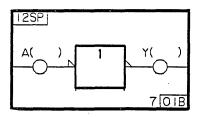
Translations of 0 or 1 activate no modifiers and therefore cause the register to hold.

A translation of 2 clocks the register.

A translation of 3 clears the register.

12SP-7 Fanout.

LOGIC SYMBOL



NØTE: THIS CIRCUIT IS AVAILABLE IN MØDE 5 ØR MØDE 6 BIAS CØNDITIØNS.

MØDE 5 - BIAS LØ = F(O), F(2), CLCK BIAS HI = F(I), F(3-4) 4 CØPIES PER ARRAY - A(2-5)

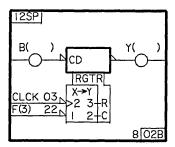
MØDE 6 - BIAS LØ = F(0-2), CLCK BIAS HI = F(3-4) 6 CØPIES PER ARRAY - A(0-5)

OPERATIONAL DESCRIPTION

Y(N) = A(N).

12SP-8 Register.

LOGIC SYMBOL



NØTE: THIS CIRCUIT IS AVAILABLE IN MØDE 5 AND MØDE 7 BIAS CØNDITIØNS.

MØDE 5 - BIAS LØ = F(O), F(2), F(4) BIAS HI = F(I) 2 CØPIES PER ARRAY - B(O-I) MØDE 7 - BIAS LØ = F(O-I), F(4) BIAS HI = F(2) 4 CØPIES PER ARRAY - B(2-5)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control pin F(3) are translated to control the register.

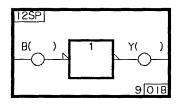
Translations of 0 or 1 activate no modifiers and therefore cause the register to hold.

A translation of 2 clocks the register.

A translation of 3 clears the register.

12SP-9 Fanout.

LOGIC SYMBOL



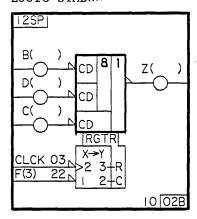
NØTE: THIS CIRCUIT IS AVAILABLE IN MØDE 5 AND MØDE 7 BIAS CØNDITIØNS.

MØDE 5 - BIAS LØ = F(0), F(2), CLCK BIAS HI = F(1), F(3-4) 2 CØPIES PER ARRAY - B(0-1)

MØDE 7 - BIAS LØ = F(O-I). CLCK BIAS HI = F(2-4) 4 CØPIES PER ARRAY - B(2-5)

OPERATIONAL DESCRIPTION

Y(N) = B(N).



BIAS LØ = F(O-2), F(4) BIAS HI = NØNE 2 CØPIES PER ARRAY - B(O-1), D(O-1), C)-1), Z(O-1)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control input F(3) are translated to control the registers.

Translations of 0 or 1 activate no modifiers and therefore cause the registers to hold.

A translation of 2 clocks the B, C, and D highways into their respective registers.

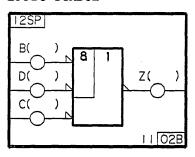
A translation of 3 clears the registers.

The outputs of the registers pass through AND/OR logic.

Z(N) = (B(N) AND D(N)) OR C(N).

12SP-11 AND/OR Logic.

LOGIC SYMBOL



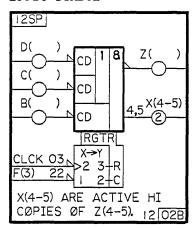
BIAS LØ = F(O-2), CLCK BIAS HI = F(3-4) 2 CØPIES PER ARRAY - B(O-1), C(O-1), D(O-1), Z(O-1)

OPERATIONAL DESCRIPTION

Z(N) = (B(N) AND D(N)) OR C(N).

12SP-12 Registers to AND/OR Logic.

LOGIC SYMBOL



BIAS LØ = F(0), F(2), F(4) BIAS HI = F(1) 4 CØPIES PER ARRAY - D(2-5), C(2-5), B(2-5), Z(2-5), X(4-5)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control input F(3) are translated to control the registers.

Translations of 0 or 1 activate no modifiers and therefore cause the registers to hold.

A translation of 2 clocks the B, C, and D highways into their respective registers.

A translation of 3 clears the registers.

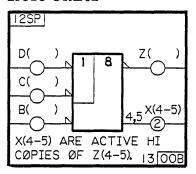
The outputs of the registers pass through AND/OR logic.

Z(N) = ((D(N) OR C(N)) AND B(N).

There is an active LO output for each result bit. There is an active HI output only for the 2 least-significant result bits.

12SP-13 OR/AND.

LOGIC SYMBOL



BIAS LØ = F(O), F(2), CLCK BIAS HI = F(I), F(3-4) 4 CØPIES PER ARRAY - D(2-5), C(2-5), B(2-5), Z(2-5), X(4-5)

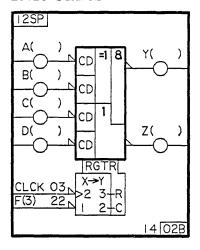
OPERATIONAL DESCRIPTION

Z(N) = (D(N) OR C(N)) AND B(N).

There is an active LO output for each result bit. There is an active HI output only for the 2 least-significant bits.

12SP-14 Registers to Exclusive OR, OR, and AND Logic.

LOGIC SYMBOL



BIAS LØ = F(O-1), F(4) BIAS HI = F(2) 2 CØPIES PER ARRAY - A(O-1), B(O-1), C(O-1), D(O-1), Z(O-1)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control input F(3) are translated to control the registers. Translations of 0 or 1 activate no modifiers and therefore cause the registers to hold.

A translation of 2 clocks the A, B, C, and D highways into their respective registers.

A translation of 3 clears the registers.

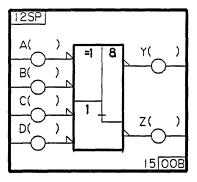
The outputs of the registers pass through the exclusive OR, OR, and AND logic.

Y(N) = [A(N) exclusive OR B(N)] AND [C(N) OR D(N)].

Z(N) = C(N) OR D(N).

12SP-15 Exclusive OR, OR, and AND Logic.

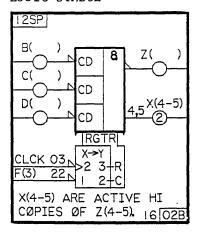
LOGIC SYMBOL



OPERATIONAL DESCRIPTION

Y(N) = [A(N) exclusive OR B(N)] AND [C(N) OR D(N)]

Z(N) = C(N) OR D(N).



BIAS LØ = F(O-2), F(4) BIAS HI = NØNE 4 CØPIES PER ARRAY - B(2-5), C(2-5), D(2-5), Z(2-5), X(4-5)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control input F(3) are translated to control the registers.

Translations of 0 or 1 activate no modifiers and therefore cause the registers to hold.

A translation of 2 clocks the B, C, and D highways into their respective registers.

A translation of 3 clears the registers.

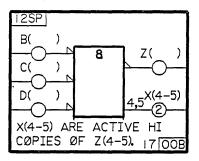
The outputs of the registers pass through the AND logic.

Z(N) = B(N) AND C(N) AND D(N).

There is an active LO output for each result bit. There are active HI outputs only for the 2 least-significant bits.

12SP-17 AND Logic.

LOGIC SYMBOL



BIAS LØ = F(O-2), CLCK BIAS HI = F(3-4). 4 CØPIES PER ARRAY - B(2-5), C(2-5), D(2-5)

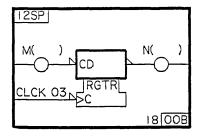
OPERATIONAL DESCRIPTION

Z(N) = B(N) AND C(N) AND D(N).

There is an active LO output for each result bit. There are active ${\tt HI}$ outputs only for the 2 least-significant bits.

12SP-18 Register.

LOGIC SYMBOL



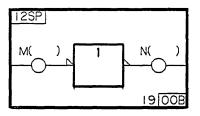
BIAS LØ = F(4) BIAS HI = NØNE 2 CØPIES PER ARRAY - M(O-I), N(O-I)

OPERATIONAL DESCRIPTION

Clock on pin CLCK clocks the M highway into the register.

12SP-19 Fanout.

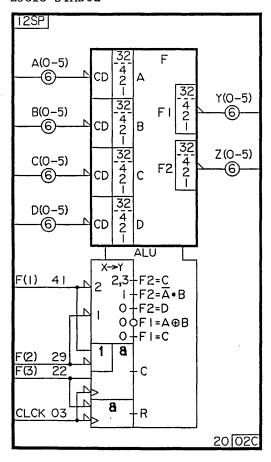
LOGIC SYMBOL



BIAS LØ = CLCK BIAS HI = F(4) 2 CØPIES PER ARRAY - M(O-1), N(O-1)

OPERATIONAL DESCRIPTION

N(N) = M(N).



BIAS LØ = F(4)BIAS HI = F(0)

OPERATIONAL DESCRIPTION

Registers

Clock on pin CLCK and control inputs F(1-3) control the registers. The F(1,2) inputs also control the ALU.

Clock modifier C clocks the A, B, C, and D highways into the their respective registers. $C = \overline{(F(1) \text{ OR } F(2))}$ AND CLCK.

Reset modifier R clears the registers. R = F(3) AND CLCK.

12SP-20 (Cont'd)

ALU

The outputs of the registers enter the ALU where they are weighted binarily and designated as operands A, B, C, and D. The ALU has two output operands designated F1 and F2. Output operands F1 and F2 are weighted binarily and leave the array on output highways Y and Z respectively. The F qualifying symbol indicates that the symbol is incomplete and the function information (contents of the F1 and F2 output operands) is expressed by equations in the common control block.

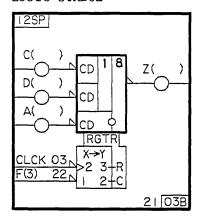
Input pins F(1) and F(2) are translated to control the F1 and F2 output operands.

A translation of O selects the C operand to Fl and the D operand to F2.

A translation of 1 selects an exclusive OR of the A and B operands to F1. F2 is an AND operation between the B operand and the complement of the A operand.

Translations of 2 and 3 both select an exclusive OR of the A and B operands to F1 and the C operand to F2.

60458120 B 2 of 2



BIAS LØ = F(0), F(2), F(4) BIAS HI = F(1) 2 CØPIES PER ARRAY \sim C(0-1), D(0-1), A(0-1), Z(0-1)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control input F(3) are translated to control the registers.

Translations of 0 or 1 activate no modifiers and therefore cause the registers to hold.

A translation of 2 clocks the C, D, and A highways into their respective registers.

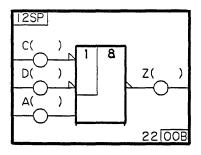
A translation of 3 clears the registers.

The outputs of the registers pass through the OR/AND logic.

 $Z(N) = (C(N) \text{ OR } D(N)) \text{ AND } \overline{A(N)}.$

12SP-22 OR/AND Logic.

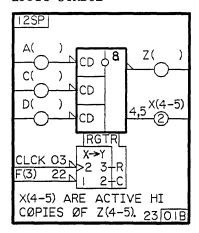
LOGIC SYMBOL



BIAS LØ = F(O), F(2), CLCK BIAS HI = F(I), F(3-4) 2 CØPIES PER ARRAY - C(O-I), D(O-I), A(O-I), Z(O-I)

OPERATIONAL DESCRIPTION

 $Z(N) = (C(N) \text{ OR } D(N)) \text{ AND } \overline{A(N)}.$



BIAS LØ = F(O-1), F(4) BIAS HI = F(2) 4 CØPIES PER ARRAY - A(2-5), C(2-5), D(2-5), Z(2-5), X(4-5)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control input F(3) are translated to control the registers.

Translations of 0 or 1 activate no modifiers and therefore cause the registers to hold.

A translation of 2 clocks the A, C, and D highways into their respective registers.

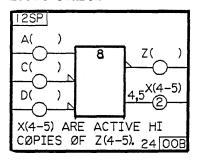
The outputs of the registers pass through the AND logic.

 $Z(N) = \overline{A(N)}$ AND C(N) AND D(N).

There is an active LO output for each result bit. There are active HI outputs only for the 2 least-significant bits.

12SP-24 AND Logic.

LOGIC SYMBOL

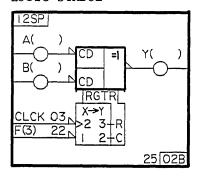


BIAS LØ = F(O-1), CLCK BIAS HI = F(2-4) 4 CØPIES PER ARRAY - A(2-5), C(2-5), D(2-5), Z(2-5), X(4-5)

OPERATIONAL DESCRIPTION

 $Z(N) = \overline{A(N)}$ AND C(N) AND D(N).

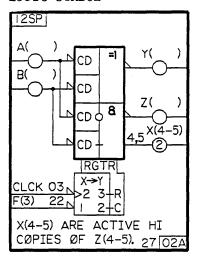
There is an active LO output for each result bit. There are active HI outputs only for the 2 least-significant bits.



BIAS LØ = F(O), F(4) BIAS HI = F(I-2) 6 CØPIES PER ARRAY - Δ (O-5), B(O-5), Y(O-5)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control input F(3) are translated to control the registers. Translations of 0 or 1 activate no modifiers and therefore cause the registers to hold. A translation of 2 clocks the A and B highways into their respective registers. The outputs of the registers pass through an exclusive OR. Y(N) = Z(N) exclusive OR B(N).



BIAS LØ = F(2), F(4), C(0-5)BIAS HI = F(0-1)6 CØPIES PER ARRAY - A(0-5), B(0-5), Y(0-5), Z(0-5)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control input F(3) are translated to control the registers.

Translations of 0 or 1 activate no modifiers and therefore cause the registers to hold.

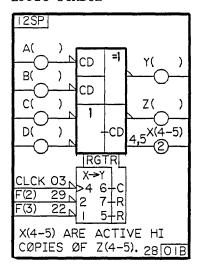
A translation of 2 clocks the A and B highways into two pairs of registers.

The outputs from the top pair of registers pass through the exclusive OR function. Y(N) = A(N) exclusive OR B(N).

The outputs from the bottom pair of registers pass through the AND function.

$$Z(N) = \overline{A(N)}$$
 AND $B(N)$.

There is an active LO output for each AND result bit. There are active HI outputs only for the 2 least-significant AND result bits.



BIAS LØ = F(1), F(4) BIAS HI = F(0) 6 CØPIES PER ARRAY - A(0-5), B(0-5), C(0-5), D(0-5)

OPERATIONAL DESCRIPTION

Clock on pin CLCK and control inputs F(2,3) are translated to control the registers.

Translations of 0-4 activate no modifiers and therefore cause the registers to hold.

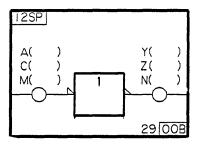
Translations of 5 or 7 clear the registers.

A translation of 6 clocks the A and B highways into their respective registers. Y(N) = A(N) exclusive OR B(N).

A translation of 6 also clocks the result of the OR function (C OR D) into its register. There is an active LO output from each bit of the register. There are active HI outputs only for the 2 least-significant bits.

12SP-29 Fanout.

LOGIC SYMBOL

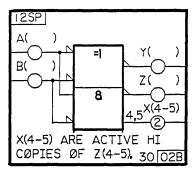


NØTE: INPUTS ARE A(O-5), C(O-5), M(O-1). ØUTPUTS ARE Y(O-5), Z(O-5), N(O-1).

BIAS LØ = CLCK, F(0-2), B(2-5), D(2-5) BIAS HI = F(3-4), B(0-1)

OPERATIONAL DESCRIPTION

Y(N) = A(N), Z(N) = C(N), N(N) = M(N).



BIAS LØ = CLCK, F(2), C(0-5)BIAS HI = F(0-1), F(3-4)

OPERATIONAL DESCRIPTION

Y(N) = A(N) exclusive OR B(N).

 $Z(N) = \overline{A(N)} \text{ AND } B(N).$

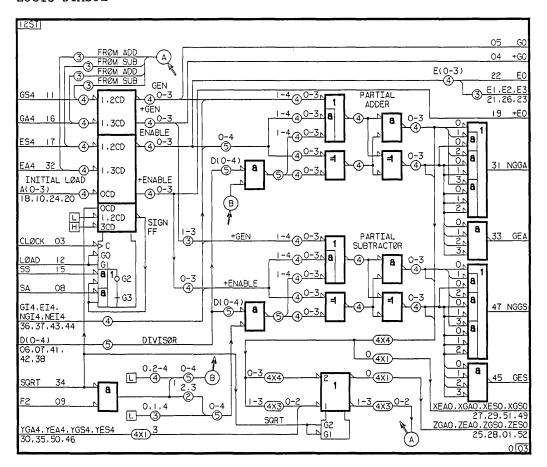
There is an active LO output for each AND gate bit. There are active HI outputs only for the 2 least-significant bits.

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12ST

PIN	REAL	VIRT
NAME	PIN	PIN
A _o	18	V01
A ₁	10	V02
A ₂	24	V03 V04
A ₃	20	
C D _o	03 06	V45 V09
D_0	07	V03 V10
D ₂	41	V11
D_3	42	V12
D_4	38	V13
EA ₄	32	V29
EI ₄	37	V43
ES₄	17	V33
F ₁	34 09	V18 V19
FORCE	02	V48
GA₄	16	V31
GI ₄	36	V37
GS₄	11	V35
L	12	V44
NEI₄	44	V41
NGI₄	43	V39
SA	08 13	V47 V46
YEA₄ YES₄	35 46	V21 V25
YGA₀	30	V23
YGS₄	50	V27
Eo	22	V05
E ₁	21	V06
E ₂	26	V07
E ₃	23	V08
G₀ GEA	05 33	V36 V15
GEA	33 45	V15 V17
NE _o	19	V40
NG₀	04	V38
NGGA	31	V14
NGGS	47	V16
XEA _o	27	V20
XGA₀	29	V22
XGS	49 51	V26 V24
XES _o	51 28	V24 V21
ZES	52	V32
ZGA ₀	25	V32 V30
ZGS	01	V34

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BIAS LØ = 02

60458120 D

12ST-0 (Cont'd)

OPERATIONAL DESCRIPTION

This circuit is a nonrestore divide network. There are 13 circuits of this type in a stack. This circuit can either doa divide or a square root operation.

The register element in the first column is used to generate a partial sum (enable) and a partial carry (generate). This sum and carry each consists of four bits (00 through 03). Depending on the G terms active, the terms GS4, ES4 or GA4, EA4 are input. For the initial loading, AO through A3 are forced to subtract. For each generate and enable a partial add and subtract are done. For the partial add and subtract, the divide terms DO through D4 are also input. The outcome of the partial add and subtract are both output through terms NGGA (not group generate add), GEA (group enable add), NGGS (not group generate subtract), and GES (group enable subtract). These terms are sent to the first level of the carry tree which determines the sign. If the sign is negative, an add is done; if positive, a subtract is done on the next cycle (SS and SA). The terms GO (generate O), NGO (not generate O), NEO (not enable 0), and EO (enable 0) are sent to the next higher-order bit position GI4, NGI4, NEI4, and NEI4, ensuring that the correct bit positions are used. The terms XEAO, XGAO, XESO, and XGSO are output to the next higher-order bit positions YEA4, YGA4, YES4, and YGS4. These are input to the gated input OR gate. IF Gl is active, the terms are used in the square root operation. The top output from the gated OR gate is ZGAO, ZEAO, ZGSO, and ZESO. These terms are output to the next higher-order chip at GA4, EA4, GS4, and ES4, respectively. The output is the desired result and is looped back to GA4, EA4, GS4, and ES4.

60458120 D 2 of 2

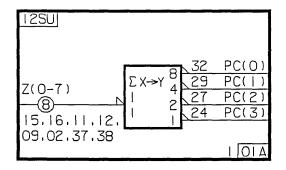
<u>12SU</u>

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	19	V09
A(1)	17	V10
A(2)	20	V11
A(3)	18	V12
A(4)	34	V13
A(5)	36	V14
A(6)	42	V15
A(7)	35	V16
B(0)	07	V30
B(1)	10	V31
B(2)	04	V32
B(3)	52	V33
B(4)	46	V34
B(5)	43	V35
B(6)	44	V36
B(7)	41	V37
Z(0)	15	V01
Z(1)	16	V02
Z(2)	11	V03
Z(3)	12	V04
Z(4)	09	V05
Z(5)	02	V06
Z(6)	37	V07
Z(7)	38	V08
C(0)	22	V17
C(1)	23	V18
C(2)	25	V19
C(3)	28	V20
C(4) C(5) C(6) C(7)	30 31 33 SAME AS P	V21 V22 V23
NC(0)	21	V28
NC(1)	26	V29
D(0)	06	V38
D(1)	04	V39
D(2)	01	V40
D(3)	31	V41
D(4)	49	V42
D(5)	50	V43
D(6)	48	V44
D(7)	47	V45
ND(0)	05	V46
ND(1)	03	V47
POPCNT POPCNT POPCNT POPCNT	(0) 32 (1) 29 (2) 27	V24 V25 V26 V27

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12SU-1 Summing Network.

LOGIC SYMBOL



BIAS LØ - 17, 18, 19, 20, 34, 35, 36, 42

OPERATIONAL DESCRIPTION

This circuit is a summing network. An array contains one circuit.

Each LO input (ZO-Z7) is assigned a value of one. The total number of LO inputs is decoded and the binary representation of that number appears at the output.

	Out	puts		
Number of LO inputs	32	29	27	24
0	H	H	Н	H
1	H	H	H	L
2	H	H	L	H
3	H	H	L	L
4	H	L	H	H
5	H	L	Н	L
6	H	L	L	H
7	H	L	L	L
8	L	Н	Н	Н

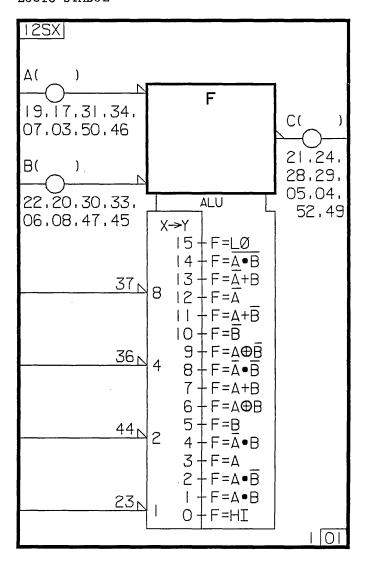
Term	Pin
Z0	15
Z1	16
Z2	11
Z3	12
. .	0.0
Z4	09
Z 5	02
Z6	37
z 7	38

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			*	

12SX

PIN	REAL	VIRT
NAME	PIN	PIN
A(0)	19	V01
A(1)	17	V02
A(2)	31	V03
A(3)	34	V04
A(4)	07	V05
A(5)	03	V06
A(6)	50	V07
A(7)	46	V08
B(0)	22	V09
V(1)	20	V10
B(2)	30	V11
B(3)	33	V12
B(4)	06	V13
B(5)	08	V14
B(6)	47	V15
B(7)	45	V16
M(0)	09	V17
M(1)	15	V18
M(2)	35	V19
M(3)	38	V20
M(4)	12	V21
M(5)	11	V22
M(6)	43	V23
M(7)	42	V24
F(1)	37	V33
F(2)	36	V34
F(3)	44	V35
F(4)	23	V36
F(5)	27	V37
F(6)	26	V38
F(7)	41	V39
F(8)	16	V40
F(9)	51	V46
S(1)	18	V41
S(2)	10	V42
C(0)	21	V25
C(1)	24	V26
C(2)	28	V27
C(3)	29	V28
C(4)	05	V29
C(5)	04	V30
C(6)	52	V31
C(7)	49	V32
H(1)	01	V43
H(2)	02	V44
H(3)	25	V45

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BIAS | (LØ) = NØNE BIAS O (HI μ = 16, 26, 27, 41, 51

12SX-1 (Cont'd)

OPERATIONAL DESCRIPTION

This circuit is a logic unit. An array contains eight circuits with common control.

The translator in the common control block has four inputs assigned binary weights and decoded to determine the logic operation performed by the logic unit.

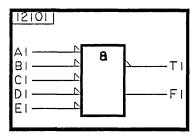
The table below shows the output, C, for each function.

Decoded	Logic	Α	=	Η	H	L	L
Value	Function	В	=	Н	L	H	L
0	ΗI			H	H	Н	Н
1	A.B			H	H	Н	L
1 2 3	A.B			Н	H	L	H
3	Α			Н	H	L	L
4	A.B			H	L	Н	H
4 5 6	В			Н	L	H	L
6	A B			H	L	L	Н
7	A+B			H	L	L	L
_							
8	A.B			L	H	H	H
9	A B			L	H	H	L
10	В			L	H	L	H
11	A_B			L	H	L	L
12	Α			L	L	H	H
13	<u>A+B</u>			L	L	H	L
14	A · B			L	L	L	Н
15	LO			L	L	L	L

Term	Pin	Term	Pin	Term	Pin
A0	19	во	22	C0	21
Al	17	Bl	20	C1	24
A2	31	В2	30	C2	28
A3	34	В3	33	C3	29
A4	07	В4	06	C4	05
A5	03	В5	08	C5	04
A6	50	В6	47	C6	52
A7	46	в7	45	С7	49

12101 AND Gate.

LOGIC SYMBOL

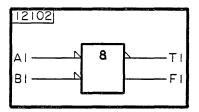


OPERATIONAL DESCRIPTION

(None required.)

12102 AND Gate.

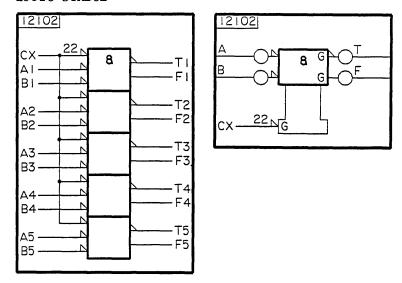
LOGIC SYMBOL



BIAS LØ=22

OPERATIONAL DESCRIPTION

(None required.)

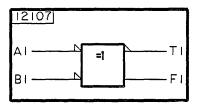


OPERATIONAL DESCRIPTION

Input CX is common to all the AND gates and must be enabled to activate the outputs. Inputs Al and Bl generate outputs Tl and Fl. Inputs A2 and B2 generate outputs T2 and F2, etc.

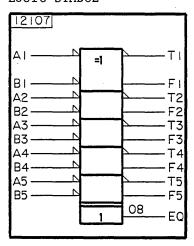
12107 Exclusive OR Gate.

LOGIC SYMBOL



OPERATIONAL DESCRIPTION

(None required.)



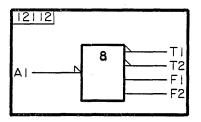
OPERATIONAL DESCRIPTION

The 12107 divides into two areas: the data input portion which consists of five exclusive OR functions (above the double line) and an OR function which is the common output block.

When any pair of inputs A and B consists of a HI and a LO, output EQ will be active (HI).

12112 AND Gate.

LOGIC SYMBOL



BIAS LØ = 22

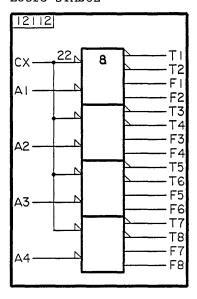
OPERATIONAL DESCRIPTION

Output Tl and T2 = Al.

Output F1 and F2 = $\overline{A1}$.

12112 Gated Fanout.

LOGIC SYMBOL



OPERATIONAL DESCRIPTION

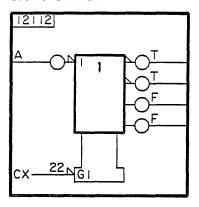
Input CX is common to all four AND gates.

Outputs T1 and T2 = A1 and outputs F1 and F2 = $\overline{A1}$.

Outputs T3 and T4 = A2 and outputs F3 and F4 = $\overline{A2}$, etc.

12112 (Cont'd)

LOGIC SYMBOL



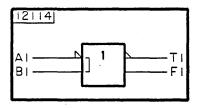
OPERATIONAL DESCRIPTION

Input CX must be active to enable input A.

When gating modifier Gl is active, the top two active LO output highways each equal input highway A and the bottom two active HI output highways each equal the complement of input highway A.

12114 Receiver.

LOGIC SYMBOL

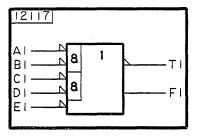


OPERATIONAL DESCRIPTION

The 12114 is an OR function with a grouping bracket on the input. This indicates that the inputs are a differential pair, carry only I bit of binary information and represent a single input. The input signals are always of opposite polarity, i.e. when one is HI the other is LO. The function is active when pin Al is LO and Bl is HI.

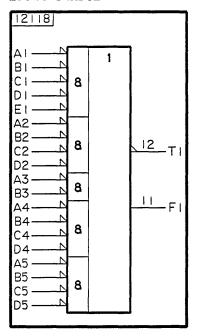
12117 Combination AND/OR.

LOGIC SYMBOL



OPERATIONAL DESCRIPTION

Output pin Tl = (Al \bullet Bl) + (Cl \bullet Dl) + El

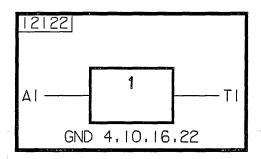


OPERATIONAL DESCRIPTION

Circuit operation is self-explanatory so no description is provided.

12122-1 Buffer Gate, 9-Bit.

LOGIC SYMBOL



OPERATIONAL DESCRIPTION

This symbol is a single section of 12122-2. The 12122 is a buffer gate. Whatever appears on the Al-input is output on the Tl-output.

12122							
	<u> </u>						
AI — 3	1	5TI					
A22		6 T2					
A3		7 T3					
A4 - 20		<u>12</u> T4					
A5 23		<u> 11</u> T5					
A6 <u>24</u>		<u>8</u>					
A7 <u>17</u>		_15T7					
A8 <u>18</u>		<u> 14</u> T8					
A9 <u>19</u>		<u>13</u> T9					
GND 4,10,16,22							

OPERATIONAL DESCRIPTION

NOTE

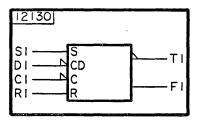
This symbol may appear in prints with pins as shown. Or it may appear with pins designated for a particular application.

The 12122 is a buffer gate. Whatever appears on an A-input is output on the corresponding T-output.

60458120 D

12130 Latch with Direct Set and Reset Inputs.

LOGIC SYMBOL



BIAS LØ = PINS 19, 20, 22

OPERATIONAL DESCRIPTION

The 12130 symbol shown above is a 1-bit latch. The latch has Direct Set (S1), Direct Reset (R1), Clock (C1), and Data (D1) inputs.

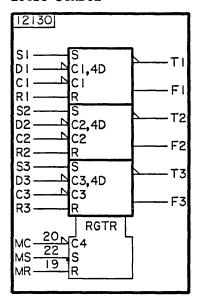
When the Sl input goes HI, the latch sets.

When the Rl input goes HI, the latch resets (clears).

This is RS latch, therefore when Rl and Sl are active at the same time, the state of the latch is unknown.

When input Cl goes LO, it clocks the data (input Dl) into the latch.

Outputs T1 and F1 are active LO and active HI outputs respectively from the latch.



OPERATIONAL DESCRIPTION

The 12130 symbol shown above is a 3-bit register. Each latch in the register has its own Direct Set (S1-3), Direct Reset (R1-3), Clock (C1-3), and Data (D1-3) inputs. In addition, there are Master Reset (MR), Master Set (MS), and Master Clock (MC) inputs which control all three latches.

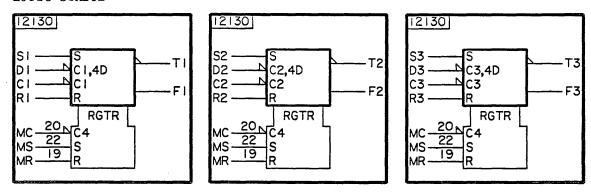
When the MS input goes HI, all three latches set.

When the MR input goes HI, all three latches reset (clear).

The S1-3 and R1-3 inputs set or reset their respective latches individually.

These are RS latches, therefore, if any latch receives both set and reset signals at the same time, the state of the latch is unknown.

When the MC input is LO, clock modifier C4 is active and the individual clock signals (inputs C1-3) are allowed to control the latches. Both clock modifiers (C4 and the respective individual clock modifier) must be active in order to clock data into a latch.



OPERATIONAL DESCRIPTION

The 12130 symbols shown above are three 1-bit latches. Each latch has its own Direct Set (S1-3), Direct Reset (R1-3), Clock (C1-3), and Data (D1-3) inputs. In addition there are Master Reset (MR), Master Set (MS), and Master Clock (MC) inputs which control all three latches.

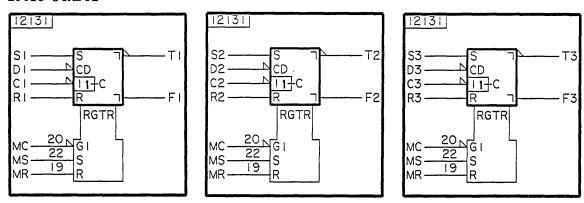
When the MS input goes HI, all three latches set.

When the MR input goes HI, all three latches reset (clear).

The S1-3 and R1-3 inputs set or reset their respective latches individually.

These are RS latches, therefore, if any latch receives both set and reset signals at the same time, the state of the latch is unknown.

When the MC input is LO, clock modifier C4 is active and the individual clock signals (inputs C1-3) are allowed to control the latches. Both clock modifiers (C4 and the respective individual clock modifier) must be active in order to clock data into a latch.



OPERATIONAL DESCRIPTION

The 12131 symbols shown above are 3-bit flip-flops with delayed outputs. Each flip-flop has its own Direct Set (S1-3), Direct Reset (R1-3), Clock (C1-3), and Data (D1-3) inputs. In addition there are Master Rest (MR), Master Set (MS), and Master Clock (MC) inputs which control all three flip-flops.

When the MS input goes HI, all three flip-flops set and all outputs go active with no delay.

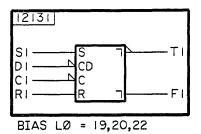
When the MR input goes HI, all three flip-flops reset and all outputs go inactive with no delay.

The S1-3 and R1-3 inputs set or reset their respective flip-flops individually. The outputs reflect the state of their respective flip-flops with no delay.

These are RS flip-flops, therefore if any flip-flop receives both set and reset signals at the same time, the state of the flip-flop is unknown.

When the MC input is LO, gating modifier Gl is active and the individual clock signals (Cl-3) are allowed to control the clock modifier (C) for their respective flip-flops. The clock modifier for a flip-flop is active when MC is LO and the respective individual clock input is LO.

When a clock modifier is active, it clocks data into the flip-flop. The output does not reflect the state of the flip-flop until the clock modifier goes inactive (MC or the individual clock input goes HI).



OPERATIONAL DESCRIPTION

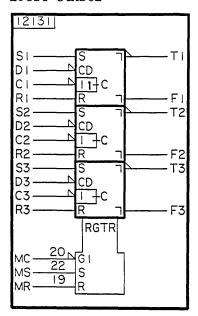
The 12131 symbol shown above is a 1-bit flip-flop with delayed outputs. The flip-flop has Direct Set (S1), Direct Reset (R1), Clock (C1) and Data (D1) inputs.

When the S1 input goes HI, the flip-flop sets and the outputs go active with no delay.

When the R1 input goes HI, the flip-flop resets (clears) and the outputs go inactive with no delay.

This is an RS flip-flop, therefore when Rl and Sl are active at the same time, the state of the flip-flop is unknown.

When input Cl goes LO, it clocks the data (input Dl) into the flip-flop. The outputs do not reflect the state of the flip-flop until Cl goes inactive (HI).



OPERATIONAL DESCRIPTION

The 12131 symbol shown above is a 3-bit register with delayed outputs. Each flip-flop in the register has its own Direct Set (S1-3), Direct Reset (R1-3), Clock (C1-3), and Data (D1-3) inputs. In addition there are Master Reset (MR), Master Set (MS), and Master Clock (MC) inputs which control all three flip-flops.

When the MS input goes HI, all three flip-flops set and all outputs go active with no delay.

When the MR input goes HI, all three flip-flops reset and all outputs go inactive with no delay.

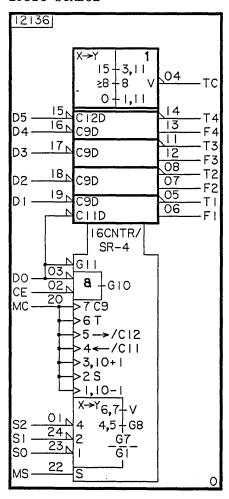
The S1-3 and R1-3 inputs set or reset their respective flip-flops individually. The outputs reflect the state of their respective flip-flops with no delay.

These are RS flip-flops, therefore if any flip-flop receives both set and reset signals at the same time, the state of the flip-flop is unknown.

When the MC input is LO, gating modifier G1 is active and the individual clock signals (C1-3) are allowed to control the clock modifier (C) for their respective flip-flops. The clock modifier for a flip-flop is active when MC is LO and the respective individual clock input is LO.

When a clock modifier is active, it clocks data into the flip-flop. The output does not reflect the state of the flip-flop until the clock modifier goes inactive (MC or the individual clock input goes HI).

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OPERATIONAL DESCRIPTION

The 12136-0 contains a 4-bit register which can be loaded from input pins, incremented, decremented, shifted in either direction, toggled, or forced set.

The count operation (increment or decrement) has a modulus of 16; i.e., 0 through 15. The counter is also circular; i.e., one count beyond 15 is 0 and one count less than 0 is 15.

The shift operation is an end-off shift of l-bit position in either direction with a serial bit input which fills data in behind the shifted data.

The 12136-0 symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the contents of the register. The register contents, gating modifiers G1, 3, 8, and 11, and OR modifier V control the carry output TC.

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12136-0 (Cont'd)

The middle area at the symbol is a 4-bit register. Control from the common control block (lower area of the symbol) can load, increment, decrement, shift, set, or toggle the contents of this register. Inputs Dl-4 are used for loading the 4-bit register. Input D5 is the serial bit input for a right (down) shift and D0 is the serial bit input for left (up) shift. Outputs Tl-4 are active (LO) outputs from the register and Fl-4 are active (HI) outputs.

The common control block on the bottom of the symbol contains the control for both the register and common output block.

Input DO is ANDed with input pin CE to form gating modifier G10 which is the count enable. DO controls gating modifiers G11 which enables the carry output (TC) when in count mode. DO also is the serial bit input for the left shift operation.

Inputs SO-2 are translated to form gating modifiers GI-7 which select the mode of operation. Translations of SO-2 also control gating modifier GS and GS modifier GS which are used in the common output block to control output GS.

MC is the master clock input which, during a transition to HI, clocks the operation selected by S0-2.

Input MS is the master set input and, when active (HI), will override all other inputs and set each bit of the register to a one.

Load Operation

A translation of 7 makes gating modifier G7 and OR modifier V active. V forces output TC LO. G7 enables MC to control clock modifier C9. C9 will become active during a HI transition of the master clock input. C9 clocks data from D1-4 into the register.

Toggle Operation

A translation of 6 makes gating modifier G6 and OR modifier V active. V forces output TC LO. G6 enables MC to control toggle modifier T. T will become active during a HI transition of the master clock input. T causes each bit in the register to change to its opposite state.

Right Shift Operation

A translation of 5 makes gating modifiers G5 and G8 active. G8 is used in the common output block to control the TC output when the register contents are greater than or equal to eight. Note that the register contents will be greater than or equal to eight any time the most-significant bit (top) is set. Thus when G8 is active, output TC will be the same as output T4.

G5 enables MC to control the right shift modifier (right arrow) and clock modifier Cl2. These modifiers will become active during a HI transition of the master clock input. The right shift modifier causes each bit in the register to shift down 1-bit position. Cl2 clocks data from input pin D5 into the most-significant bit of the register.

Left Shift Operation

A translation of 4 makes gating modifiers G4 and G8 active. G8 is used in the common output block to activate the TC output when the register contents are greater than or equal to eight. Note that the register contents will be greater than or equal to eight any time the most-significant bit (top) is set. Thus when G8 is active, output TC will be the same as output T4.

60458120 B 2 of 3

12136-0 (Cont'd)

G4 enables MC to control the left shift modifier (left arrow) and clock modifier Cll. These modifiers will become active during a HI translation of the master clock input. The left shift modifier causes each bit in the register to shift down 1-bit position. Cll clocks data from input pin D0 into the least-significant bit of the register.

Increment Operation

A translation of 3 makes gating modifiers G3 active. G3 is ANDed with G10, (count enable) to enable MC to control the count modifier (+1). The count modifier will become active during a HI transition of the master clock input. The +1 causes the contents of the register to increment by 1.

G3 is also ANDed with G11 in the common output block to enable a count of 15 to control the carry output TC. Thus TC will be active (LO) when G3 AND G11 are active AND the count is equal to 15.

Synchronous Set Operation

A translation of 2 makes gating modifier G2 active. G2 enables MC to control the set modifier S. S will become active during a HI transition of the master clock input. S will force each bit in the register to its active state.

Decrement Operation

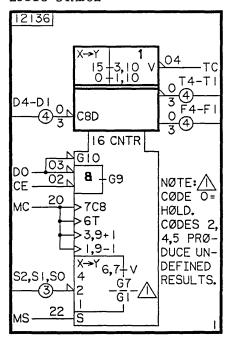
A translation of l makes gating modifier Gl active. G2 is ANDed with GlO (count enable) to enable MC to control the count modifier (-l). The count modifier will become active during a HI transition of the master clock input. The -l causes the contents of the register to decrement by l.

Gl is also ANDed with Gll in the common output block to enable a count of 0 to control the carry output TC. Thus TC will be active (LO) when Gl AND Gll are active AND the count is equal to 0.

No Operation

A translation of 0 does not make any gating modifier active. Therefore, all operations clocked by MC are disabled.

60458120 B



D5 (PIN 15) IS NØT USED. D4-D1 FEED CØUNTER BITS 0-3.

OPERATIONAL DESCRIPTION

The 12136-1 contains a 4-bit register which can be loaded from input pins, incremented, decremented, toggled, or forced set.

The count operation (increment or decrement) has a modulus of 16; i.e., 0 through 15. The counter is also circular; i.e., one count beyond 15 is 0 and one count less than 0 is 15.

The 12136-1 symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the contents of the register. The register contents, gating modifiers G1, 3, and I0, and OR modifier V control the carry output TC.

The middle area of the symbol is a 4-bit register. Control from the common control block (lower area of the symbol) can load, increment, decrement, set, or toggle the contents of this register. Inputs D4-1 are used for loading the 4-bit register. Output T4-1 are active (LO) outputs from the register and F4-1 are active (HI) outputs.

The common control block on the bottom of the symbol contains the control for both the register and common output block.

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12136-1 (Cont'd)

Input DO is ANDed with input pin CE to form gating modifier G9 which is the count enable. DO also controls gating modifier G10 which enables the carry output (TC) when in count mode.

Inputs S2-0 are translated to form gating modifiers G1-7 which select the mode of operation. Translations of S2-0 also controls OR modifier V which is used in the common output block to control output TC.

MC is the master clock input which, during a transition to HI, clocks the operation selected by S2-0.

Input MS is the master set input and, when active (HI), will override all other inputs and set each bit of the register to a one.

Load Operation

A translation of 7 makes gating modifier G7 and OR modifier V active. V forces output TC LO. G7 enables MC to control clock modifier C8. C8 will become active during a HI transition of the master clock input. C8 clocks data from D4-1 into the register.

Toggle Operation

A translation of 6 makes gating modifier G6 and OR modifier V active. V forces output TC LO. G6 enables MC to control toggle modifier T. T will become active during a HI transition of the master clock input. T causes each bit in the register to change to its opposite state.

Increment Operation

A translation of 3 makes gating modifier G3 active. G3 is ANDed with G0 (count enable) to enable MC to control the count modifier (+1). The count modifier will become active during a HI transition of the master clock input. The +1 causes the contents of the register to increment by 1.

G3 is also ANDed with G10 in the common output block to enable a count of 15 to control the carry output TC. Thus TC will be active (L0) when G3 AND G10 are active AND the count is equal to 15.

Decrement Operation

A translation of l makes gating modifier Gl active. Gl is ANDed with G9 (count enable) to enable MC to control the count modifier (-1). The count modifier will become active during a HI translation of the master clock input. The -l causes the contents of the register to decrement by l.

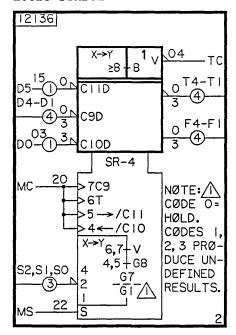
G1 is also ANDed with G10 in the common output block to enable a count of 0 to control the carry output TC. Thus TC will be active (LO) when G1 AND G10 are active AND the count is equal to 0.

No Operation

A translation of 0 does not make any gating modifier active. Therefore, all operations clocked by MC are disabled.

Translations of 2, 4, and 5 produce undefined results.

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D5 FEEDS SHIFT RGTR BIT O WHEN SHIFTING DØWN. D4-D1 FEED SHIFT RGTR BITS O-3 WHEN LØADING. DO FEEDS SHIFT RGTR BIT 3 WHEN SHIFTING UP.

OPERATIONAL DESCRIPTION

The 12136-2 contains a 4-bit register which can be loaded from input pins, shifted either direction, toggled, or forced set.

The shift operation is an end-off shift of l-bit position in either direction with a serial bit input which fills data in behind the shifted data.

The 12136-2 symbol divides into three areas from top to bottom. The common output block (above the double line) monitors the contents of the register. The register contents, gating modifier G8 and OR modifier V control the carry output TC.

The middle area of the symbol is a 4-bit register. Control from the common control block (lower area of the symbol) can load, shift, set, or toggle contents of this register. Inputs D4-1 are used for loading the 4-bit register. Input D5 is the serial bit input for a right (down) shift and D0 is the serial bit input for left (up) shift. Outputs T4-1 are active (L0) outputs from the register and F4-1 are active (HI) outputs.

The common control block on the bottom of the symbol contains the control for both the register and common output block.

12136-2 (Cont'd)

Inputs S2-0 are translated to form gating modifiers G1-7 which select the mode of operation. Translations of S2-0 also controls gating modifier G8 and G8 Modifier G8 which are used in the common output block to control output G8.

MC is the master clock input which, during a transition to HI, clocks the operation selected by S2-0.

Input MS is the master set input and, when active (HI), will override all other inputs and set each bit of the register to a one.

Load Operation

A translation of 7 makes gating modifier G7 and OR modifier V active. V forces output TC LO. G7 enables MC to control clock modifier C9. C9 will become active during a HI transition of the master clock input. C9 clocks data from D4-1 into the register.

Toggle Operation

A translation of 6 makes gating modifier G6 and OR modifier V active. V forces output TC LO. G6 enables MC to control toggle modifier T. T will become active during a HI transition of the master clock input. T causes each bit in the register to change to its opposite state.

Right Shift Operation

A translation of 5 makes gating modifiers G5 and G8 active. G8 is used in the common output block to activate the TC output when the register contents are greater than or equal to eight. Note that the register contents will be greater than or equal to eight any time the most-significant bit (top) is set. Thus when G8 is active, output TC will be the same as output T4.

G5 enables MC to control the right shift modifier (right arrow) and clock modifier Cll. These modifiers will become active during a HI transition of the master clock input. The right shift modifier causes each bit in the register to shift down one bit position. Cll clocks data from input pin D5 into the most-significant bit of the register.

Left Shift Operation

A translation of 4 makes gating modifiers G4 and G8 active. G8 is used in the common output block to activate the TC output when the register contents are greater than or equal to eight. Note that the register contents will be greater than or equal to eight any time the most-significant bit (top) is set. Thus when G8 is active, output TC will be the same as output T4.

G4 enables MC to control the left shift modifier (left arrow) and clock modifier C10. These modifiers will become active during a HI transition of the master clock input. The left shift modifier causes each bit in the register to shift down one bit position. C10 clocks data from input pin D0 into the least-significant bit of the register.

No Operation

A translation of 0 does not make any gating modifier active. Therefore, all operations clocked by MC are disabled.

Translations of 1, 2, or 3 produce undefined results.

60458120 B 2 of 2

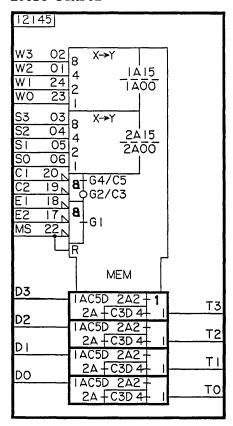
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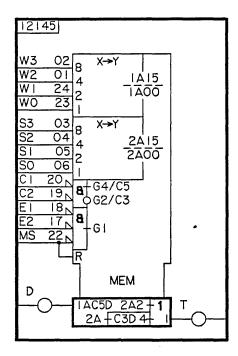
12141		
D7 15N C6D P7 16N C4D	14	<u>Q7</u>
P6 17N 04D	13	Q6
P5 18 C4D P4 19 C4D	12	Q5 Q4
P3 24 C4D	8 7	96 95 94 93 92 90 90
PI 2 C4D	6 5	QI
DO 4 N C4D C5D		QO.
C 20 SR-8 [> 3C4	1	
2 ← C5 > 1 → C6		
SI 23 2 G3 SO 22 I GI		

OPERATIONAL DESCRIPTION

The 12141-1 is a shift register. Input C is the enable required for any input to be accepted by the array. Inputs SO and SI define the type of shift on bits PO-P7 and DO,D7.

<u>s1</u>	<u>so</u>		
0	0	undefined	
0	1	translation Gl. input D7.	Bit shift is downward with new bit being drawn into C6D from
1	0	translation G2. input D0.	Bit shift is upward with new bit being drawn into C5D from
1	1	translation G3.	Register is loaded at all C4 bit locations (inputs PO-P7).





OPERATIONAL DESCRIPTION

The 12145 is a memory which can write or read 4-data bits to/from any 1 of 16 memory locations.

Inputs

W3-W0 are the write address bits which are translated to form the 1A address.

S3-S0 are the read address bits which are translated to form the 2A address.

 ${\tt C1}$ and ${\tt C2}$ are ANDed and control the write (gate active) and the read (gate inactive) operations.

E1, E2 and MS LO are ANDed to form the chip enable. When G1 is active, it enables the read data to the T outputs.

MS HI will clear the entire memory.

D designates the data inputs.

12145 (Cont'd)

Write Operation

C1 and C2 are both LO. Therefore G4 and C5 are both active and G2 and C3 are inactive. C5 clocks the input data (D) into the memory location specified by the lA address. G4 gates the contents of the read register (loaded during the previous read operation) to the T outputs.

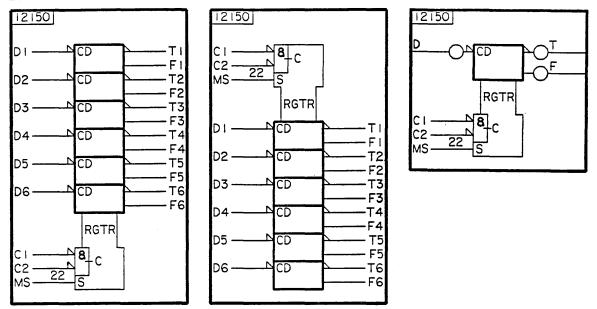
Read Operation

Cl and C2 are both HI. Therefore G2 and C3 are active and G4 and C5 are inactive. G2 gates the read data from the memory location specified by the A2 address to the T outputs. The contents of this same memory location are clocked into the read register by the C3 clock. G4 gates the contents of the read register to the T outputs during the next write operation.

60458120 B 2 of 2

12150 Register.

LOGIC SYMBOL

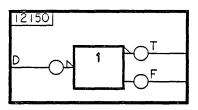


OPERATIONAL DESCRIPTION

Pins C1 and C2 are ANDed to clock the data (D) into the register(s). Master Set (MS) sets the register.

12150 Fanout.

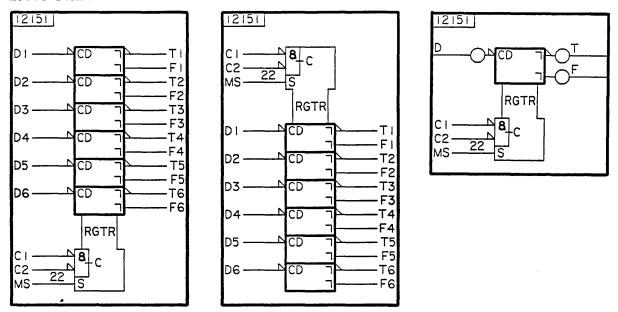
LOGIC SYMBOL



BIAS LØ = C1, C2, MS(23, 24, 22) BIAS HI = NØNE

OPERATIONAL DESCRIPTION

(None required.)

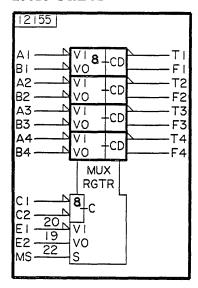


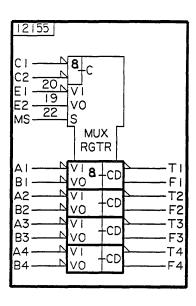
OPERATIONAL DESCRIPTION

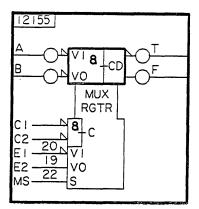
Pins Cl and C2 are ANDed to clock the selected data (D) into the register. Master Set (MS) sets the register.

When MS sets the register, the outputs all become active with no delay.

When the clock modifier clocks data into the register (C active), the outputs do not change state to equal the new contents of the register. The outputs change state only when the C modifier becomes inactive (C1 or C2 inputs go HI).







OPERATIONAL DESCRIPTION

Input pins El and E2 control the inputs to the mux and input pins Cl, C2, and MS control the register.

Register Control

C1 and C2 are ANDed to control the C (clock) modifier. C clocks the result of the mux into the register.

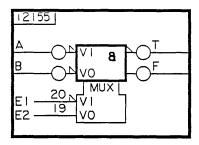
Mux Control

El and E2 control V (OR) modifiers which are used in an OR/AND function. The equation for the input to the register is as follows: (V1+A) o (V0+B)

Note from the above equation that the way to allow the A inputs to reach the register is to make VO active and VI inactive. This forces the B side of the AND gate active and allows the A inputs to control the other side.

The B inputs reach the register when VI is active and VO is inactive.

Note on the 12155 symbol that input El LO makes V1 active and input E2 HI makes V0 active. This design allows the connection of a single control signal to both the El and E2 inputs. Thus when the control signal is HI, V0 is active and V1 is inactive allowing the A inputs to reach the register. When the control signal is LO, V0 is inactive and V1 is active allowing the B inputs to reach the register.



BIAS LØ = CI, C2, MS(23, 24, 22) BIAS HI = NØNE

OPERATIONAL DESCRIPTION

E1 and E2 control V(OR) modifiers which are used in an OR/AND function. The equation for the mux is as follows: (V1 OR A) and (V0 OR B).

Note from the above equation that the way to allow the A inputs through the mux is to make VO active and VI inactive. This forces the B side of the AND gate active and allows the A inputs to control the other side.

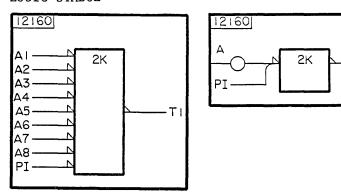
The B inputs pass through the mux when Vl is active and VO is inactive.

Note on the 12155 symbol that input El LO makes V1 active and input E2 HI makes V0 active. This design allows the connection of a single control signal to both the El and E2 inputs. Thus when the control signal is HI, V0 is active and V1 is inactive allowing the A inputs to pass through the mux. When the control signal is LO, V0 is inactive and V1 is active allowing the B inputs through the mux.

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12160 Parity Checker.

LOGIC SYMBOL

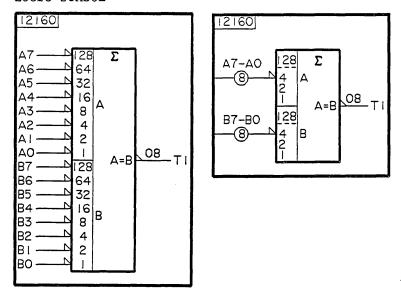


OPERATIONAL DESCRIPTION

Output Tl is active when an even number of inputs are LO.

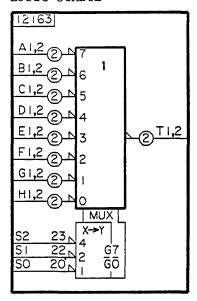
12160 (Cont'd)

LOGIC SYMBOL



OPERATIONAL DESCRIPTION

The 12160 is a pin-for-pin comparison of the A operand and the B operand. Output Tl is active LO when A equals B (i.e. AO = BO and Al = Bl, etc.).

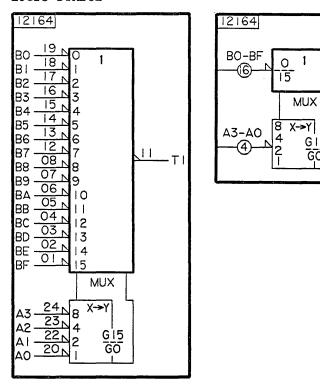


OPERATIONAL DESCRIPTION

Pins SO-2 select one of eight inputs to output T1, 2.

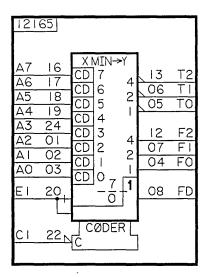
12164 16-Bit Multiplexer.

LOGIC SYMBOL





Pins A0-3 select 1 of 16 inputs to output T1.



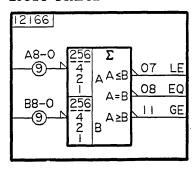
OPERATIONAL DESCRIPTION

The 12165-1 contains eight input latches with a common enable (C1) followed by encoding logic which generates the binary address of the highest priority input having a HIGH signal. The circuit operates as a single eight-input encoder when the mode control (pin 23) is biased HIGH. In the eight-input mode, T2, T1, T0 are the relevant outputs. A0 is the highest priority input and FD is the relevant Group Signal output. The FD output goes LOW when all inputs are LOW.

Inputs are latched when Cl goes HIGH. A HIGH signal on the Output Enable (E1) input forces all true outputs (Tn) HIGH and the FD output HIGH. Expansion to accommodate more inputs can be accomplished by connecting the FD output of a higher priority group to the El input of the next lower priority group.

60458120 D

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OPERATIONAL DESCRIPTION

The 12166 is a pin-for-pin highwayed comparison of the A operand and the B operand. When A is less than or equal to B, output LE is active (LO). When A equals B, output EQ is active (LO). Output GE is active (LO) when A is greater than or equal to B.

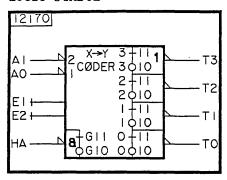
12166 Comparator.

LOGIC SYMBOL

131	66]					
A8 A7 A6 A5 A4 A3 A2 A1 A0 B8 B7 B6 B5 B4 B3 B2 B1 B0	20987767776777677767776777777777777777777	256 128 64 32 16 8 4 2 256 128 64 32 16 8 4 2 1	В	Σ Α≤Β Α=Β	07	LE EQ GE

OPERATIONAL DESCRIPTION

The 12166 is a pin-for-pin comparison of the A operand and the B operand. When A is less than or equal to B, output LE is active (LO). When A equals B, output EQ is active (LO). Output GE is active (LO) when A is greater than or equal to B.



BIAS LØ=7,18,1

OPERATIONAL DESCRIPTION

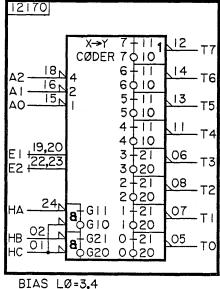
The 12170 is a coder which translates two input bits (A0,1) to activate one of four outputs. The A0,1 inputs enter the coder function where they are weighted binarily (A1 is the most-significant bit). The coder function translates the two inputs and activates one of four pairs of weighting modifiers on the output (Y side) of the function.

The pairs of translations feed OR functions where gating modifiers select either the true or complement state of the translation.

Gating modifier Gll gates the true translation to the output pins. GlO gates the complement of the translation to the output pins.

An AND gate in the lower left portion of the symbol controls the gating modifiers. Gll is active when the AND gate is active. GlO is active when the AND gate is inactive. Input HA controls the one-input AND gate.

Input pins El and E2 are active HI inhibits. When either El or E2 is active (HI), all the outputs of the coder function become inactive. The gating modifiers still operate to control the selection of the true or complement states of the coder function output.



BIAS LØ=3,4 BIAS HI=17

OPERATIONAL DESCRIPTION

The 12170 is a coder which translates 3-input bits (A0-2) to activate one of eight outputs. The A0-2 inputs enter the coder function where they are weighted binarily (A2 is the most-significant bit). The coder function translates the three inputs and activates one of eight pairs of weighting mofidiers on the output (Y side) of the function.

The pairs of translations feed OR functions where gating modifiers select either the true or complement state of the translation.

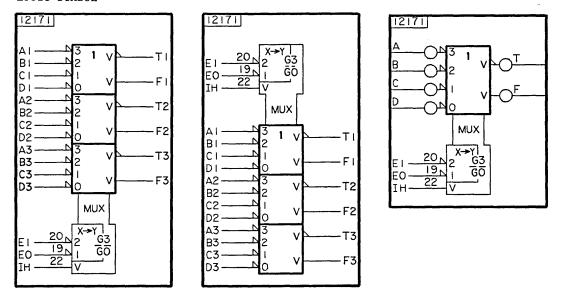
Gating modifiers G11 and G21 gate the true translation to the output pins. G10 and G20 gate the complement of the translation to the output pins.

Two AND gates in the lower left portion of the symbol control the gating modifiers. Gll and G21 are active when their respective AND gates are active. G10 and G20 are active when their respective AND gates are inactive. Inputs HA, HB, and HC control the AND gates.

Input pins E1 and E2 are active HI inhibits. When either pin E1 or E2 is HI, all the outputs of the coder function become inactive. The gating modifiers still operate to control the selection of the true or complement states of the coder function output.

12171 Four - Input Multiplexer.

LOGIC SYMBOL



OPERATIONAL DESCRIPTION

Pins EO and El select one of four inputs to outputs T and F.

When pin IH is HI during the select code, modifier V will be active, forcing output T true and output F HI.

60458120 F

12180-1 Summer, Tri-Input.

LOGIC SYMBOL

12180		
AO 16 N 32 AI 18N 16 A2 20N 8 A3 24N 4 A4 2N 2 A5 4N 1 BO 15N 32 BI 17N 16 B2 19N 8 B3 23N 4 B4 1 N 2 B5 3N 1 C1 22 1 C	ΣΑ.Β.C 32 16 8 4 2 1 ΣΑ.Β=63 ΣΑ.Β>63	12 TO 11 T1 8 T2 7 T3 6 T4 5 T5 13 PO 14 GO

OPERATIONAL DESCRIPTION

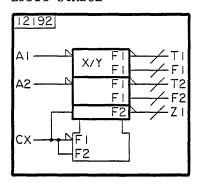
• The 12180-1 provides a summation of three inputs: two input-bit groups, A0-A5 and B0-B5 and the single-bit input C1. It sums as in this example:

An active A2 equals summation input 8 An active B3 equals summation input 4 Zero on C1 equals summation input 1

Sum is 13 causing output high on summation output 8, 4, 1 (Array outputs T2, T3, T5).

Summation output PO active when summation A and B output (C not considered) sum total 63.

Summation output GO active when summation A and B output (C not considered) sum total 64 or greater.



OPERATIONAL DESCRIPTION

The 12192 is a differential line driver. The inputs are standard logic levels (-1.7V and -.9V) and the pairs of T and F outputs connect to either 12114 circuits via twisted pair or TR30 transformers. The logic levels of the outputs depend on the connection.

When the 12192 connects to a 12114, the output logic levels are -0.8V and 0V.

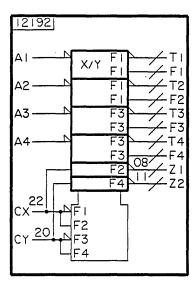
When the 12192 connects to a TR30 transformer, the output logic levels are -2.4 V and OV.

The CX input controls free dependency modifiers Fl and F2. When a free dependency modifier is active, it connects the function (in this case the X/Y level converter) to the outputs labeled with the same modifier. When a free dependency modifier is inactive, it disconnects the function from the output labeled with the same modifier. Thus when Fl is active (CX LO), input Al controls outputs Tl and Fl.

When Al is active (LO), the differential outputs Tl and Fl are both active. When Al is inactive (HI), the differential outputs are both inactive.

Output Zl is always tied to ground. F2 connects the function to ground when CX is HI. Thus when the CX signal disconnects the A inputs from the differential outputs, it connects the CX signal through the driver to ground. This serves as a load for the current source in the 12192 and reduces current spikes.

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OPERATIONAL DESCRIPTION

The 12192 is a differential line driver. The inputs are standard logic levels (-1.7V and -.9V) and the pairs of T and F outputs connect to either 12114 circuits via twisted pair or TR30 transformers. The logic levels of the outputs depend on the connection.

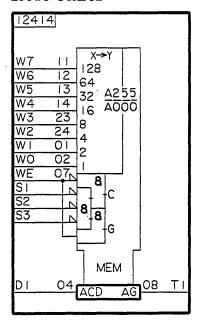
When the 12192 connects to a 12114, the output logic levels are -0.8V and OV.

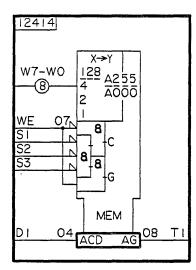
When the 12192 connects to a TR30 transformer, the output logic levels are -2.4 V and OV.

The CX and CY inputs control free dependency modifiers F1-4. When a free dependency modifier is active, it connects the function (in this case the X/Y level converter) to the outputs labeled with the same modifier. When a free dependency modifier is inactive, it disconnects the function from the output labeled with the same modifier. Thus when F1 is active (CX LO), input Al controls outputs T1 and T1.

When Al is active (LO), the differential outputs Tl and Fl are both active. When Al is inactive (HI), the differential outputs are both inactive.

Outputs Z1 and Z2 are always tied to ground. F2 and F4 connect these functions to ground when CX and CY are HI. Thus when the CX and CY signals disconnect the A inputs from the differential outputs, it connects the CX and CY signals through the drivers to ground. This serves as a load for the current source in the 12192 and reduces current spikes.





OPERATIONAL DESCRIPTION

The 12414 is a memory which can write or read a single data bit to/from any 1 of 256 memory locations.

Inputs

S1, S2, S3, along with WE LO are ANDed to control the write clock (C).

S1, S2, S3, along with WE HI are ANDed to control the read gate (G).

W7-0 are translated to form the write or read address.

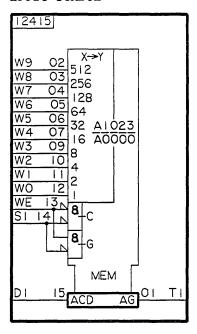
Dl is the data input.

Write Operation

When the C (clock) modifier is active, it clocks the input data (D1) into the memory location specified by the W7-0 write address.

Read Operation

When the G (gating) modifier is active, it gates data from the memory location specified by the W7-0 read address.



OPERATIONAL DESCRIPTION

The 12415 is a memory which can read or write the data bit to/from any $1_{.}$ of 1024 memory locations.

Inputs

WE and S1 (both LO) are ANDed to control the write clock (C).

WE HI and S1 LO are ANDed to control the read gate (G).

W9-0 are translated to form the write or read address.

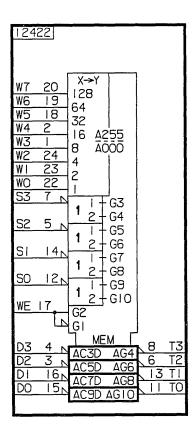
Dl is the data input.

Write Operation

When the C (clock) modifier is active, it clocks the input data (D1) into the memory location specified by the W9-0 write address.

Read Operation

When the G (gating) modifier is active, it gates data from the memory location specified by the W9-O read address.



OPERATIONAL DESCRIPTION

The 12422 is a memory which can write or read 4-data bits to/from any 1 of 256 memory locations.

Inputs

W7 through W0 are the write/read address bits which are translated to form the write/read address.

WE controls the write (gate active (LO)) and read (gate active (HI)) operations.

S3 through S0 are the bit selector inputs which select the appropriate data inputs.

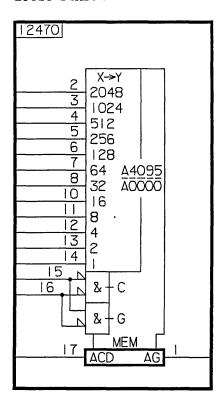
D3 through D0 are the data inputs.

Write Operation

WE is active (LO). Therefore G10 is inactive and C5 is active. C5 clocks the input data (D3-D0) as specified by the bit selector inputs (S3-S0).

Read Operation

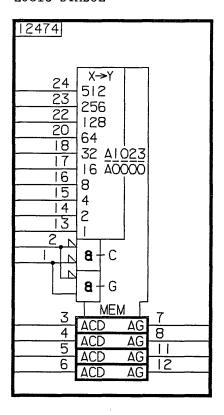
WE is active (HI). Therefore, G10 is active and C5 is inactive. G10, along with G9-G6, gates the read data from the specified memory location to outputs T3-T0.



OPERATIONAL DESCRIPTION

The 12470 directs a single data bit (input pin 17) by address inputs (array inputs 2-14) to one of 4096 memory locations. Input pins 15 and 16 must both be high to translate enable C which gates address and data into this element. On the lower part of the symbol, in term ACD, A is address, D is data, and C is the enable for both. To gate out of the array, input pin 15 must be high and 16 low to translate enable G.

60458120 D



OPERATIONAL DESCRIPTION

The 12474 directs four data bits (input pins 3-6) by address inputs (array inputs 13-24) to one of 1024 memory locations. Input pins 1 and 2 must both be high to translate enable C which gates address and data into this element. On the lower part of the symbol, in terms ACD, A is address, D is data, and C is the enable for both. To gate out of the array, input pin 2 must be high and 1 low to translate enable G.

121HA

121HA PARITY

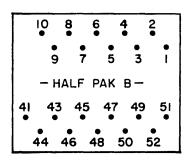
PIN NAME	RE. PI A	–	VIRT PIN	FLAT PAK PIN
IVAIVIE			FIIN	
A(0)	20	46	V01	01
A(1)	19	45	V02	02
A(2)	22	48	V03	03
A(3)	21	47	V04	04
A(4)	24	50	V05	05
A(5)	15	41	V06	22
A(6)	18	44	V07	23
A(7)	17	43	V08	24
API	23	49	V09	06
B(0)	29	03	V11	13
B(1)	30	04	V12	14
B(2)	31	05	V13	15
B(3)	32	06	V14	16
B(4)	33	07	V15	17
B(5)	34	08	V16	18
B(6)	35	09	V17	19
B(7)	36	10	V18	20
BPI	28	02	V19	12
AT1	26	52	V10	07
BT1	27	01	V20	11

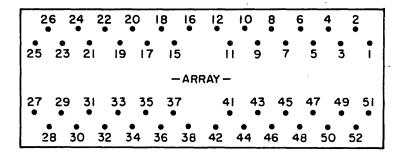
121HA COMPARATOR

PIN	RE PI	AL N	VIRT	FLAT PAK
NAME	A	В	PIN	PIN
A(0)	18	44	V01	23
A(1)	36	10	V02	20
A(2)	34	80	V03	18
A(3)	32	06	V04	16
A(4)	30	14	V05	14
A(5)	24	50	V06	05
A(6)	22	48	V07	03
A(7)	20	46	V08	01
B(0)	15	41	V11	22
B(1)	35	09	V12	19
B(2)	33	07	V13	17
B(3)	31	05	V14	15
B(4)	29	03	V15	13
B(5)	21	47	V16	04
B(6)	19	45	V17	02
B(7)	17	43	V18	24
T1	25	51	V20	08

26 24 22 20 18
25 23 21 19 17 15

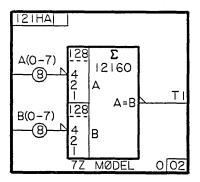
- HALF PAK A27 29 31 33 35
28 30 32 34 36





121HA-0 Comparator.

LOGIC SYMBOL



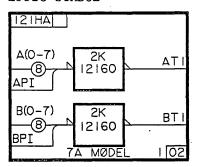
BIAS NØNE

OPERATIONAL DESCRIPTION

The 121HA-O is a pin-for-pin comparison of the A operand and the B operand. Output T1 is active LO when A equals B (i.e. AO=BO and Al=B1, etc.).

121HA-1 Parity Checks.

LOGIC SYMBOL



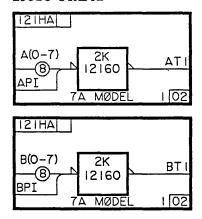
BIAS NØNE

OPERATIONAL DESCRIPTION

The 121HA-1 is a dual parity checker. Each parity checker has 9 inputs (8 data, 1 parity). Outputs AT1 and BT1 are active when an even number of inputs are LO.

121HA-1 (Cont'd)

LOGIC SYMBOL



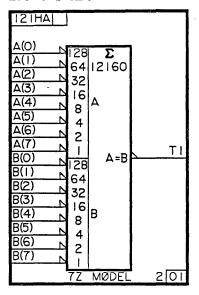
BIAS = NØNE NØTE: THIS IS NØT AN X SECTIØN

OPERATIONAL DESCRIPTION

Each parity checker has 9 inputs (8 data, 1 parity). Outputs AT1 and BT1 are active when an even number of inputs are ${\tt IO}$.

121HA-2 Comparator.

LOGIC SYMBOL



BIAS NONE

. OPERATIONAL DESCRIPTION

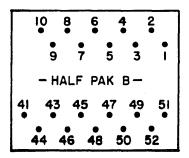
The 121HA-2 is a pin-for-pin comparison of the A operand and the B operand. Output Tl is active LO when A equals B (i.e. AO=BO and Al=Bl, etc.).

121HB

121HB (12112)

	REAL								
PIN	Р	IN	VIRT	PAK					
NAME	Α	В	PIN	PIN					
A(0)	17	43	V05	24					
A(1)	18	44	V06	23					
A(2)	36	10	V07	20					
A(3)	35	09	V08	19					
сх	15	41	V10	22					
F1(0)	22	48	V31	03					
F1(1)	23	49	V32	06					
F1(2)	29	03	V33	13					
F1(3)	32	06	V34	16					
F2(0)	21	47	V39	04					
F2(1)	24	50	V40	05					
F2(2)	30	04	V41	14					
F2(3)	31	05	V42	15					
T1(0)	20	46	V15	01					
T1(1)	25	51	V16	08					
T1(2)	27	01	V17	11					
T1(3)	34	80	V18	18					
T2(0)	19	45	V23	02					
T2(1)	26	52	V24	07					
T2(2)	28	02	V25	12					
T2(3)	33	07	V26	17					

26 24 22 20 18 25 23 21 19 17 15 -HALF PAK A-27 29 31 33 35 28 30 32 34 36



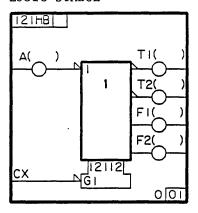
26 24 22 20 18 16 12 10 8 6 4 2
25 23 21 19 17 15 11 9 7 5 3 1

-ARRAY27 29 31 33 35 37 41 43 45 47 49 51
28 30 32 34 36 38 42 44 46 48 50 52

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121HB-0 Gated Fanout.

LOGIC SYMBOL



BIAS NØNE

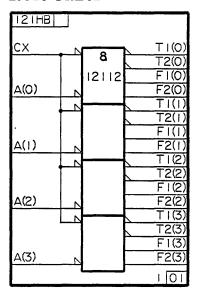
OPERATIONAL DESCRIPTION

Input CX must be active to enable input A.

When gating modifier Gl is active, the top two active LO output highways each equal input highway A and the bottom two active HI output highways each equal the complement of input highway A.

121HB-1 Gated Fanout.

LOGIC SYMBOL



BIAS NONE

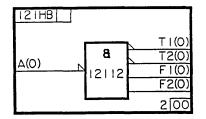
OPERATIONAL DESCRIPTION

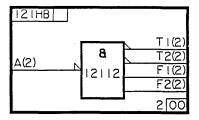
Input CX is common to all four AND gates.

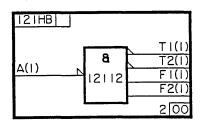
Outputs T1 and T2 = A and outputs F1 and F2 = \overline{A} .

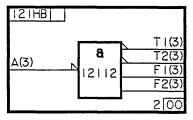
121HB-2 AND Gate.

LOGIC SYMBOL









NØTE: THESE ARE $\underline{\text{NØT}}$ X-SECTIØNS, NØTE THE UNIQUE PIN NAMES

BIAS LØ = CX BIAS HI = NØNE

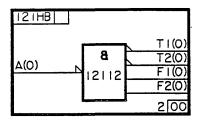
OPERATIONAL DESCRIPTION

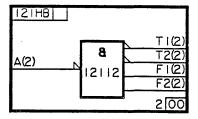
Outputs T(1) and T(2) = A.

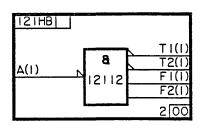
Outputs F(1) and F(2) = A.

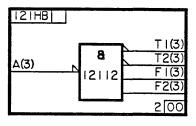
121HB-2 AND Gate.

LOGIC SYMBOL









BIAS LØ = CX BIAS HI = NØNE

OPERATIONAL DESCRIPTION

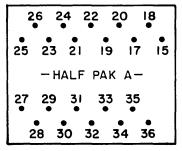
Outputs T(1) and T(2) = A.

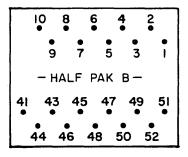
Outputs F(1) and F(2) = A.

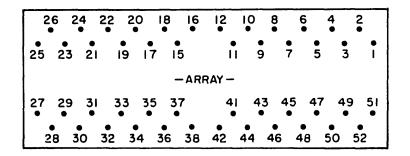
121HC

121HC (12145)

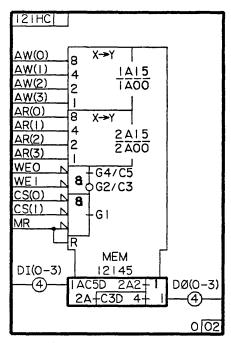
121110 (12110)							
PIN NAME	Р	AL IN	VIRT	FLAT PAK			
IVAIVIE	A	В	PIN	PIN			
AR(0) AR(1) AR(2) AR(3)	23 24 21 22	49 50 47 48	R0 R1 R2 R3	06 05 04 03			
~(5)	~~	70	113	03			
AW(0) AW(1) AW(2) AW(3)	18 17 20 19	44 43 46 45	W0 W1 W2 W3	23 24 01 02			
CS(0) CS(1) DI(0) DI(1)	33 34 32 31	07 08 06 05	CS0 CS1 D0 D1	17 18 16 15			
DI(2) DI(3) MR WE0	30 29 15 35	04 03 41 09	D2 D3 MR WE0	14 13 22 19			
WE1	36	10	WE1	20			
DO(0) DO(1) DO(2)	26 25 27	52 51 01	DO0 DO1 DO2	07 08 11			
DO(3)	28	02	DO3	12			







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BIAS NØNE

OPERATIONAL DESCRIPTION

The 121HC is a memory which can write or read 4-data bits to/from any 1 of 16 memory locations.

Inputs

AW (0-3) are the write address bits which are translated to form the 1A address.

AR (0-3) are the read address bits which are translated to form the 2A address.

WEO, and WEI are ANDed and control the write (gate active) and the read (gate inactive) operations.

CS (0,1) and MR LO are ANDed to form the chip enable. When Gl is active it enables the read data to the DO (0-3) outputs.

MR HI will clear the entire memory.

DI (0-3) are the data inputs.

Write Operation

WEO and WEI are both LO. Therefore G4 and C5 are both active and G2 and C3 are inactive. C5 clocks the input data (DI(0-3)) into the memory location specified by the lA address. G4 gates the contents of the read register (loaded during the previous read operation) to output highway DO (0-3).

Read Operation

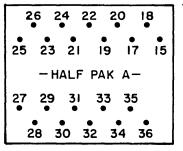
WEO and WE1 are both HI. Therefore G2 and C3 are active and G4 and C5 are inactive. G2 gates the read data from the memory location specified by the A2 address to the DO (0-3) outputs. The contents of this same memory location are clocked into the read register by the C3 clock. G4 gates the contents of the read register to the output during the next write operation.

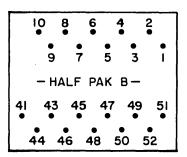
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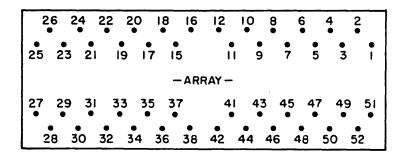
121HD

121HD (12414)

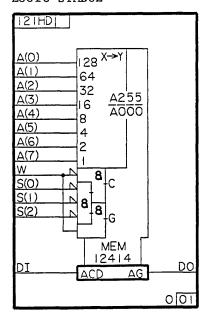
PIN NAME	–	AL IN B	VIRT PIN	FLAT PAK PIN
A(0)	27	01	A0	11
A(1)	28	02	A1	12
A(2)	29	03	A2	13
A(3)	30	04	A3	14
A(4)	18	44	A4	23
A(5)	17	43	A5	24
A(6)	20	46	A6	01
A(7)	19	45	A7	02
DI	21	47	DI	04
S(0)	32	06	S0	16
S(1)	35	09	S1	19
S(2)	36	10	S2	20
W	26	52	W	07
DO	25	51		08







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BIAS NONE

OPERATIONAL DESCRIPTION

The 121HD-0 is a memory which can write or read a single data bit to/from any 1 of 256 memory locations.

Inputs

S(0), S(1), S(2), along with W LO are ANDed to control the write clock (C).

S(0), S(1), S(2), along with W HI are ANDed to control the read clock (G).

A(0-7) are translated to form the write or read address.

DI is the data input.

Write Operation

When the C (clock) modifier is active, it clocks the input data (DI) into the memory location specified by the A(0-7) write address.

Read Operation

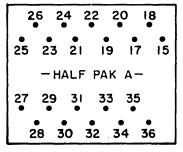
When the G (gating) modifier is active, it gates data from the memory location specified by the A(0-7) read address.

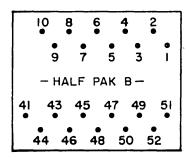
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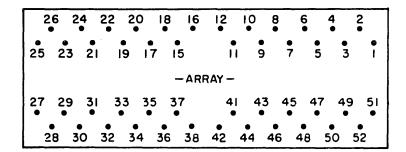
121HE

121HE (12102)

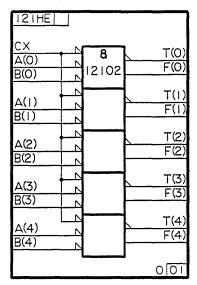
PIN NAME	RE PI A	AL N B	VIRT	FLAT PAK PIN
		<u> </u>		
A(0)	20	46	V02	01
A(1)	22	48	V04	03
A(2)	33	7	V06	17
A(3)	35	9	V08	19
A(4)	18	44	V10	23
B(0)	19	45	V03	02
B(1)	21	47	V05	04
B(2)	34	8	V07	18
B(3)	36	10	V09	20
B(4)	17	43	V11	24
CX	15	41	V01	22
F(0)	26	52	V13	07
F(1)	23	49	V15	06
F(2)	31	5	V17	15
F(3)	30	4	V19	14
F(4)	27	1	V21	11
T(0)	25	51	V12	08
T(1)	24	50	V14	05
T(2)	32	6	V16	16
T(3)	29	3	V18	13
T(4)	28	2	V20	12

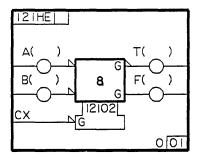






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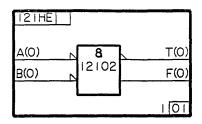
BIAS NØNE

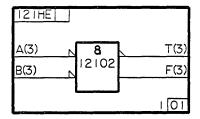
OPERATIONAL DESCRIPTION

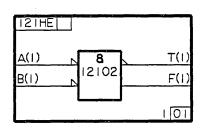
Input CX is common to all the AND gates and must be enabled to activate the outputs. Inputs A(0) and B(0) generate outputs T(0) and F(0). Inputs A(1) and B(1) generate outputs T(1) and F(1), etc.

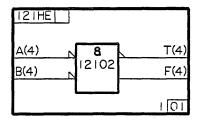
121HE-1 AND Gates.

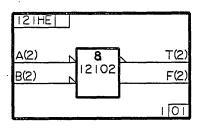
LOGIC SYMBOL











NØTE: THESE ARE <u>NØT</u> X-SECTIØNS. NØTE THE UNIQUE PIN NAME ANNØTATIØN.

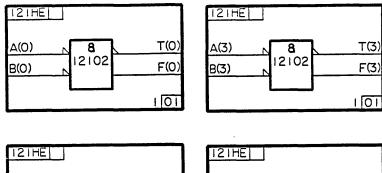
BIAS LØ = CX BIAS HI = NØNE

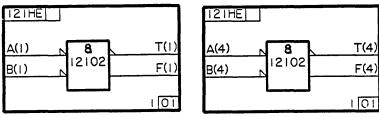
OPERATIONAL DESCRIPTION

(None required.)

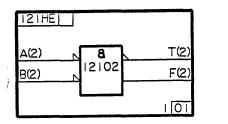
121HE-1 (Cont'd)

LOGIC SYMBOL





41.20



OPERATIONAL DESCRIPTION

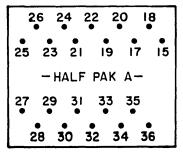
(None required.)

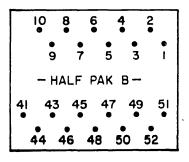
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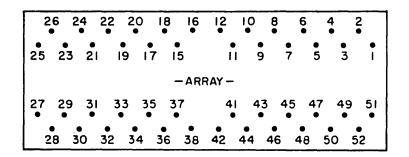
121HF

121HF (12101)

	FLAT			
PIN		AL IN	VIRT	PAK
NAME	Α	В	PIN	PIN
A(0)	19	45	Α0	02
A(1)	20	46	A1	01
A(2)	31	05	A2	15
B(0)	22	48	B0	03
B(1)	36	10	B1	20
B(2)	32	06	B2	16
C(0)	21	47	CO	04
C(1)	15	41	C1	22
C(2)	33	07	C2	17
D(0)	24	50	D0	05
D(1)	18	44	D1	23
D(2)	34	08	D2	18
E(0)	23	49	E0	06
E(1)	17	43	E1	24
E(2)	35	09	E2	19
F(0)	25	51	F0	08
F(1)	28	02	F1	12
F(2)	29	03	F2	13
T(0)	26	52	T0	07
T(1)	27	01	T1	11
T(2)	30	04	T2	14



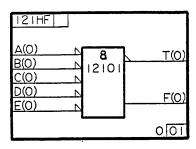


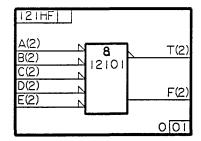


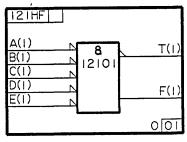
· •		

121HF-0 AND Gates.

LOGIC SYMBOL





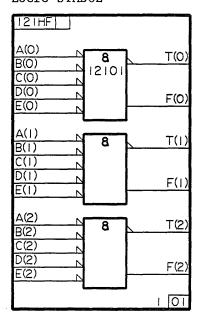


BIAS NØNE

OPERATIONAL DESCRIPTION

(None Required.)

LOGIC SYMBOL



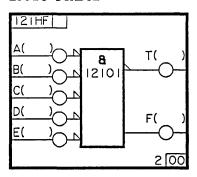
BIAS NONE

OPERATIONAL DESCRIPTION

(None required.)

121HF-2 AND Gates.

LOGIC SYMBOL



BIAS NØNE

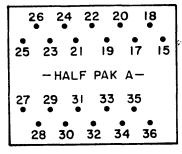
OPERATIONAL DESCRIPTION

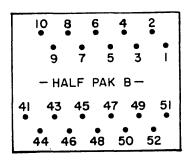
(None Required.)

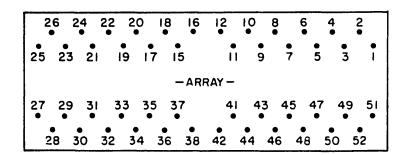
.

121HH 121HH (12166)

	RE	FLAT		
PIN	PI		VIRT	PAK
NAME	<u>A</u>	В	PIN	PIN
A(0)	36	10	V01	20
A(1)	35	9	V02	19
A(2)	34	8	V03	18
A(3)	33	7	V04	17
A(4)	32	6	V05	16
A(5)	31	5	V06	15
A(6)	30	4	V07	14
A(7)	29	3	V08	13
A(8)	28	2	V09	12
B(0)	15	41	V10	22
B(1)	18	44	V11	23
B(2)	17	43	V12	24
B(3)	20	46	V13	1
B(4)	19	45	V14	2
B(5)	22	48	V15	3
B(6)	21	47	V16	4
B(7)	24	50	V17	5
B(8)	23	49	V18	6
EQ	25	51	V19	8
GE	27	1	V20	11
LE	26	52	V21	7







MC37 1197

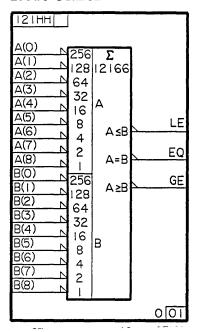
្រក្សាល់កែលខណ្ឌ ប្រធានក្បារ ១ ភូមិ ប្រភព សា សា ខែការប្រ

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121HH-0 Comparator.

LOGIC SYMBOL



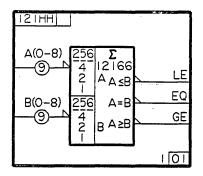
BIAS NØNE

OPERATIONAL DESCRIPTION

The 121 HH-O is a pin-for-pin comparison of the A operand and the B operand. When A is less than or equal to B, output LE is active LO. When A equals B, output EQ is active LO. Output GE is active LO when A is greater than or equal to B.

121HH-1 Comparator.

LOGIC SYMBOL



BIAS NONE

OPERATIONAL DESCRIPTION

The 121HH-1 is a pin-for-pin highwayed comparison of the A operand and the B operand. When A is less than or equal to B, output LE is active LO. When A equals B, output EQ is active LO. Output GE is active LO when A is greater than or equal to B.

CDC key to level 4 Logic Diagrams Symbol Descriptions

12DA through 12DD, 12SA through 12SX, 12101 through

MANUAL TITLE:

12422, 121HA through 121HH Volume 2 Logic Diagram

Symbols Manual

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